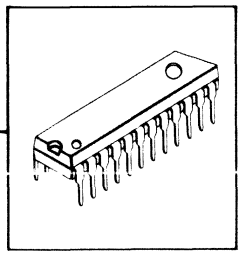
SAMSUNG

Data Book

Linear IC

Vol. 1, 1992



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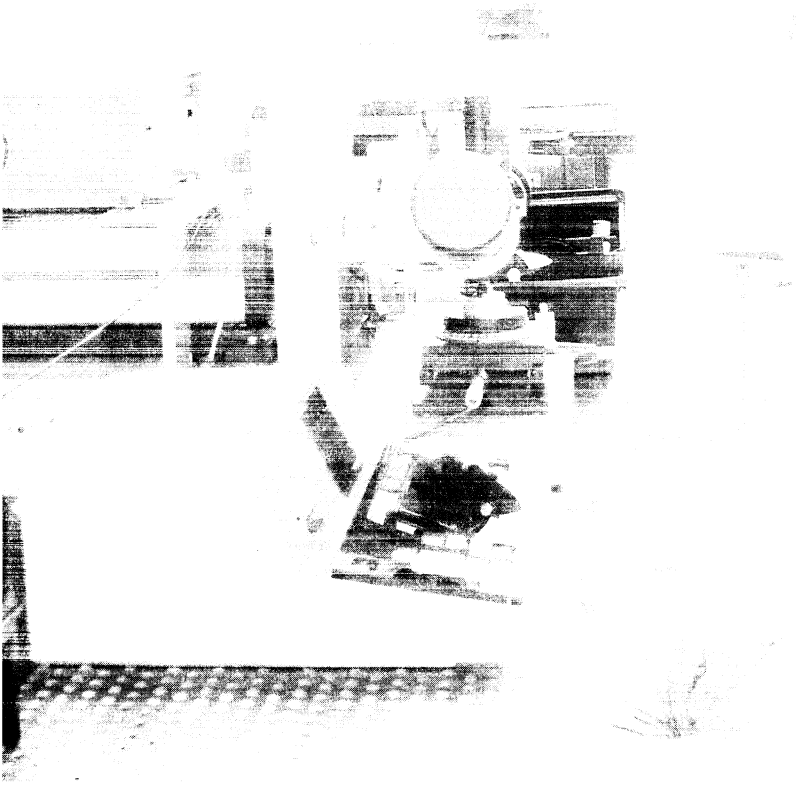
QUALITY & RELIABILITY 1



QUALITY and RELIABILITY

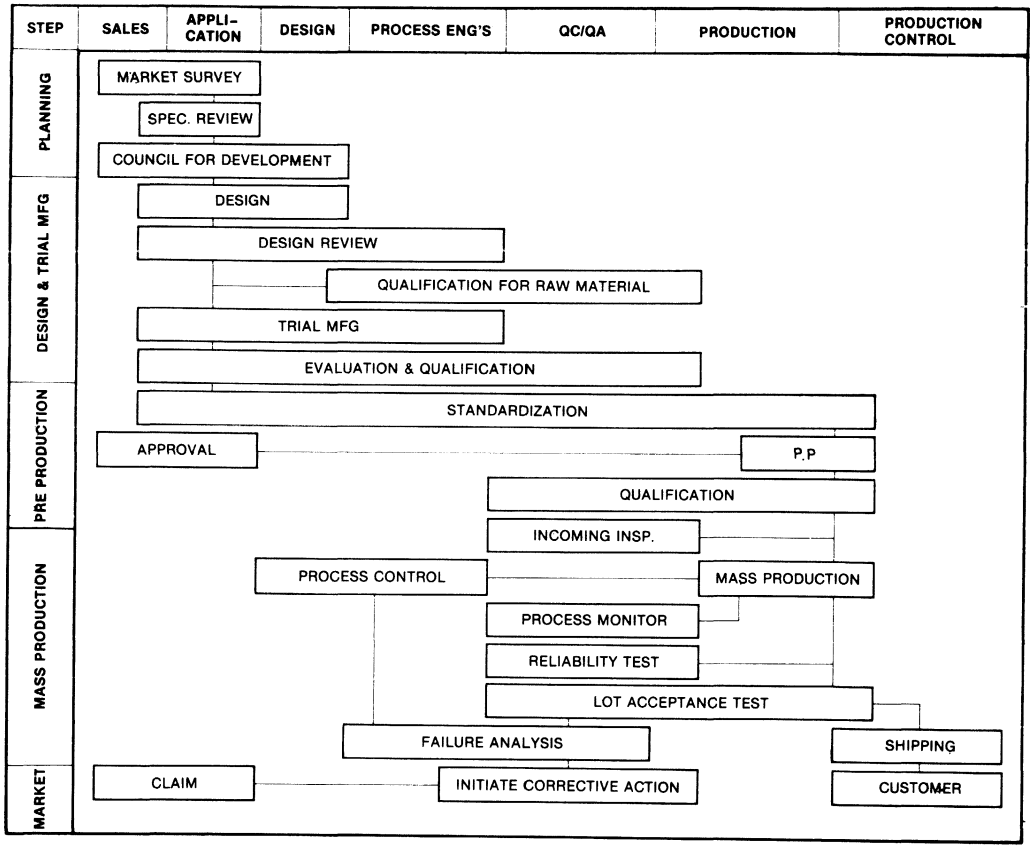
1. INTRODUCTION

SEC has been providing a wide variety of semiconductor products to the world since 1974. Since this time, extensive in-sights have been gained to create methods which most effectively result in reliable products. The worldwide customers of SEC have encouraged and helped develop the existing manufacturing and quality philosophy that is a way of life for SEC management and it's employees. This philosophy dictates the need for a zero defect environment throughout SEC's processes leading ultimately to total customer satisfaction. By developing and using methods of Statistical Process Control and Statistical Quality Control, SEC has made great strides in improving product quality & reliability. The direct result of these improvements has been reduced product DPM (Defects Per Million) to levels below customer requirements. SEC's repeated ability to exceed requirements for customer's "Dock to Stock" programs and its commitments to all its customers' needs, has made SEC the company to watch as we move ahead into the 1990's and beyond.

SEC's linear IC products are among the most reliable in the industry. SEC has always made a commitment to achieve the highest possible quality, reliability, and customer satisfaction with its products. Extensive qualification, monitoring and outgoing programs are used to scrutinize product quality and reliability. Stringent controls are applied to every wafer fabrication and assembly lot to achieve reproducibility, and, therefore, maintain product reliability.

In this chapter, the quality and reliability programs established at SEC will be discussed. In addition, a description of reliability theory, reliability tests, and various support efforts provides a broad framework from which to comprehend SEC quality and reliability.

To better understand the Quality Department's role in product development and manufacturing, a detailed diagram is listed below. As can be noted, Quality Engineering is involved in all phases, save that of initial product planning.

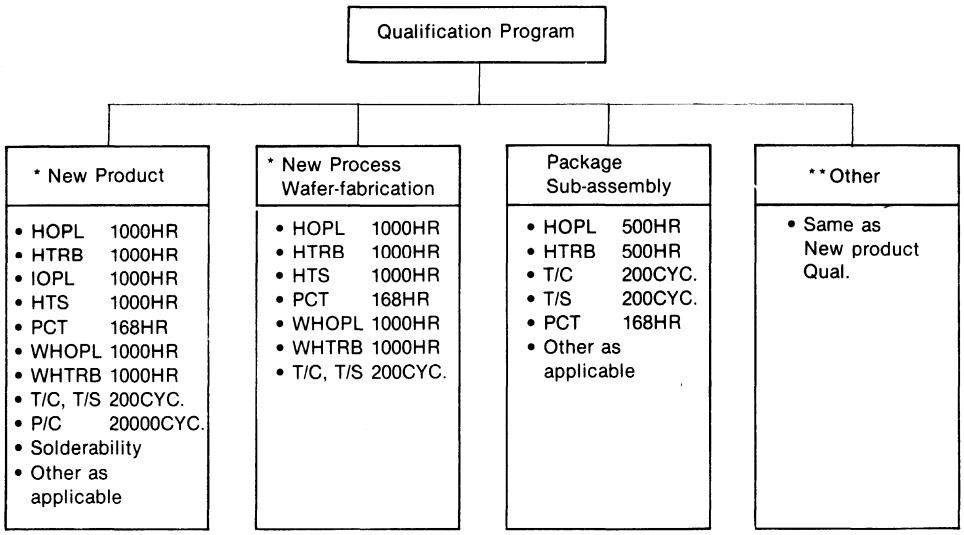


Quality Assurance During Development

2. QUALITY & RELIABILITY PROGRAM

2.1 QUALIFICATION

Procedures to qualify devices are listed below. There are both general and product-specific requirements. Procedures are detailed for new products, die-only qualifications, and package-only qualifications. The latter two are for products and/or packages already qualified, but there is room for further product optimization.



*Testing time for each test items depends on the grade (group) of devices. (see the device group list 2.1 2))

** Design, Equipment, Material(s), etc....

1) PROCESS DEVELOPMENT QUALIFICATION

Purpose: To investigate the change of a process parameter and then apply it to a production process by the reliability testing of a process which has been newly developed.

New Process, Wafer Fabrication Qualification

No	Test Item	Test Condition	Package	
			L-IC	Discrete
1	High Temperature Operating Life (HOPL)	$T_a = T_{opr}$(max) $V_{CC} = V_{CC}$(max) STATIC, DYNAMIC 1000HRS	YES	—
2	High Temperature Reverse Bias (HTRB)	$T_a = T_j$(max) $V_{CB} = 0.8 \times V_{CBO}$ 1000HRS	—	YES
3	High Temperature Storage (HTS)	$T_a = T_j$(max) 1000HRS	YES	YES
4	Pressure Cooker Test (PCT)	$T_a = 121°C \pm 2°C$ RH = 100% 15 PSIG 168HRS	YES	YES
5	Wet High Temperature Operating Life (WHOPL)	$T_a = 85°C$, RH = 85% $V_{CC} = V_{CC}$(min) 1000HRS	YES	—
6	Wet High Temperature Reverse Bias (WHTRB)	$T_a = 85°C$, RH = 85% $V_{CB} = 0.8 \times V_{CBO}$ 1000HRS	—	YES
7	Thermal Shock (T/S)	$-65°C \rightleftarrows 150°C$ (Liquid) 5min, <10sec, 5min 200 cycles	YES	YES
8	Temperature Cycle (T/C)	$-65°C \rightleftarrows 150°C$ (Air) 10min, 10min 200 Cycles	YES	YES

When the results of a reliability test are good, the process characteristics good, and the yield level is satisfied, the process can be applied to production. If there are any problems found in a process after it has been applied to production, the problem will be investigated in detail and the process will be revised. Once the process has been revised and approved, it will again be applied to production.

2) PRODUCT DEVELOPMENT QUALIFICATION

Purpose: To develop a stable and uniform product that satisfies the customer's requirements for quality by using exact reliability test specification called for by the new product.

Products are grouped according to the importance of their application.

Group 1	Group 2	Group 3
1. A/D, D/A Converter 2. IC for LCD 3. IC for PC 4. ASIC Master 5. Codec 6. MPR 7. IC for Exchange 8. New Products	1. Transistor 2. Regulator/OP AMP 3. IC for Telephone 4. Comparator/Timer 5. MICOM 6. Audio/Video IC 7. General Mos IC	1. ASIC Opinion Product 2. Toy/Melody IC 3. MICOM family 4. Products Except Group 1, Group 2 Products

New Product Qualification Test Items

No.	Test Item	Test Condition	Part		Reference Method	Note
			L-IC	Discrete		
1	High Temperature Reverse Bias (HTRB)	Ta = T_j(max) $V_{CB} = 0.8 \times V_{CBO}$ 1000HRS	—	YES		
2	High Temperature Operating Life (HOPL)	Ta = T_{opr}(max) $V_{CC} = V_{CC}$(max) Static, Dynamic 1000HRS	YES	—	MIL-STD-883 1005	
3	High Temperature Storage (HTS)	Ta = T_{stg}(max) 1000HRS	YES	YES		
4	Operating Life (OPL)	Ta = 25°C $P_C = P_C$(max) 1000HRS	—	YES	MIL-STD-750 1026.3	For Small-Signal Device
5	Intermittent OPL (IOPL)	Ta = 25°C $P_C = P_C$(max) 2min/2min On/Off 1000HRS	—	YES	MIL-STD-750 1036.3	
6	Power Cycle (P/C)	ΔT_j = 125°C 120Sec/120Sec On/Off 10000CYC.	YES	YES		For PWR TR, PWR IC
7	Pressure Cooker Test (PCT)	Ta = 121°C ± 2°C RH = 100% 15PSIG 168HRS	YES	YES		
8	Wet High Temperature Reverse Bias (WHTRB)	Ta = 85°C, RH = 85% $V_{CB} = 0.8 \times V_{CBO}$ 1000HRS	—	YES		
9	Wet High Temperature Operating Life (WHOPL)	Ta = 85°C, RH = 85% $V_{CC} = V_{CC}$(min) Pdmin 1000HRS	YES	—		
10	Thermal Shock (T/S) (Liquid)	−65°C↔150°C 5min, <10Sec, 5min 200 Cycles	YES	YES	MIL-STD-883 1011	
11	Temperature Cycle (T/C) (Air)	−65°C↔150°C 10min, 10min 200 Cycles	YES	YES	MIL-STD-883 1011	
12	Solder Heat Resistance (S/H)	Ta = 260°C ± 5°C t = 10 ± 2Sec	YES	YES	MIL-STD-750 2031.1	
13	Solderability	Ta = 245°C ± 5°C t = 5 ± 0.5sec Reject is >10% uncovered surface	YES	YES	MIL-STD-883 2003	
14	Salt Atmosphere	Ta = 35°C, 5% NaCl 24HRS	YES	YES	MIL-STD-883 1009A	

New Products Qualification Test Item (Continued)

No.	Test Item	Test Condition	Part		Reference Method	Note
			L-IC	Discrete		
15	Mechanical Shock	1500G, 0.5ms 3 Times Each direction of X, Y and Z Axis	YES	YES	MIL-STD-750 2016	For Hermetic
16	Vibration	20G, 3 Axis f = 20 to 2000 cps for 4 min, 4 cycles	YES	YES	MIL-STD-883 2007	For Hermetic
17	Constant Acceleration	2000G X,Y,Z Axis 1min for each Axis	YES	YES	MIL-STD-883 2001	For Hermetic
18	ESD (Human Body Model)	R = 1.5kΩ C = 100pF 5 Discharge V ≥ ± 1000V	YES	YES	MIL-STD-883 3015	
19	Latch-up Test		YES	—	—	For CMOS
20	Fine Leak Gross Leak	Helium Fluoro Carbon	YES	YES	MIL-STD-883 1014	For Hermetic

Note) • SOT-23, TO-92S PKG: PCT-48HR

3) PACKAGE DEVELOPMENT QUALIFICATION

Purpose: Whenever a new package type is developed, it must meet the specifications for devices that have been qualified and have maintained certain specified quality levels before the new package type may be applied to production.

Flow	Contents	Remarks
	Beginning of PKG development	Select representative device for product group (proceed at least 2 lots)
	Ass'y Qual	• Push Test • Die Thick • Bond Pull • Lead Torque • MPT • Dimension • X-Ray • Solderability
	Reliability Qual	• HTRB (TR) • HOPL (IC) • T/C • PCT • LTS • S/H • Vibration • M/S • Const
	Approvement of Qual	• New PKG Development will be approved when Rel qual is good for 500HR.

Package Sub-Assembly Qualification Test Items

No.	Test Item	Test Condition	Package		Notes
			Plastic	Hermetic	
1	High Temperature Reverse Bias (HTRB)	Ta = T_j(max) $V_{CB} = 0.8 \times V_{CBO}$ 500HRS	YES	YES	For Discrete
2	High Temperature Operating Life (HOPL)	Ta = T_{opr}(max) $V_{CC} = V_{CC}$(max) Static, Dynamic, 500HRS	YES	YES	For IC
3	Temperature Cycle (T/C)	−65°C⇌25°C⇌150°C 10min, 5min, 10min 200 CYCLES	YES	YES	
4	Pressure Cooker Test (PCT)	Ta = 121°C ± 2°C RH = 100%, 15PSIG 168HRS	YES	—	
5	Thermal Shock (T/S)	−65°C⇌150°C (Liquid) 5min, < 10sec, 5min 200 CYCLES	YES	YES	
6	Solder Heat Resistance (S/H)	260°C ± 5°C 10 ± 1 sec Once without Flux	YES	YES	
7	Vibration (Variable-Frequency)	100 ~ 2000 ~ 100Hz 20G, 5min, 5Times, X, Y, Z	—	YES	For Discrete, others as applicable
8	Mechanical Shock (M/S)	1500G, 0.5ms 3 Times, X, Y, Z	—	YES	same as above
9	Constant Acceleration	20000G X, Y, Z Axis 1 min for each Axis	—	YES	same as above

4) CHANGE QUALIFICATIONS:

Purpose: To apply changes to production processes and designs by evaluating the quality levels for those processes and designs of devices in production.

Classification		Change
Design		Change of more than 1EA MASK for the product in production.
Process	Ass'y	• D/A • Coating • W/B • Mold
	Diffusion	• Diffusion/Photo/Etch, etc. • Metalization • Passivation

Procedure: Issuance of EIN for the change → Review of initial characteristics → Reliability test → Issuance of ECN (register of specification) → Application for production. Evaluation level: LTPD 10% (1/2)

2.2 MONITOR PROGRAM

1) ON GOING PROCESS CONTROL

All parameters of each process are controlled by SPC (Statistical Process Control). All resultant SPC data are gathered by computers are recorded automatically. Trends of each parameter are plotted on control charts by the computer and corrective actions are immediately taken whenever a parameter goes "out-of-control", beyond the control limits.
Whenever a parameter goes "out-of-control" in a process, engineers involved with that particular process have meetings to decide the disposition of those lots that were effected by the out-of-control process and corrective actions are implemented. In the case of critical defects, all lots are scrapped by the MRB (Material Review Board).
As the key item of ongoing process control, the Cp or Cpk value is controlled by computer for each process. the UCL and LCL for each process is then determined by the computer generated Cp or Cpk value. Cp or Cpk values are continually upgraded to insure the stabilization of the process, and a QIP (quality improvement plan) is made out to drive defects down to zero.
Process capabilities of each process are totaled and analyzed and those results are reflected on the QIP. The stabilization and maximization of process capabilities are driven by SPC.

2) PRODUCT RELIABILITY MONITOR

The reliability monitor program begins where the qualification program ends, at the start-up of limited production. Everything that is subject to qualification is considered subject to the monitor program. Generally, the products to be used for reliability monitors are gathered from each fab lot each month, where the product selected is representative of:

1) each fab process technology
2) each generic product type
3) each package technology
4) each subassembly plant

The products are shipped directly to the appropriate Q & R group, which puts the products through a series of electrical, mechanical, thermal, and environmental tests that usually are identical to those used initially for qualifying the product. Most tests are of short duration, but some may extend out to thousands of hours. Each month the test results are evaluated and problems, should they exist, identified.
Each monitor failure is analyzed. If a problem is detected where the failure rate is greater than that considered acceptable, or a reliability problem is suspected, a Material Review Board (MRB) is called. This meeting is attended by appropriate Q & R personnel, scheduling personnel, engineering personnel, and any other affected groups.
This group reviews the data, decides on the disposition of the affected material, decides on appropriate corrective action, and basically controls the problem or issue until it is satisfactorily resolved.

3) FINAL QUALITY ASSURANCE PROGRAM

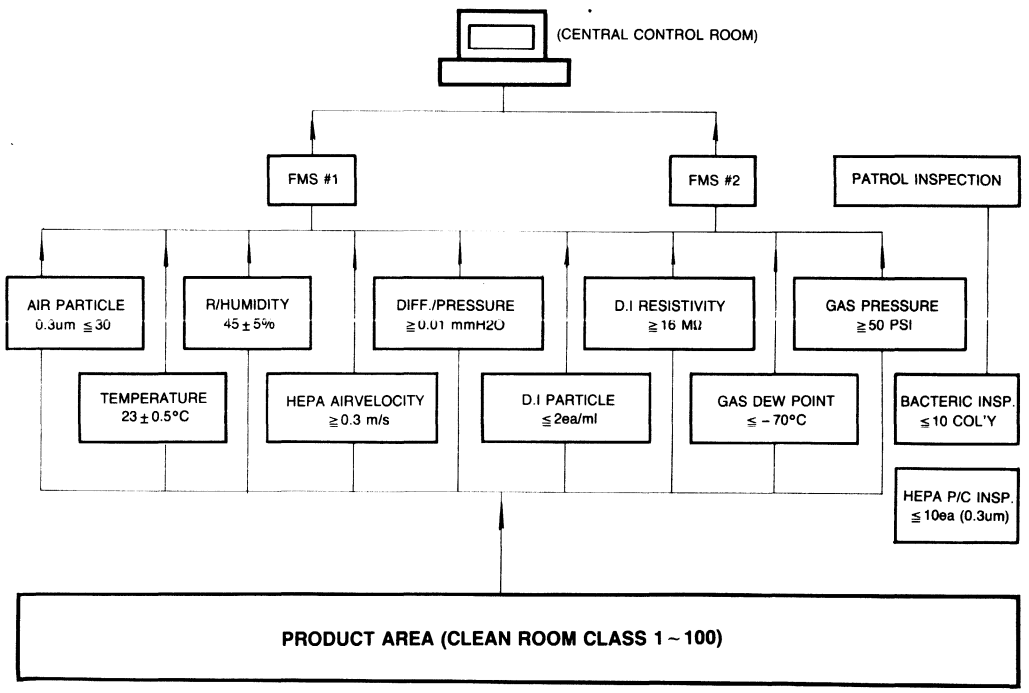
After the completion of the entire manufacturing process, a sample of each lot is pulled and the data sheet verification test is repeated. This final verification objective is to ensure that test system to test system variations are not compromising the quality, and that inadvertent system or handling problems have not occurred.

4) ENVIRONMENT MONITOR

- **Instruments**

- F.M.S #1 (HIAC/ROYCO System 1 Set)
- F.M.S #2 (P.M.S System 1 Set)
- Control Particle Monitoring System (2 Set) — On line monitoring system (Central control room)
- Portable Particle Counter, Sensors

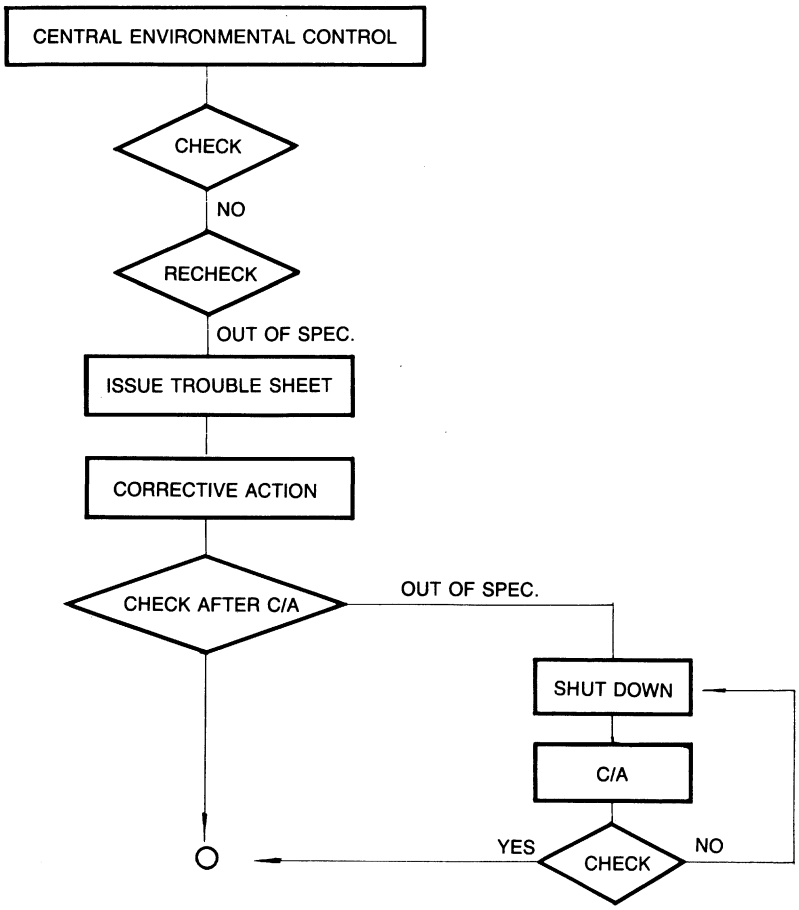
- **Block Diagram**



• **Environment Monitor**

Item	Frequency
1. Particle (Air, D-I Water)	5 min
2. Temperature, Relative Humidity	5 min
3. D.I Resistivity	5 min
4. Differential Pressure	5 min
5. HEPA Air Velocity	5 min
6. Gas (H_2, O_2, N_2, Air) Dew Point	5 min
7. Gas Pressure	5 min
8. HEPA Filter Particle	All HEPAs/1 room/Day
9. D-I Bacteria Main Lot	Weekly
10. D-I Bacteria Using Lot	Monthly

Corrective Action Requirement



2.3 QUALITY CONFORMANCE PROGRAM

1) DESCRIPTION

SEC has established a comprehensive reliability program to monitor and ensure the ongoing reliability of its Linear IC family. This program involves not only reliability data collection and analysis on existing parts, but also rigorous in-line quality controls for all products.
Listed below are details of tests performed to ensure that manufactured product continues to meet SEC's stringent quality standards. On-line quality controls are reviewed extensively in later sections.
The tests run by the quality department are accelerated tests, serving to model "real world" applications through boosted temperature, voltage and/or humidities. Accelerated conditions are used to derive device knowledge through means quicker than that of typical application situations. These accelerated conditions are then used to assess differing failure rate mechanisms that correlate directly with ambient conditions. Following are summaries of various stresses (and their conditions) run by SEC on Linear IC products.

2) HIGH TEMPERATURE OPERATING LIFE TEST (HOPL)

($T_j = 125°C$, $V_{CC} = V_{CC}$ max, static)

The high temperature operating life test is performed to measure actual field reliability. Life tests of 1000HR to 2000HR durations are used to accelerate failure mechanisms by operating the device at an elevated ambient temperature (125°C). Data obtained from this test are used to predict product infant mortality, early life, and random failure rates. Data are translated to standard operating temperatures via failure analysis to determine the activation energy of each of the observed failures, using the Arrhenius relationship as previously discussed.

3) WET HIGH TEMPERATURE OPERATING LIFE TEST (WHOPL)

(Ta = 85°C, R.H. = 85%, $V_{CC} = V_{CC}$ opt, static)

The wet high temperature operating life test is performed to evaluate the moisture resistance characteristics of plastic encapsulated components. Long time testing is performed under static bias conditions at 85°C/85 percent relative humidity with nominal voltages. To maximize metal corrosion, the biasing configuration utilizes low power levels.

4) INTERMITTENT OPERATING LIFE (IOPL)

(Pmax, 25°C, 2min on/2 min off)

This test is normally applied to scrutinize die bond thermal fatigue. A stressed device undergoes an "ON" cycle, where there is thermal heating due to power dissipation, and an "OFF " cycle, where there is thermal cooling due to lack of inputted power. Die attach (between die and package) and bond attach (between wire and die) are the critical areas of concern.

5) HIGH TEMPERATURE STORAGE TEST (HTS)

(Ta = 125°C, UNBIASED)

High temperature storage is a test in which devices are subjected to elevated temperatures with no applied bias. The test is used to detect mechanical instabilities such as bond integrity and process wearout mechanisms.

6) PRESSURE COOKER TEST (PCT)

(121°C, 15PSIG, 100% R.H., UNBIASED)

The pressure cooker test checks for resistance to moisture penetration. A highly pressurized vessel is used to force water (thereby promoting corrosion) into packaged devices located within the vessel.

7) TEMPERATURE CYCLING (T/C)

(−65°C to +150°C, AIR, UNBIASED)

This stress test uses a chamber with alternating temperatures of −65°C and +150°C (air ambient) to thermally cycle devices within it. No bias is applied. The cycling checks for mechanical integrity of the packaged device, in particular bond wires and die attach, along with metal/polysilicon microcracks.

8) THERMAL SHOCK (T/S)

(−65°C to +150°C, LIQUID, UNBIASED)

This stress test uses a chamber with alternating temperatures of −65°C to +150°C (liquid ambient) to thermally cycle devices within it. No bias is applied. The cycling is very rapid, and primarily checks for die/package compatibility.

9) RESISTANCE TO SOLDER HEAT

(UNBIASED, 260°C, 10 sec)

Solder Heat Resistance is performed to establish that devices can withstand the thermal effects of solder dip, soldering iron, or solder wave operations.

10) MECHANICAL SHOCK

(UNBIASED, 1500g, Pulse = 0.5msec)

This test determines the suitability of a device to be used in equipment where mechanical "shocks" may occur. Such shocks result from sudden or abrupt changes produced by rough (non-standard) handling, transportation, or field operations.

11) VARIABLE FREQUENCY VIBRATION

(UNBIASED, Range = 100 to 2000Hz)

Variable Frequency Vibration is done to model the effects of differential vibration in the specified range. Die attach and bonding integrity are particularly stressed, testing the mechanical soundness of device packaging.

12) CONSTANT ACCELERATION

(UNBIASED, 10kg to 20kg)

This is an accelerated test designed to indicate types or modes of structural and mechanical weaknesses not necessarily detectable in Mechanical Shock and Variable Frequency Vibration stressing.

13) RELATIVE STRESS COMPARISONS

Many stress tests are run at SEC on many different devices. Through both theoretical and actual results, it can clearly determined which tests are most effective. It can also establish which tests were not fully effective.

Comparisons have been made on the basis of defects able to be determined, efficiency in detection, and cost. For the reader's benefit, SEC provides the results and its conclusions on the following pages.

3. CUSTOMER SUPPORT SYSTEM

3.1 INTRODUCTION

Manufacturing companies have developed customer support systems for the purpose of uniting communications. Through these communications pass the information and knowledge required to satisfy the customers needs in areas such as quality and reliability, customer claims, customer training, field service technical issues, pricing or availability and above all, trust. Open lines of communication establishes thorough trust between the customer and vendor and are essential for such programs as dock-to-stock in order to achieve the ultimate in customer/vendor relations. SEC, in its commitment to customer satisfaction, has installed within its organization a support system that is designed to produce the open lines of communication between the customer and SEC in all facets of relations.

3.2 POLICY

SEC has developed within its organization, a customer support system. SEC's policy requires that this system be manned with the proper personnel that are thoroughly trained in the areas that each represent and are dedicated to opening and maintaining lines of communication with the customer. Technical data used by SEC to support the customer must be up to date and always available for use by the customer (privileged or confidential information maybe excluded). Customer training is provided to the customer by only the most knowledgeable SEC personnel. SEC will provide customer field service in the form of periodic goodwill visits to customer sites or specialized problem solving services as required. Process change notification procedures as well as safety standards are also strictly adhered to.

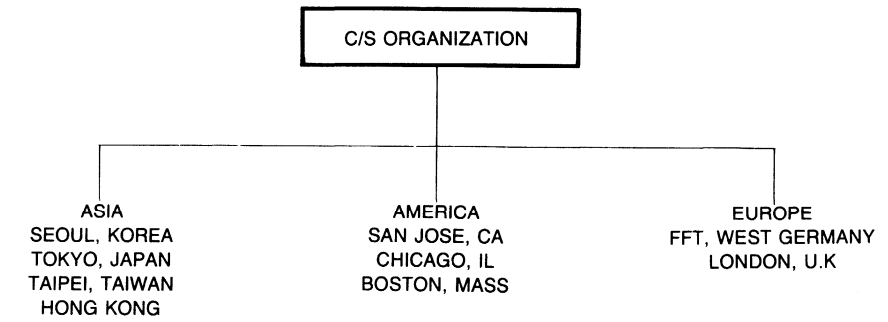
3.3 CUSTOMER SUPPORT SYSTEM

1) QUALITY ASSURANCE SERVICE

SEC has felt the need to reorganize its current Quality Assurance Sections in order to better service our customers. From this new organizational change, a new QA section was born. This new QA section, known as QA Section 3, was developed specifically for the customer. The customer service team in QA3, was organized to respond promptly to customers quality requirements. The purpose of this team is to form a more responsive communication channel between plant R & D, the sales department, and the customer. Customers should achieve satisfaction with our company's products by use of the newly organized customer service system. This service system is openly available to customers for comments concerning problems or opinions about SEC's devices. An 800 number is published on the inside of the handbooks' over.

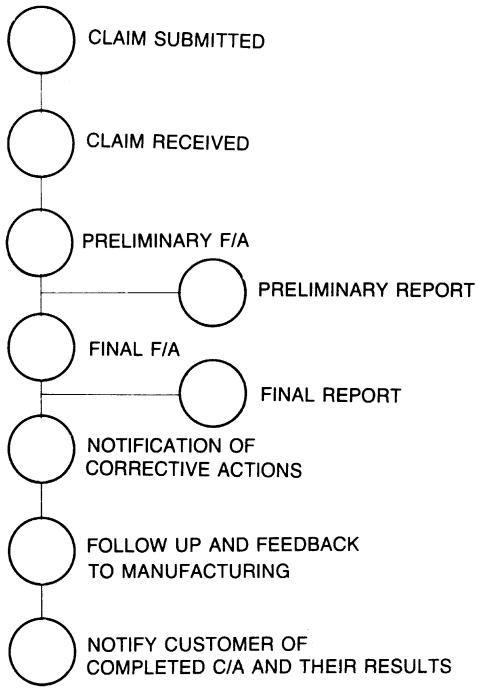
2) CUSTOMER SERVICE TEAM

The following organizational chart illustrates the world-wide base that the customer service team of SEC has established. Maintaining continuity between all of SEC's worldwide customer service teams is accomplished through the use of a newly installed computer network which allows constant communication between all teams.



3) CUSTOMER CLAIM SUPPORT SYSTEM

Information from the field concerning quality is an essential factor in the improvement of product quality. Equally important, is the investigation of field failures. Timely feedback of the results from the analysis is required to better service customers properly. This data also serves as a direct guide to the improvement of reliability and quality for both SEC and our customers.
The flowchart below demonstrates the process in which SEC currently follows for customer claims.



4) CUSTOMER TRAINING SYSTEM

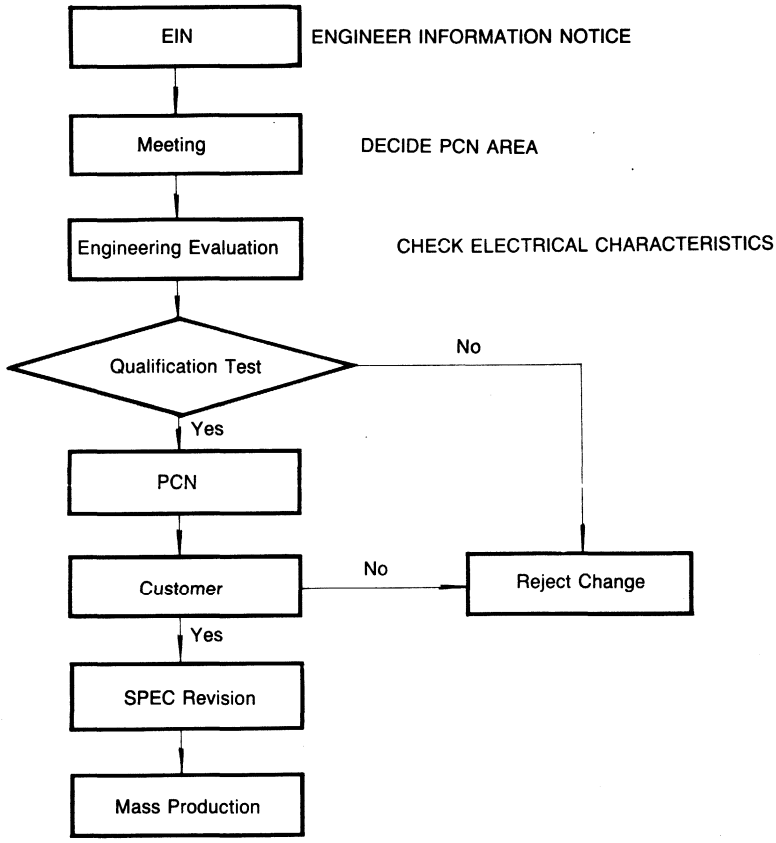
SEC has recently established a training team for the purpose of teaching SEC's customers the methods currently used by SEC to insure product quality and reliability at the customers site. SEC offers this training in the form of group seminars or presentations and, when requested or deemed necessary, individualized training is offered. In some cases, the training will take place at the customers site at the customers convenience while in other cases, SEC will extend an invitation to the customer to visit our manufacturing site.

5) CUSTOMER FIELD SERVICE

SEC has developed field service teams that are devoted to making customer contact even when there are not any problems. In other words, SEC is interested in making periodic goodwill visits. The visiting team would be comprised of those managers and engineers that are involved with the product types that the customer currently uses. The main goal of this team is to establish customer trust through communication.

3.4 PROCESS CHANGE NOTIFICATION SYSTEM (PCN)

Changes in process are sometimes required to produce a higher quality product at a lower price. Thexe changes can include new or different types of material, new or modified designs 2 and new or different processes. SEC has developed a PCN procedure that is followed whenever a major or critical change is to be considered for any process. The idea behind the PCN is to allow change to a process by submitting the planned change for qualification by SEC engineering personnel and then presenting the PCN to the customer for final approval. By following this procedure, the customer is assured that no major or critical change will occur to the process without the customers consent.



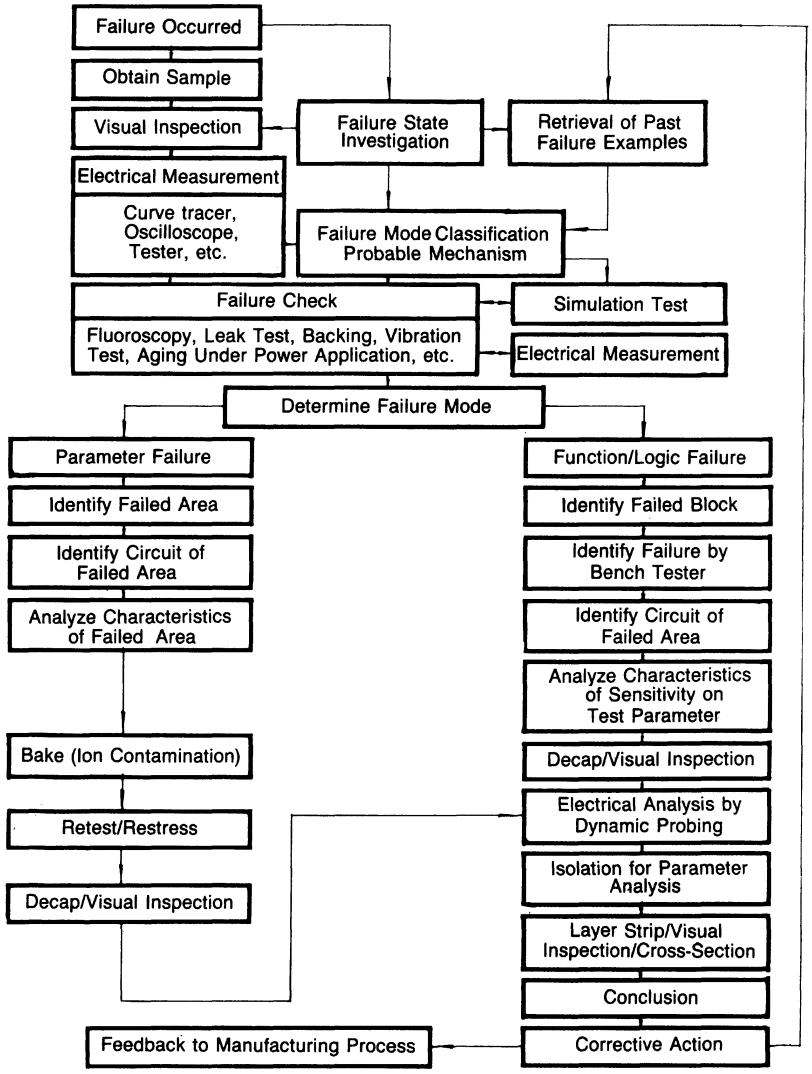
3.5 SAFETY STANDARDS

Most customers express the desire to use only products which have been manufactured with materials that meet the safety specifications of the Underwriters Laboratories. SEC has chosen to adhere to the specifications called out in the UL standard 94 by purchasing and using only those plastic materials that conform to this standard. UL 94 tests for a number of different flammability conditions that effect the plastic material used in semiconductor devices, including horizontal burning, vertical burning and flame spread.

4. FAILURE ANALYSIS

4.1 PROCEDURE

A general failure analysis procedure is shown below. The method demonstrated in the flow chart applies to all rejects. However, each analysis is specific unto itself, so that a completely exhaustive analytical flow is impossible to show in the limited space of this manual. Specific instances and examples of interest are provided later in the chapter. Also included in this section is a typical day-by-day accounting of a failure analysis in progress. A two-week turnaround is the objective, with greater than 90% of analysis lasting equal to or less than this duration. A sample analysis plan and report are attached at the conclusion of this section.



Failure Analysis Procedure Flow Chart

Applicable Comments for the above flow chart are made below.

1) DETERMINATION OF FAILURE MODE

The basic failure mode shall be determined with data from computer and bench testing. As a defect can represent various electrical failure modes, it is critical to determine the most basic failure mode. (For example, a V_{OL}/V_{OH} parameter failure may be also analyzed as a functional failure. However, it is very important to determine V_{OL}/V_{OH} as the basic failure mode.)

2) IDENTIFICATION AND ANALYSIS OF FAILED CIRCUIT AREA

Correlation shall be derived with general (macroscopic) failure phenomenon through circuit interpretation of the failed area.

3) SENSITIVITY OF TEST

Parametric value of a failed sample shall be determined by adjusting DC and AC parameters, temperature range, etc.

4) ION CONTAMINATION

For a sample assumed to have an inversion phenomenon caused by ionic contamination, characteristics shall be identified by conducting a Ta = 150°C, 24 hour cure and, repeating test/restress.
Contamination of a specific layer shall be determined by stripping each layer.

5) DECAPSULATION

There are 5 decap methods with respective merits and demerits. The appropriate method must be utilized on the basis of the characteristics and potential cause for each failure.

6) ISOLATION AND DYNAMIC PROBING

It is essential to isolate the probable failing part of the circuit for its electrical failure mode. Without isolation, exact detection of a failed part can not be accurately accomplished as an electrical failure mode has an influence on other parts of the circuit.

7) LAYER STRIPPING

Each layer strip should meet specification requirements with respect to time. It should never be the case that chemical attack is mistaken for causing the failure of a part.

8) GENERATION OF ACTIVATION ENERGY

Accelerated life testing requires generation of actual activation energies based upon establishing a definitive failure mode. This generation has a great effect in determining the acceleration factor of an Arrehenius' model.

9) CORRECTIVE ACTION

Failure analysis is fully completed only by establishing a future plan and corrective action, which are taken to resolve a problem and prevent its recurrence.

4.2 Failure Modes and Mechanisms

1) Failure mechanisms for devices vary widely. They are caused by both front-end (wafer) and back-end (assembly) processing. To classify problems and their instigations, the table listed below is provided.

Items and Causes of Failure Modes

Item	Type of Failure	Failure Mode	Cause
Wire Bonding	Wire Disconnection	Open	Incomplete Manufacture or Misuse
	Wire Short	Short	
	Purple Plague	Open, High Resistance	
	Bond Detaching	Open, High Resistance	
	Misplaced Bonding, Loose Contact	Open, High Resistance Short	
	Improper Bond Shape Erroneous Bonding	Open, High Resistance Open, High Resistance	Incomplete Manufacture
Junction Region	Destruction by Surge	Low Breakdown Voltage, Short, Open	Incomplete Manufacture or Misuse
	Hot Spot		
Case	Lead Disconnection	Open, High Resistance	Same as above
	Lead Short	Short, High Leakage	
Seal	Incomplete Seal	Breakdown Voltage Deterioration, High Leakage	Same as above
	Enclosed High Humidity Gas		
	Contamination of Surface		
	Dust and Dirt	Short, Low Breakdown Voltage Large Leakage	
Metallization	High Current Density	Open, Short	Misuse
	Electromigration	Open, High Resistance	
	Scratch	Open, Short	Incomplete Manufacture
	Insufficient Thickness Excessive Etching	Open, High Resistance	
	Contamination, Dust and Dirt	Open, High Resistance	Incomplete Manufacture or Misuse
	Poor Wiring and Element Connection		
Chip Mounting	Chip Crack	Open, Short	Same as above
	Chip Detaching	Open, Short, High Thermal Resistance	
Oxidized Film	Pinhole, Crack	Low Breakdown Voltage, Short	Incomplete Manufacture
	Insufficiently Oxidized Film Thickness	Low Breakdown Voltage	
Surface Treatment	Channel Formation	Low Breakdown Voltage High Leakage	Same as above
	Contamination		
Mask	Insufficient Photoresist	Low Breakdown Voltage Short, Open, High Leakage	Same as above
	Mask Misalignment		
Material and Diffusion	Improper Impurity Density	Same as above	Same as above

2) Standard product reliability tests can naturally generate failures. Here, in this section, a table is given which lists tests and their associated rejects. Each test has a specific purpose, and if there exists a particular product weakness, a given test will expose it. In this manner, by knowing a test and it's function, a clear determination can be made as to the relevance of a failure for that particular test.

Reliability Tests and Associated Failure Modes

	Failure Cause	Diffusion	Oxide	Metalization	Wire Bonding	Package Environment	Package Seal	Lead Fatigue	Solderablity	Mark	Die bonding
Item	Test Condition	•Contamination •Crystal Defect •Photoresist Reject	•Contamination •Pin Hole •Crack •Thickness Unstable	•Conpos. •Scratch •Void •Open	•Interface •Corrosion •Misbonding •Wire Open •Chemical Interface	•Conductive ions •Inadequate •Environments	•Sealing Reject	•Conpos.	•Marking	•Themal Reject	Resistance Reject •Crack •Chip Position Reject
T/C	-65°C→150°C 200 Cycles		0	0	0		0				0
T/S	-65°C→125°C 200 Cycles		0	0	0		0				0
Moisture Resistance	90-98%R.H./65°C3HRS 80-98%R.H./25°C8HRS 90-98%R.H./65°C3HRS 10 Cycles		0	0	0	0	0				
Vibration Fatigue	20G-3 Axis Orientation f=20 to 2000 cpe for 4 min. 4 cycles				0	0					0
Constant Acceleration	Pulse Duration: 0.1-1m sec Shock pulse: 0.5-3Kg				0						0
Mechanical Shock	1500g, 0.5ns Each Direction of X, Y and Z Axis				0						0
Lead Integrity	W=227g 90°C 3 times						0				
Marking	Isoprophylalcohol									0	
Solderability	Ta=230° 5 Sec. Once With Flux								0		
Salt Spray	Ta=35°C, 5% NaCl				0				0		
OPL	Individual Spec	0	0	0	0	0					0
IOPL	Individual Spec	0	0	0	0	0					0
HTRB	Individual Spec	0	0	0	0	0					0
HTS	Individual Spec		0		0	0			0		
WHTS	80°C, 90% RH 85°C, 85% RH		0	0			0	0	0		
WHTRB	85°C, 85% RH Bias	0	0	0	0	0	0	0	0		0

3) An anomalous manufacturing step can manifest itself in many ways with respect to product reliability. The chart below depicts process steps, the types of rejects they can generate, and the way to defeat such failures. Of course, there are numerous QC and Production checks along all stages of the manufacturing process. However, a semiconductor product typically involves so many operations it's nearly impossible to detect all potential reliability hazards. Thus, there are final electrical and visual tests, reliability tests, and statistical analyses which are run prior to a product release. The chart below speaks to the electrical, visual, and reliability tests.

Failure Mechanisms of Integrated Circuits

Process Step Affecting Reliability	Failure Mechanism	Failure Mode	Failure Detection Method
Wafer Fabrication	Dislocation and Stacking Fault	Degradation of Function Characteristics	Electrical Test Operation Life
	Non-Uniform Resistivity	Unpredictable Characteristic Values	Electrical Test
	Surface Abnormalities	Improper Electrical Characteristics, Short and Open	Electrical Test Operation Test
	Cracks, Chips, Scratches (Usually Caused During Handling)	Open and Short	Electrical Test Visual Inspection (Before Seal) Temperature Cycling
	Contamination	Degradation of Junction Characteristics	Visual Inspection (Before Seal), Temperature Cycling, High Temperature Storage, Reverse Bias
Passivation	Cracks and Pin Holes	Shorts, Low Breakdown Voltage	Temperature Cycling High Temperature Storage High-Voltage Test, Operation Life Visual Inspection (Before Seal)
	Non-Uniformity of Film Thickness	Low Breakdown Voltage Increase of Leakage Current in Oxide Film	Same as Above
Mask	Scratch, Crack, Scar of Photo Mask	Open, Short	Visual Inspection (Before Seal), Electrical Test
	Misalignment	Open, Short	Same as Above
	Abnormality of Photo-Resist Pattern (Line-Width, Space, Pin Hole)	Degradation of Characteristics Due to Parameter Drift Open, Short	Same as Above
Etching	Improper Elimination of Oxide Film	Open, Short, Intermittent Failure	Visual Inspection (Before Seal) Electrical Test Operation Life
	Under-Cut	Short or Open in Metallization	Visual Inspection (Before Seal) Electrical Test

Failure Mechanisms of Integrated Circuits (Continued)

Process Step Affecting Reliability	Failure Mechanism	Failure Mode	Failure Detection Method
Etching	Spotting (Smear) Inhomogeneous Etching	Latent Short	Visual Inspection (Before Seal) Temperature Cycle, High Temperature Storage Operation Life
	Contamination (Photo Resist, Residue of Chemical Substance)	Low Breakdown Voltage Increase of Leak Current	Same as Above Reverse Bias
Diffusion	Improper Control of Doping Profile	Performance Degradation Caused by Instability and Fault	High Temperature Storage Temperature Cycling Operation Life Electrical Test
Metallization	Scratched and Smeared Metallization (Caused During Handling)	Open and Short	Visual Inspection (Before Seal) Temperature Cycling Operation Life
	Thin Metallization Due to Insufficient Deposition or Oxide Film Step	Open or High Impedance Internal Connection	Electrical Test Operation Life Temperature Cycle
	Oxid Film Contamination Material Incompatibility	Open Metallization Caused by Poor Adhesion	High Temperature Storage Temperature Cycling Operation Life Test
	Corrosion (Residue of Chemical Substance)	Open Metallization	Visual Inspection (Before Seal), High Temperature Storage Temperature Cycle, Operation Life
	Displacement Contaminated Contact	High Contact Resistance, Open	Visual Inspection (Before Seal), Electrical Test, High Temperature Storage Temperature Cycle, Operation Life
	Improper Temperature and Period for Metallization	Peeled Metallization Poor Adhesion Short	Electrical Test High Temperature Storage Temperature Cycle Operation Life
Die Separation	Cracks and Chips Caused by Improper Dicing	Open	Visual Inspection (Before Seal) Temperature Cycling Thermal Shock Vibration Shock

Failure Mechanisms of Integrated Circuits (Continued)

Process Step Affecting Reliability	Failure Mechanism	Failure Mode	Failure Detection Method
Die Bonding	Void Between Header and Die	Degradation Due to Overheating	Radiography, Operation Life Constant Acceleration Shock, Vibration
	Over-Spreading of Eutectic Solder	Short, Intermittent Short	Visual Inspection (Before Seal), Radiography, Vibration Shock
	Poor Bonding of Die to Header	Die Crack and Lifting	Visual Inspection (Before Sealing), Constant Acceleration, Shock, Vibration
	Mismatching of Materials	Crack or Peeling of Die	Temperature Cycling High Temperature Storage Constant Acceleration
Wire Bonding	Poor Bonding Strength	Open Wire, Open, Lifting Vibration Shock	Constant Acceleration
	Mismatched Material and Contaminated Bonding Pad	Lead Bond Peeling	Temperature Cycling High Temperature Storage Constant Acceleration Shock, Vibration
	Formation of Intermetallic Plague	Open Bonding	High temperature storage, Temperature Cycling. Constant Acceleration Shock, Vibration
	Insufficient Bonding Area or Spacing	Open Bonding Short	Operation Life Test, Constant Acceleration, Shock Vibration, Visual Inspection (Before Seal)
	Improper Bonding Arrangement	Open, Short	Visual Inspection (Before Seal) Electrical Test
	Die Cracks or Chips	Open, Shock	Visual Inspection (Before Seal) High Temperature Storage Temperature Cycling Constant Acceleration, Shock Vibration
	Excessive Loop or Sag in Wire	Short to the Case, Substrate or other Parts of the Leads	Visual Inspection (Before Seal), Radiography, Constant Acceleration, Vibration
	Crack, Scratch, or Scar on Lead	Wire Disconnection Causing Open, Short	Visual Inspection (Before Seal), Constant Acceleration, Shock Vibration

Failure Mechanisms of Integrated Circuits (Continued)

Process Step Affecting Reliability	Failure Mechanism	Failure Mode	Failure Detection Method
	Insufficent Elimination of Tail Wire	Short, Intermittent Short	Same as Above Radiography
Sealing	Incomplete Hermetic Seal	Performance Degradation, Shorts and Opens Caused by Chemical Corrosion and Moisture	Fine Leak, Gross Leak
	Bad Atmosphere in Package	Performance Degradation Due to Inversion Layer Channeling	Operation Life Reverse Bias, High Temp. Storage, Temperature Cycling
	Bending or Breaking of the External Lead	Open	Visual Inspection, Lead Fatique
	Crack or Void in Seal Glass	Short or Open in Metallization Due to Leak	Seal, Electrical Test High Temperature Storage Temperature Cycling High Voltage Test
	Migration on Seal between Outer Lead and Metal Case	Intermittent Short	Low Voltage Test
	Electro-Conducting Particles Floating in Package	Same as Above	Constant Acceleration, Vibration Radiography
	Mismarking	Inoperable	Electrical Test

4) Equipment

A listing of important equipment used for failure analysis is shown below in tabular from, SEC's committment to comprehensive analysis of all relevant rejects necessarily implies a usefulness for key analytical instruments. Constant efforts are made to both use and modify equipment to meet specialized investigations. However, only standard equipment, not a listing of hybrids (for confidential development purposes), are listed below

Equipment for failure analysis

Category	Item	Application
Visual	1. Stereo Microscope	Use for visual inspection
	2. SEM (Scanning Electron Microscope)	Used to inspect the surface or cross-section of a device at high magnification. Through voltage contrast techniques, it is possible to analyze voltage levels while the device is operating
	3. Infrared Microscope	Using the infrared radiation emitted by a functioning device, a thermal map can be produced.
	4. X-Ray	Used to inspect the bonding wire of encapsulated devices.
	5. Metallugical Microscope	Inspect interconnects, contacts, bonds
	6. Radiographic Scope	Inspect bond wires, die attach

Equipment for failure analysis (Continued)

Category	Item	Application
Elemental Analysis	1. Auger Electron Spectrometer (AES)	Used to detect and analyze contamination on the surface of a die
	2. EDX Spectrometer	Used with SEM to analyze elements present in a device. This is done by measuring the energy distribution of X-rays produced by the interaction of primary electrons and the sample.
	3. Differential Interference Microscope	Used for elemental analysis
	4. Electron Probe Micro Analyzer (EPMA)	Used for current analysis
	5. Ion Micro Mass Analyzer (IMMA)	Spectral analysis of chemical constituents
	6. Surface Eveness Micrometer	Measures planarity
	7. Differential Scanning Calorimeter (DSC)	Permits the analysis of glasses and polymers-especially encapsulation resins-through the measurement of reaction heat
	8. Thermo Gravimetric Analyser	Used to determine the thermal stability of polymers and glasses by measuring variations in mass with temperature.
	9. Plasma Etcher	Used to open devices encapsulated in epoxy resins, to remove silicon nitride, and to remove thin oxide films
	10. Transmission Electron Microscope (TEM)	Used for elemental analysis and high resolution surface on spectron
	11. Surface Tunneling Microscope (STM)	Used for elemental analysis
	12. Electron Spectrometry for Chemical Analysis (ESCA)	Used for elemental analysis
	13. Secondary Ion Mass Spectroscope	Used for elemental analysis
Decapsulation System	1. Grinding Machines 2. Angle Lapping 3. Evaporation 4. Diamond Cutter (Cross Section Cutter) 5. Molding System 6. Jet-Etching System 7. Etching Solution 8. Hot Plates 9. Ventilation Hoods	Used to decapsulate devices, to cut the cross section of die, to remove a surface layer.

Equipment for failure analysis (Continued)

Category	Item	Application
Electrical Test	1. Curve Tracer 2. TR, IC, MOS Tester 3. ESD Simulator 4. LCR Meter 5. DC-Analyzer 6. Noise Tester 7. Logic State Analyzer 8. Manipulator Probe Ssytem 9. Electron Beam Tester 10. Hot Electron Analyzer 11. I.R Scope	Used to measure electrical characteristic of devices, to establish the cause of failure.
Stress Test	1. Temperature Probe System 2. Constant Temperature Oven 3. Ovenn for Oper Life Test 4. Humidity Oven 5. Vibration System	Used to stress or cure the failed devices to identify a failure mechanism. This is a very important tool for analyzing degradation phenomena and intermittent failures.

Methods and Equipment for Failure Analysis

Item	Contents of Inspection	Equipment for Analysis
External Visual Check	• Condition of Lead, Plating, Soldering, Welding Area • Mark, Date Code • Package damage • Solderability • Sealing	Stereo-Optical-Scope x 40 Optical Microscope x 100 Helium Leak Detector Gross Leak Detector (Using Fluorocarbon)
Electrical Test	• DC Parameter, AC Parameter Test • Function Test • Margin Test of Voltage and Temp. • Diode Characteristics between Each Pin • Disconnection, Short Circuit and / or Electrical Characteristic detected by the above Inspection	IC Tester Curve Tracer (HP4145) Oscilloscope DC Power Supply Oscillator (Sine Wave Pulse) Heat-Gun, Cooling Gas Spray Thermo-Spot
Radiography	• Internal Structure of Device is Checked Non-Destructively	Soft X-Ray
Decapping	• Internal Structure is observed after decapping	Metal Cutting Scissors, Nippers Cap opener, plastic etcher, Hot plate, Drill, HNO_3
Internal Visual Check	• Detection of Defective Spot on the Chip Surface • Detection of Discrepancy of Internal Connection (Metallization, Wire Bond -ing, Etc.) • Electrical Characteristics are Checked by Mechanical Prober • Detection of Hot Spot • Existence of Foreign Material	Optical Microscope Micro-Prober SEM Laser Cutter Infrared Micro Scanner Thermal Plotter Infrared Microscope
Internal Structure Analysis	• Cross Sectional Analysis of Chips to Observe Diffusion Layer of Oxide Film • Analysis of Metallic Elements • Removing of Over-Coating Glass and Aluminum Metallization	Optical Microscope SEM, MAX, AES, SAM, IMA Spectrometer Micro-Prober
Simulation Test	• Operational Test on Actual Equipment	Actual Electronic Equipment

4.3 FAILURE MODE EFFECT ANALYSIS (FMEA)

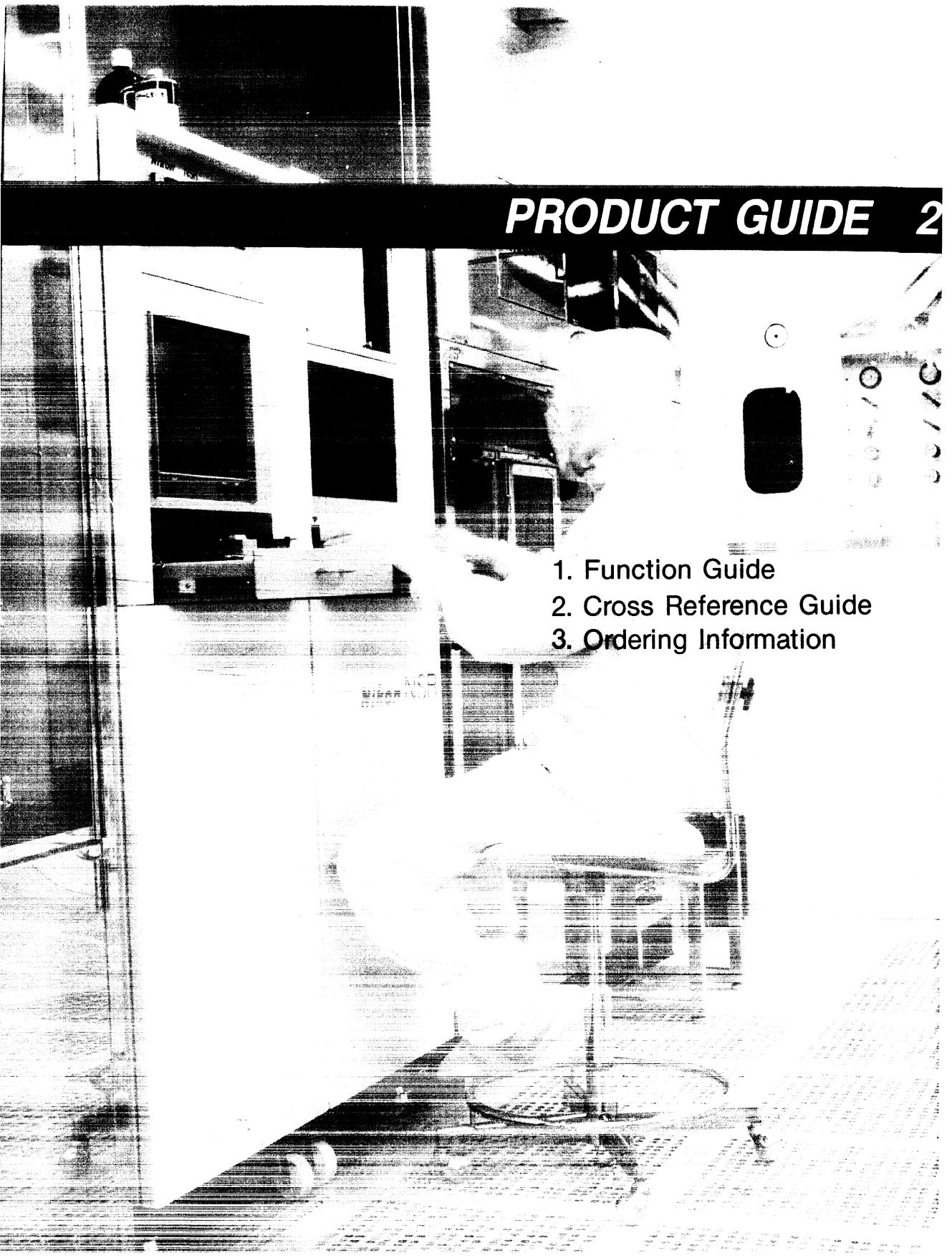
Failure Mode Effect Analysis is a method used for checking if measures are taken against every possible failure in the design, the manufacturing process, the operating method, etc. For this analysis, factors such as design, manufacturing process, packaging, and operating method are divided into small units, and its functions are clearly defined. All possible failure modes are listed for each item, its effect on the product and the cause of each failure is examined. Each item is then evaluated to clarify the corrective action to be taken.
The table below shows an example of FMEA in the manufacturing process of plastic encapsulated MOS LSI. The incident column pertaining to the Evaluation Points show the failure rate; the Effectiveness column shows the impact of the failure of the product, device, or system; and Detectability shows the rate of detection of the failure. These are individually graded on the basis of ten points. The result is then evaluated by multiplying the points. The larger value indicates the importance of the item. A counterplan for each item is then specified and action taken.

Manufacturing Process FMEA Example (Plastic Encapsulated Products)

Process Name (Process Function)	Failure Mode	Failure Effect	Failure Cause	Counterplan
Al metallization	Improper thickness Lack of Al wiring Breakage defect	Electromigration open circuit	Operator's mis-handling, dirt/foreign matter attachment, poor adjustment of equipment	Improvement and adjustment of written working process, dust control of clean room, SEM test in the process
Glassivation	Lack of glassivation film, failure film thickness	Increased leak current, improper operation	Dirt/foreign matter attachment, operator's mishandling	Dust control of clean room, improvement and adjustment of written working process
Visual Inspection	Scratch, die crack, dirt, spot, residual resist	Open circuit, increased junction leak current	Mishandling of wafer, Misclearning of water	Improvement and adjustment of written working process
Assembly Process Die Selection	Die crack	Increased junction leak current, improper operation	Poor adjustment of equipment, operator's mishandling	Corrective action to device control operator, improvement and adjustment of written working process
Die Bonding	Die crack Die floating	Open circuit, increased junction leak current, improper operation	Operator's mishandling temperature too low	Corrective action to device control operator, improvement and adjustment of written working process, visual inspection
Wire Bonding	Open bonding, improper bonding position, shorted bonding wire	Open circuit, short circuit	Poor bonding strength, operator's mishandling, poor adjustment of equipment, looped bonding wire, shape defact	Improvement and adjustment of written working process, corrective action to device control operator, visual inspection

Manufacturing Process FMEA Example (Plastic Encapsulated Products) (Continued)

Process Name (Process Function)	Failure Mode	Failure Effect	Failure Cause	Counterplan
Sealing (Resin)	Open bonding wire, shorted bonding wire, package crack, corrosion	Open circuit, short circuit, defective appearance	Poor adjustment of equipment, insufficient cure	Ditto
Lead Surface Treatment (plating)	Poor metal-plating thickness, dirt	Poor soldering, poor contact	Operator's mishandling poor adjustment of equipment, insufficient cleaning	Adjustment of written working process, corrective action to control operator
Lead Formation	Abnormal shape, broken lead	Failure inserting in the printed substrate poor operation	Operator's mishandling poor adjustment of equipment	Ditto
Marking	Marking error illegible marking	Operating destruction	Operator's mishandling insufficient cure	Improvement and adjustment of written working process



PRODUCT GUIDE 2

1. Function Guide
2. Cross Reference Guide
3. Ordering Information

1. AUDIO APPLICATION

A. FM Front End

Type	Package	Function			Use			Remark
		RF	OSC	MIXER	R/C	Car	HI-FI	
KA22495/D	9 SIP/8 SOP	*	*	*	*		*	V_{CC} = 1.6 ~ 6V

B. FM/AM RF, IF and Detector System, AM Tuner System

Type	Package	Function						Use			Remark
		AM RF CONV	AM IF AMP	AM DET	FM IF AMP	FM DET	S/M	R/C	Car	HI-FI	
KA2243	16 DIP		*	*	*	*	*	*		*	V_{CC} = 3 ~ 14V
KA2244	9 SIP				*	*	*		*		V_{CC} = 8 ~ 16V
KA22441	16 ZSIP				*	*	*		*		V_{CC} = 6 ~ 14V
KA2245	7 SIP				*	*			*		V_{CC} = 8 ~ 15V
KA2247	16 DIP	*	*	*	*	*	*	*			V_{CC} = 3 ~ 8V
KA22471	16 DIP	*	*	*	*	*	*	*			V_{CC} = 3 ~ 8V
KA2248A/D	16 DIP/16 SOP	*	*	*	*	*	*	*			V_{CC} = 1.8 ~ 6V

C. FM Stereo Multiplex Decoder

Type	Package	PLL	Lamp Driver	VCO Stop	Sep. Cont.	Use			Remark
						R/C	Car	HI-FI	
KA2261	16 DIP	*	*	*	*	*	*		Sep = 45dB
KA2263	9 SIP	*	*	*		*	*		Sep = 45dB
KA2264/D	9 SIP/16 SOP	*	*	*		*			V_{CC} = 1.8 ~ 5V
KA2265	16 DIP	*	*	*	*			*	VCO Non-Adjusting MPX

† New Product
†† Under Development

D. Audio Power Amplifier

Type	Package	V_{CC} (V)	Output Power		Use			Remark
			R_L = 4 ohm	R_L = 8 ohm	R/C	Car	Hi-Fi	
KA2201	8 DIP	6		0.5W	*			V_{CC} = 3 ~ 14V
		9		1.2W				
KA2206	12 DIP/F	9	2.3W × 2		*			V_{CC} = 4.5 ~ 11V
KA2214	14 DIP H/S	9		1.2W × 2	*			V_{CC} = 3 ~ 16V
KA2209	8 DIP	3	110mW × 2		*			V_{CC} = 1.8 ~ 9V
KA22103	17 ZSIP H/S	13.2	19W × 2			*		V_{CC} = 9 ~ 18V
KA2212	9 SIP	6		0.5W	*			V_{CC} = 3.5 ~ 12V
LM386/S	8 DIP/9 SIP	6		0.325W	*			V_{CC} = 4 ~ 12V
KA2213	14 DIP H/S	6	1W		*			Included Pre-Amp with ALC
KA22130	16 DIP	6	1W		*			
KA22131	24 SOP	3	69mW × 2(R_L = 16Ω)		*			V_{CC} = 1.8 ~ 3.6V Included Auto Reverse Pre-AMP
KA22134	16 DIP	3	27mW × 2(R_L = 32Ω)		*			V_{CC} = 1.8 ~ 6V Dual PRE + POWER AMP with Volume Control
KA22135	22 SDIP	3	28mW × 2(R_L = 32Ω)		*			V_{CC} = 2 ~ 7.5V Dual PRE-POWER AMP and DC Motor Speed Controller
KA22136	28 SOP	3	28mW × 2 (R_L = 32Ω)		*			V_{CC} = 2 ~ 5V Dual PRE-POWER AMP with Volume Control and DC Motor Speed Controller
KA8602	8 DIP/8 SOP	6	300mW (R_L = 32Ω)		*			V_{CC} = 2 ~ 16V R_L = 8Ω ~ 100Ω

† New Product

E. Pre-Amplifier

Type	Package	Function	Use			Remark
			R/C	Car	Hi-Fi	
KA1222	8 SIP	Dual Pre-amplifier	*			V_{CC} = 2.5 ~ 6V
KA2220	9 SIP	Pre-amplifier with ALC	*		*	V_{CC} = 3.5 ~ 14V
KA2221	8 SIP	Dual Pre-amplifier	*	*	*	Included Voltage Regulator
KA22211	8 SIP	Dual Pre-amplifier	*	*	*	V_{CC} = 5 ~ 14V
KA2223	16 DIP	5 Band Mono Graphic EQ AMP	*	*	*	V_{CC} = 5 ~ 13V
KA22233	22 DIP	3 Band Dual Graphic EQ AMP	*	*	*	V_{CC} = 5 ~ 15V
KA22234	24 ZSIP-S	5 Band Dual Graphic EQ AMP	*	*	*	V_{CC} = 3.5 ~ 14V
KA2224	14 DIP	Dual Pre-amplifier with ALC	*		*	V_{CC} = 4 ~ 13V
KA22241	9 SIP	Dual Pre-amplifier with ALC	*			V_{CC} = 4.5 ~ 14V
KA22242	10 SIP	Dual Pre-amplifier with ALC	*			V_{CC} = 4 ~ 12V
KA2225/D	16 DIP/16 SOP	Dual Pre-amplifier with Mute	*			V_{CC} = 1.6 ~ 5V
KA22261	16 DIP	Dual Pre-amplifier with ALC	*		*	Included REC AMP
KA2228	21 ZSIP-S	Dual Pre-amplifier system	*		*	V_{CC} = 3.5 ~ 7V
KA22291	24 SDIP	Quad Pre-amplifier system	*		*	V_{CC} = 5 ~ 14V
KA7226	14 DIP	Dual Pre-amplifier with ALC	*		*	V_{CC} = 3 ~ 16V
††KA22292	48 QFP	1 Chip Tape Recorder System	*		*	V_{CC} = 4.5 ~ 15V
††KA22293	48 QFP	Audio Signal Processor			*	V_{CC} = 12V

F. LED Level Meter Driver

Type	Package	Function	Remark
KA2281	16 DIP	5 Dot dual red/yellow/green LED driver	VU scale, input amplifier Reference voltage included
KA2284	9 SIP	5 Dot mono green LED driver	VU scale Reference voltage included
KA2285	9 SIP	5 Dot mono red LED driver	VU scale Reference voltage included
KA2287	9 SIP	5 Dot mono green LED driver	Linear scale Reference voltage included
KA2288	16 DIP	7 Dot mono LED driver	VU scale Reference voltage included

† New Product
†† Under Development

G. Electronic DC Volume Control

Type	Package	Function	Remark
†KA2250	16 DIP	Electronic DC Volume Control	V_{CC} = 6 ~ 12V

H. 1 Chip Radio, 1 Chip Tuner System

Type	Package	Function	Remark
KA22421/D	16 DIP/16 SOP	AM 1 Chip Radio	V_{CC} = 2 ~ 5V
KA22426	28 SOP	AM/FM 1 Chip Radio	V_{CC} = 1.6 ~ 6V
KA22427	16 DIP	AM/FM 1 Chip Radio	V_{CC} = 3 ~ 12V
KA22429	16 SOP	FM 1 Chip Radio	V_{CC} = 1.8 ~ 6V
KA2292/D	24 DIP-S/24 SOP	AM/FM TUNER + MPX	V_{CC} = 1.8 ~ 7V
KA2293/D	24 DIP-S/24 SOP	AM/FM TUNER + MPX	V_{CC} = 1.8 ~ 7V
††KA2295	48 QFP	AM/FM TUNER + MPX for DTS	V_{CC} = 6 ~ 12V
††KA2296	64 QFP	AM/FM TUNER + N.C + MPX for CAR	V_{CC} = 7.5 ~ 9V
††KA2297	16 DIP	AM/FM TUNER	V_{CC} = 1.8 ~ 7V

I. Noise Reduction

Type	Package	Function	Remark
KA2271/D	16 DIP/16 SOP	Dolby B Type	V_{CC} = 8 ~ 16V
KA22711/D	16 DIP/16 SOP	Dolby B Type	V_{CC} = 5 ~ 16V
KA22712/D	16 DIP/16 SOP	Dolby B Type	V_{CC} = 6.5 ~ 16V
KA2272/D	16 ZSIP/16 SOP	FM Noise Canceller	V_{CC} = 8 ~ 15V

† New Product
†† Under Development

J. CD Player

Type	Package	Function	Remark
KS5990	80 QFP	16K SRAM + Digital Signal Processor	V_{DD} = 5V
KS5991	80 QFP		V_{DD} = 3 ~ 4V
KA8309B	48 QFP	Servo Signal Processor	V_{CC} = 5V
KA9201/Q	30 SDIP/SOP/ 32 QFP	RF Amp for CDP	V_{CC} = 5V
†KS9210	80 QFP	16K SRAM + DSP + Digital Out	V_{DD} = 5V
†KS9211	80 QFP	16K SRAM + Digital Signal Processor	V_{DD} = 3.4 ~ 5.5V
††KA9220	80 QFP	RF Amp + Servo Signal Processor	V_{CC} = 5V
†KA9221	48 QFP	Servo Signal Processor	V_{CC} = 3.4V
††KS9240	80 QFP	DSP for CD-ROM	V_{DD} = 5V
KA9256	10 SIP H/S	Dual Amp for CDP Motor Driver	V_{CC} = 15V, V_{EE} = − 15V
KA9257	12 SIP H/S	Dual Amp for CDP Motor Driver	V_{CC} = 5V
††KA9258	20 SOP/F	4 CH BTL Motor Driver	V_{CC} = 5V
†KA9270/D	20 DIP/SOP	Audio Filter for CDP	V_{CC} = 5 ~ 12V
††KS9282	80 QFP	16K SRAM + DSP + D/A Converter	V_{DD} = 5V
††KS9283	80 QFP	16K SRAM + Digital Signal Processor	V_{DD} = 5V
KDA0316	20 DIP/SOP	16-Bit D/A Converter	V_{DD} = 5V

K. LDP

Type	Package	Function	Remark
†KA9410	42 SDIP	Video Signal Processor	V_{CC} = 5V
†KA9420	42 SDIP	Servo Signal Processor	V_{CC} = ± 5V
†KA9430	42 SDIP	Time Base Corrector	V_{CC} = 5V
SL220B	28 DIP	OSD and Data Processor	V_{CC} = 5V
†KA9402	10 SOP	PDP for LDP	V_{CC} = ± 5V
††KA9401	80 QFP	Audio Signal Processor	V_{CC} = 5V
††KA9490	9 SIP	CCD Clock Generator	V_{CC} = 5V

† New Product †† Under Development

L. DC Motor Speed Control

Type	Package	Function	Remark
KA2401	8 DIP	DC Motor Speed Controller	$V_{CC} = 4 \sim 12V$
KA2402	8 DIP/8 SOP	DC Motor Speed Controller	$V_{CC} = 1.8 \sim 8V$
KA2404/A	TO-92L/TO-126	DC Motor Speed Controller	$V_{CC} = 4 \sim 12V$
KA2407	TO-126	DC Motor Speed Controller	$V_{CC} = 3.5 \sim 14.4V$

M. μ-COM

Type	Package	Function	Remark
†KS55C232	64 QFP	Digital Tuning System (DTS) for Car Stereo	$V_{CC} = 5V$, $V_{EE} = -5V$
KS56C820	80 QFP	System Control for CDP	$V_{CC} = 5V$, $V_{EE} = -5V$

† New Product
†† Under Development

1. AUDIO

1-1 Analog Audio

Application	SAMSUNG	SANYO	TOSHIBA	MATSUSHITA	ROHM	Others
Power Amplifier	KA2201	LA4145		AN7116	BA527	*TBA820M
	KA2212	*LA4140	*TA7313AP	*AN7112	BA526	
	KA8602					MC34119
	KA386		TA7336P		BA546	*LM386/*NJM386
Dual Power Amplifier	KA2206	*LA4182/3	TA7769P	AN7143	BA534	TEA2025
	KA2209	LA4530	TA7376P	AN7118		*TDA2822M
	†KA22103		*TA8210			
	KA2214					*μPC1263C
EQ AMP + Power	KA2213/0	*LA4160	TA7628			
Dual EQ AMP + Power	KA22131	LA4560M			*BA3502F	
	KA22134		*TA8119P			
	KA22135					*LAG637D
	KA22136					*LAG665
EQ AMP + ALC	KA2220	*LA3210	*TA7137P	AN7320	*BA333	μPC1158H
Dual EQ AMP	KA1222	*LA3160	TA7312P			*M51521L
	KA2221	*LA3161	*TA7375P	AN7310	*BA328	*M5152L
	KA22211	*LA3160	TA7312P			*M51521L
Graphic EQ AMP	KA2223	*LA3600	*TA7796P			*M5226P
	KA22233			AN7330K		
	KA22234				*BA3822L	
Dual EQ AMP + ALC	KA2224	*LA3220		AN7312	BA343	
	KA22241	LA3225/6N			*BA3308	M51544L
	KA22242	LA3225/6N			*BA3312N	M51544L
	KA22261		*TA7668BP			
	KA7226		*TA7658P	AN7312	BA343	
	KA2228		*TA7417P		BA3416BL	
Quad EQ AMP	KA22291		TA8189N			M51166P
	††KA22292				BA3422	
Dual EQ AMP + Mute	KA2225	LA3230	*TA7709P/F	AN7315	BA3304	
AM 1 Chip Radio	KA22421		*TA7641BP			*CIC7641
AM/FM 1 Chip Radio	†KA22426					*CXA1019
	KA22427		*TA7613AP			*TDA1083/*ULN2204
	KA22429		*TDA7021T			
AM/FM IF + DET	KA2243				*BA4220	*HA12413

AUDIO (Continued)

Application		SAMSUNG	SANYO	TOSHIBA	MATSUSHITA	ROHM	Others
FM IF + DET		KA2244		*TA7303P	AN278	*BA404	
		KA22441	*LA1140		AN7277	*BA4110	
		KA2245	*LA1150	*TA7130P		*BA403	*μPC1028H
AM Tuner + AM/FM IF + DET		KA2247	*LA1260		AN7223	*BA4260	
		KA22471		*TA7640AP	AN7223		
		KA2248A	LA1270	*TA7687AP		BA4228L	
FM Front End		KA22495	*LA1185	*TA7358AP	*AN7205		
Electronic DC Volume Control		†KA2250		*TC9153			
FM Stereo Multiplex Decoder		KA2261	*LA3361	*TA7604P	*AN7410	*BA1330	*HA11227/*μPC1197C
		KA2263		*TA7343AP	*AN7420		
		KA2264	LA3330	*TA7342P	*AN7421	BA1360	
		KA2265	*LA3410	TA7413AP	AN7470		
Noise Reduction	Dolby B-Type	KA2271		TA7719P			*CXA1101P
		KA22711					*CXA1163
		KA22712					*CXA1102
	FM N.C.	KA2272	*LA2110				
LED Level Meter Driver		KA2281		*TA7666P			IR2E27
		KA2284	*LB1403	TA7366P	*AN6884	*BA6124	
		KA2285	*LB1423	TA7366P		*BA6137	
		KA2287	*LB1413			*BA6125	
		KA2288					*IR2E02
AM/FM Tuner		††KA2297		*TA2003			
AM/FM 1 Chip Tuner + FM MPX		KA2292		*TA8167/27			
		KA2293		*TA8122			
		††KA2295	LA1830				
AM/FM 1 Chip Tuner + FM MPX + N.C.		††KA2296	*LA1883				
Audio Processor		††KA22293					
DC Motor Speed Controller		KA2401					*μPC1470H
		KA2402	*LA5521D		AN6612		
		KA2404			AN6610		μPC1470H
		KA2407			*AN6651		

† New Product * Direct Replacement

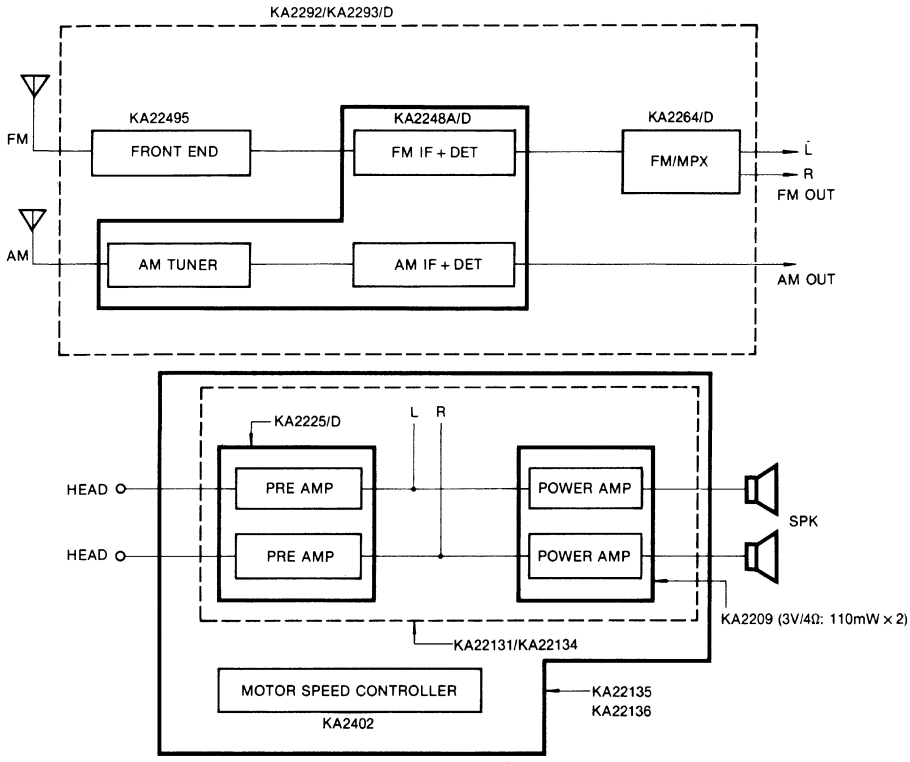
1-2 Digital Audio

Application		SAMSUNG	SANYO	TOSHIBA	SONY	HITACHI	Others
CDP	RF Amp	KA9201		TA8137	*CXA1081		
		†KA9201Q			*CXA1271		
	Digital Signal Processor	KS5990	LC7860K	TC9200F	CXD1130		
		KS5991			CXD1247		
		†KS9210		TC9221F	*CXD1167		
		†KS9211			CXD1130		
		††KS9283	LC7865	TC9236	CXD2500		
	Servo Signal Processor	KA8309		TC9201	*CXA1082		
		†KA9221			*CXA1272		
	RF Amp + SSP	††KA9220	LA9210	TA8191		HA12158	
	DSP + DAC	††KS9282				HD49220	
	D/A Converter	KDA0316	*LC7881	TC9218	*CXD1161		
		††KDA0317	LC7883	TC9239			MN6623B
		††KDA0318					CS4328
	Motor Driver	KA9256		*TA7256			
		KA9257					*BA6290
		††KA9258					*BA6296
LDP		†KA9410				*HA11528	
		††KA9420				*HA11529	
		†KA9430				*HD49403	
		††KA9401				HA12127	
		†KA9402					
		††KA9490					
μ-Com		†KS55C232	LC7230	TC9302			μPD1719
		KS56C820			CXP5024		

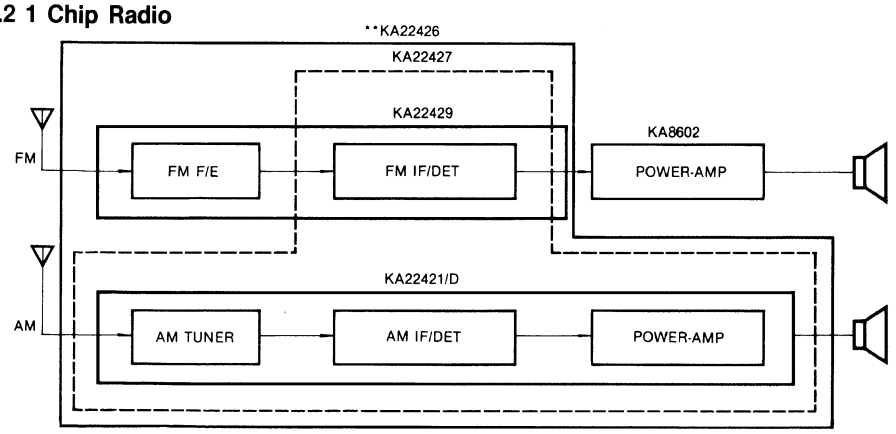
† New Product †† Under Development * Direct Replacement

1. AUDIO APPLICATION

1.1 Mini Radio Cassette

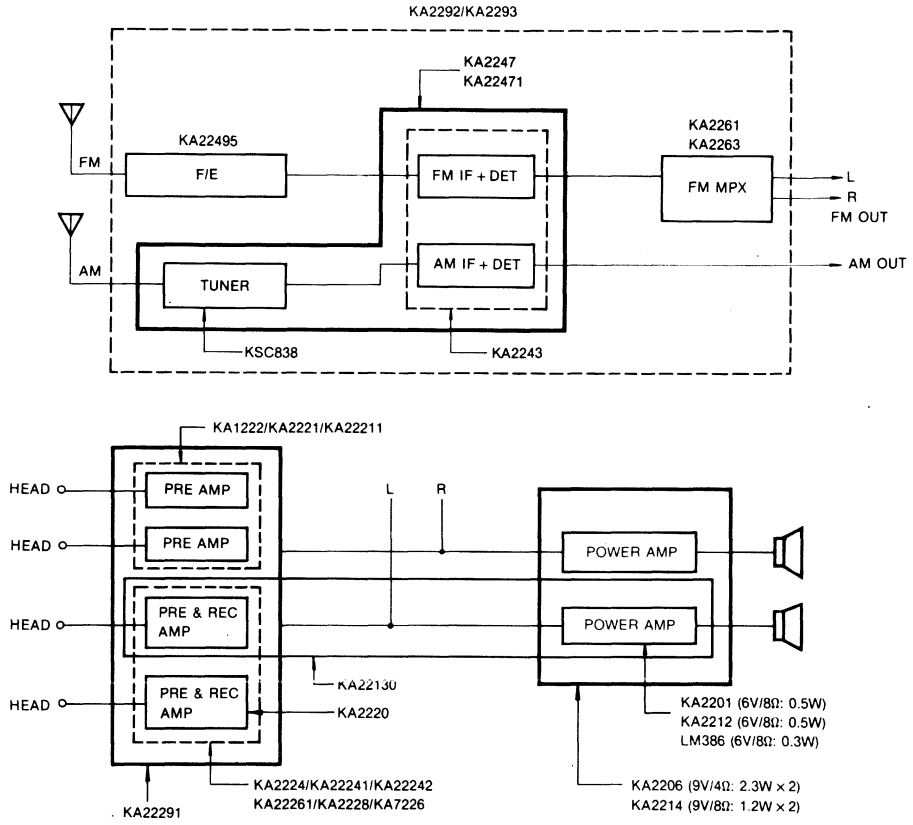


1.2 1 Chip Radio



* New Product
** Under Development

1.3 Portable Radio Cassette & Music Center

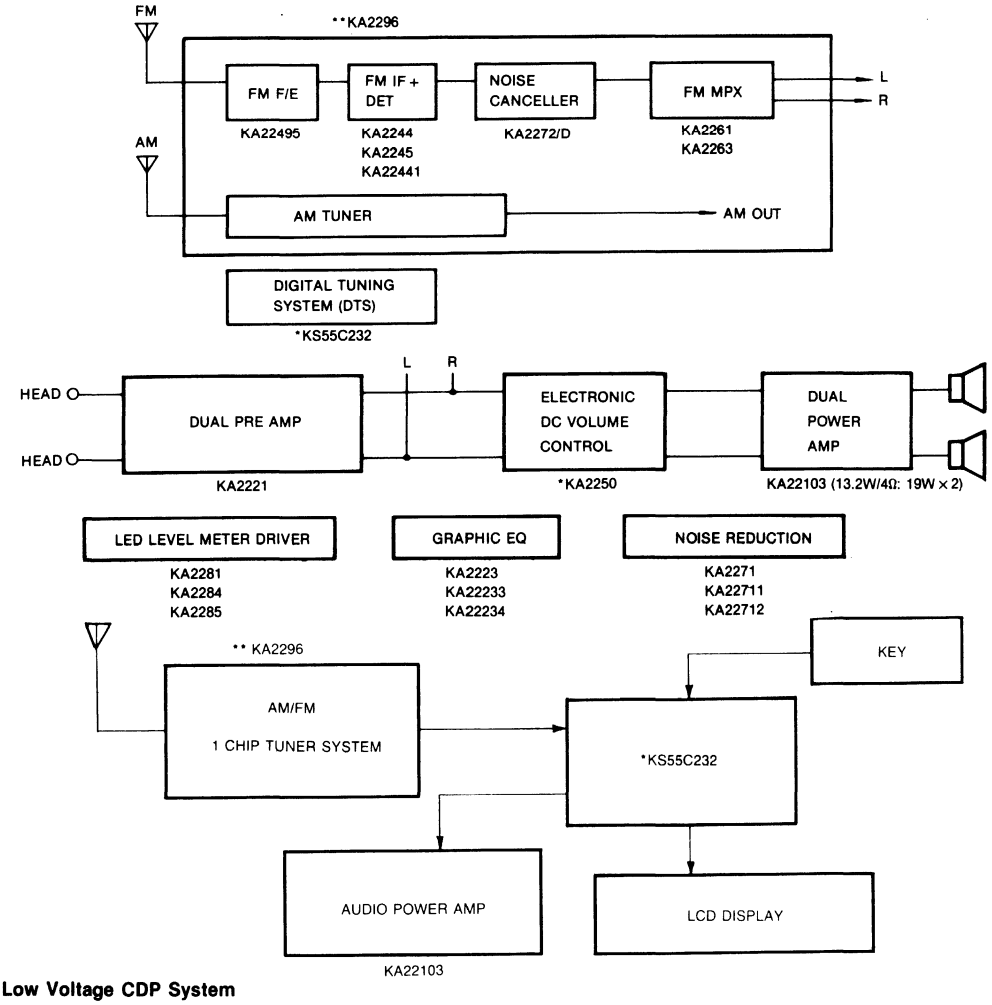


MOTOR SPEED CONTROLLER	LED LEVEL METER DRIVER	GRAPHIC EQ	ELECTRONIC DC VOLUME CONTROL
KA2401	KA2281 (5 DOT DUAL)	KA2223 (5 BAND MONO)	KA2250
KA2404	KA2284 (5 DOT MONO)	KA22233 (3 BAND DUAL)	
KA2407	KA2285 (5 DOT MONO)	KA22234 (5 BAND DUAL)	
	KA2287 (5 DOT MONO)		
	KA2288 (7 DOT MONO)		

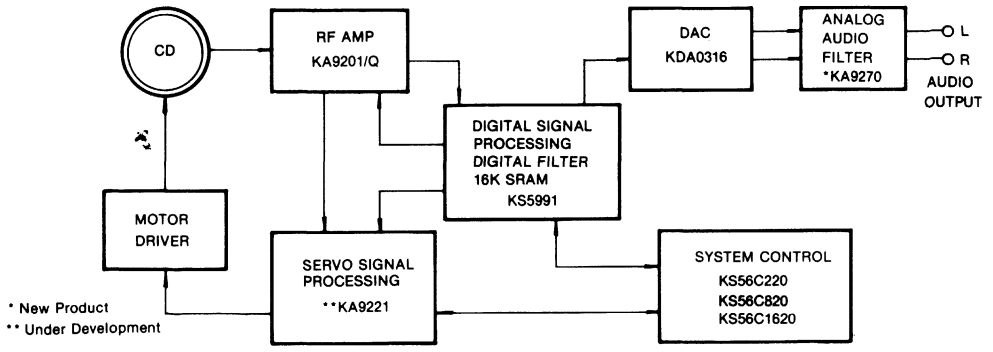
NOISE REDUCTION
KA2271
KA22711
KA22712

* New Product

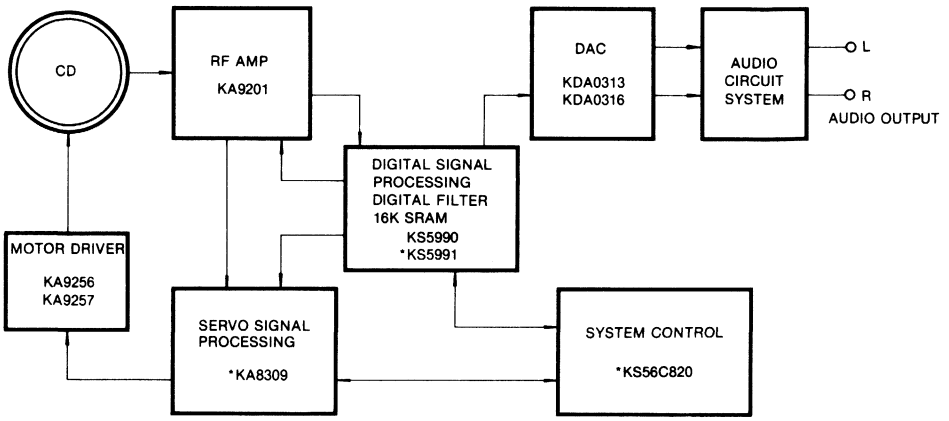
1.4 Car Audio



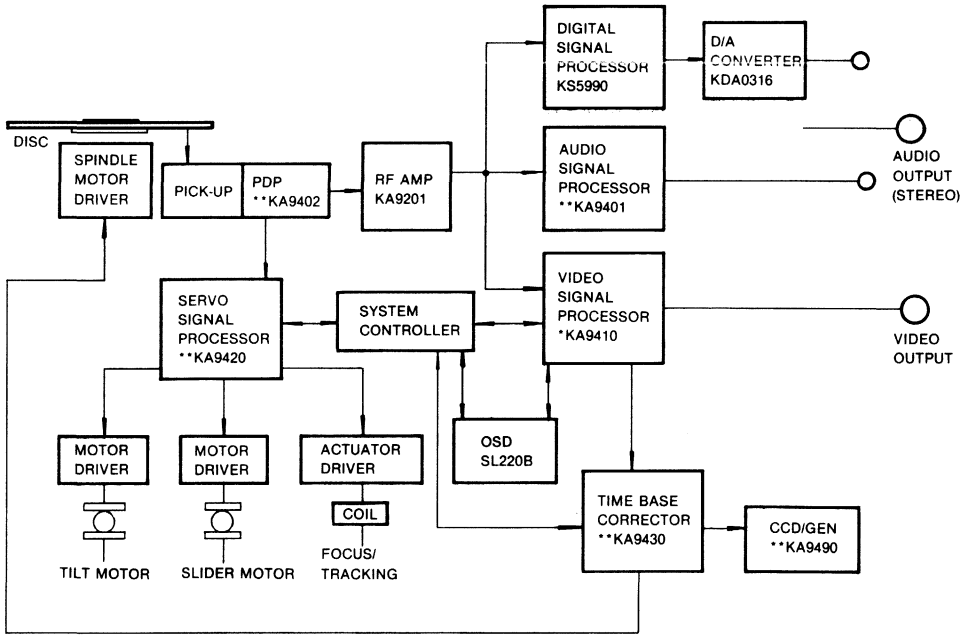
1) Low Voltage CDP System



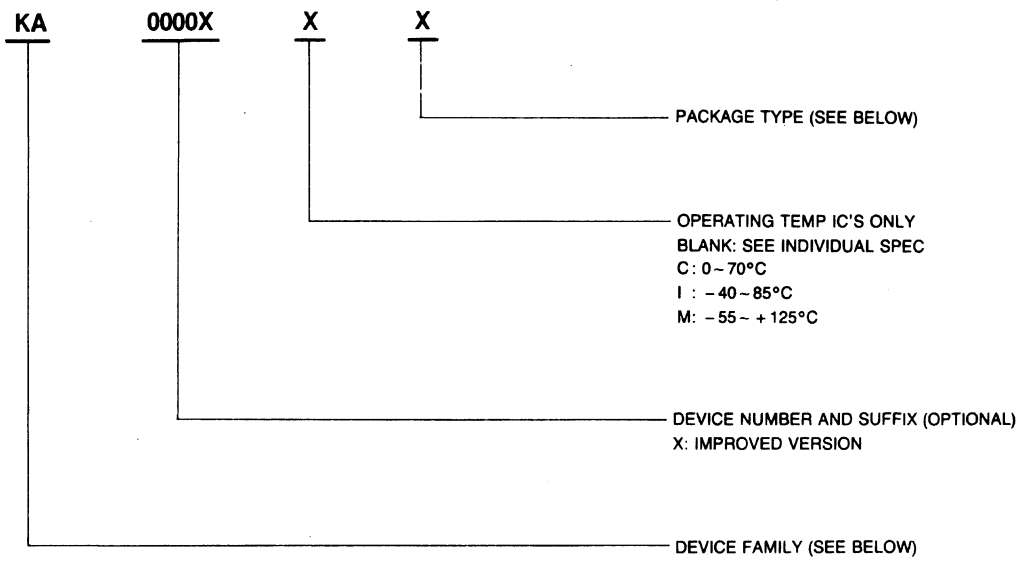
2) Potable & Home CDP System



3) LDP System



3. ORDERING INFORMATION



DEVICE FAMILY

TRANSISTOR / FET

DKS	DALINGTON TR
• IRF	MOS POWER
• IRFA	MOS POWER, TO-126
• IRFP	MOS POWER, TO-3P
• KSA	PNP TR
KSB	PNP TR
KSC	NPN TR
KSD	NPN TR
• MMBT	TR, SOT-23
• MMBTA	TR, SOT-23
• MMBTH	TR, SOT-23
• MPS	TR, SOT-23
• MPSA	TR, TO-92
• MPSH	TR, TO-92
• PN	TR, TO-92
SSH	MOS POWER, TO-3P
SSM	MOS POWER, TO-3
SSP	MOS POWER, TO-220
• TIP	BIPOLAR TR
• 2N	TR

INTEGRATED CIRCUIT

KA	LINEAR IC
KF	J-FET OP AMP
KG	GATE ARRAY
KS	CMOS IC
KT	TELECOM
SA	LINEAR ARRAY
SD	H.D AND LINEAR ARRAY
KSV	A/D-D/A CONVERTER
KAD	A/D CONVERTER
KDA	D/A CONVERTER

RENAMED INFORMATION

TRANSISTOR

• MMBT
• MMBTA
• MMBTH
→ KST

• MPS
• MPSA
• MPSH
→ KSP

PACKAGE TYPE

IC'S ONLY

D	SOP
DT	D-PACK
J	CERAMIC
K	TO-3P
L	LCCC
N	PLASTIC
PL	PLCC
R	TO-126
T	TO-220
Z	TO-92
V	TO-92L
W	ZIP
S	SIP
G	BARE CHIP
E	SSM

INTEGRATED CIRCUIT

• LM
• MC
• NE
→ KA (BIPOLAR TYPE)
KS (CMOS TYPE)

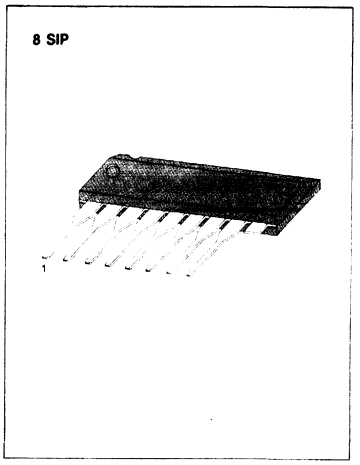
• NOTE: Direct-Replacement parts for products initiated by other manufacturers.

AUDIO ICs 3

Device	Function	Package	Page
KA1222	Dual Low Noise Equalizer Amplifier	8 DIP	55
KA2201	1.2W Audio Power Amplifier	8 DIP	59
KA2206	2.3W Dual Audio Power Amplifier	12 DIP IF	63
KA2209	Dual Low Voltage Power Amplifier	8 DIP	67
KA22103	19W Dual Power Amplifier	17 ZIP H/S	70
KA2212	0.5W Audio Power Amplifier	9 SIP	76
KA2213	One-Chip Tape Recorder System	14 DIP H/S	80
KA22130	One-Chip Tape Recorder System	16 DIP	84
KA22131	Dual Pre-Power Amplifier for Auto Reverse	24 SOP	88
KA22134	Dual Pre-Power Amplifier with DC Volume Control	16 DIP	92
KA22135	Dual Pre-Power Amplifier and DC Motor Speed Controller	22 SDIP	96
KA22136	Dual Pre-Power Amplifier, Volume Controller and DC Motor Speed Controller	28 SDIP/28 SOP	101
KA2214	1W Dual Power Amplifier	14 DIP H/S	105
KA2220	Equalizer Amplifier with ALC	9 SIP	108
KA2221	Dual Low Noise Equalizer Amplifier	8 SIP	113
KA22211	Dual Low Noise Equalizer Amplifier	8 SIP	117
KA2223	5-Band Graphic Equalizer Amplifier	16 DIP	120
KA22233	3-Band Dual Graphic Equalizer Amplifier	22 DIP	124
KA22234	5-Band Dual Graphic Equalizer Amplifier	24 ZSIP	128
KA2224	Dual Equalizer Amplifier with ALC	14 DIP	132
KA22241	Dual Equalizer Amplifier with ALC	9 SIP	138
KA22242	Dual Equalizer Pre-Amplifier with ALC	10 SIP	142
KA2225	Dual Pre-Amplifier for 3V Using	16 DIP/16 SOP	150
KA22261	Dual Equalizer Amplifier with Ree AMP	16 DIP	153
KA2228	Dual Equalizer Amplifier System	21 ZSIP	157
KA22291	Quad Equalizer Amplifier for Double Cassette	24 SDIP	167
KA22421	AM 1-Chip Radio	16 DIP/16 SOP	172
KA22426	AM/FM 1-Chip Radio	28 SOP/28 DIP	177
KA22427	AM/FM 1-Chip Radio	16 DIP	180
KA22429	FM One-Chip Radio	16 SOP	189
KA2243	AM/FM IF System	16 DIP	193
KA2244	FM IF System for Car Radio	9 DIP	200
KA22441	FM IF System for Car Stereo	16 ZSIP	204
KA2245	FM IF System for Car Radio	7 SIP	210
KA2247	FM IF/AM Tuner System	16 DIP	213
KA22471	FM IF/AM Tuner System	16 DIP	216
KA2248	3V FM IF/AM Tuner System	16 DIP/20 SOP	220
KA22495	FM Front End for FM Band	9 SIP/14 SOP	224
KA2250	Dual Electronic Volume Control	16 DIP	231
KA2261	FM Stereo Multiplex Decoder	16 DIP	239
KA2263	FM Stereo Multiplex Decoder	9 SIP	244
KA2264	FM Stereo Multiplex Decoder	9 SIP/16 SOP	248
KA2265	Vco Non-Adjusting FM Stereo Multiplex Decoder	16 DIP	251
KA2271	Dolby B-Type Noise Reduction Processor	16 DIP	254
KA22711	Dolby B-Type Noise Reduction Processor	16 DIP	261
KA22712	Dolby B-Type Noise Reduction Processor	16 DIP	268
KA2272	FM Noise Canceller	16 ZSIP/16 SOP	275
KA2281	5-Dot Dual LED Level Meter Driver	16 DIP	281
KA2284/85	5-Dot LED Level Meter Driver	9 SIP	284
KA2287	5-Dot LED Linear Level Meter Driver	9 SIP	287
KA2288	7-Dot LED Level Meter Driver	16 DIP	290
KA2292	AM/FM Tuner + MPX	24 SDIP/24 SOP	293
KA2293	AM/FM Tuner + MPX	24 SDIP/24 SOP	298
KA2401	DC Motor Speed Controller	8 DIP	303
KA2402	Low Voltage DC Motor Speed Controller	8 DIP/8 SOP	308
KA2404	DC Motor Speed Controller	TO-92L	311
KA2407	DC Motor Speed Controller	TO-126	317
KA7226	Dual Equalizer Amplifier with ALC	14 DIP	321
KA8602	Low Voltage Audio Amplifier	8 DIP/8 SOP	327
KA386	Low Voltage Audio Power Amplifier	8 DIP/8 SOP	331

DUAL LOW NOISE EQUALIZER AMPLIFIER

The KA1222 is a monolithic integrated circuit consisting of a 2-channel pre-amplifier in a 8-pin plastic single in line package. Minimum operating voltage is 2.5 volts, thus it is suitable for low voltage application.



FEATURES

- **Wide operating supply voltage: V_{CC} = 2.5V ~ 6V**
- **Low noise (V_{NI} = 1.0μV: Typ).**
- **High channel separation.**
- **Good ripple rejection ratio.**
- **Minimum number of external parts required.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA1222	8 SIP	-20 ~ +70°C

BLOCK DIAGRAM

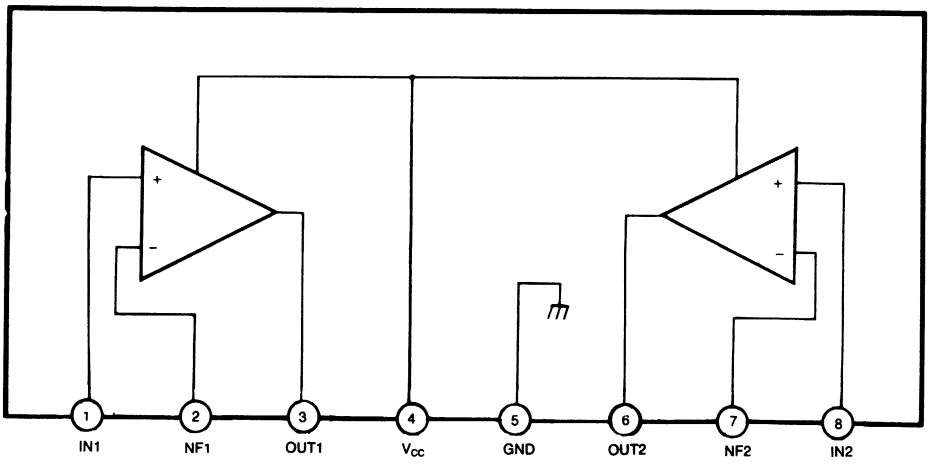


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	7.5	V
Power Dissipation	P_D	200	mW
Operating Temperature	T_{OPR}	−20 ~ +70	°C
Storage Temperature	T_{STG}	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 4V, R_L = 10KΩ, R_G = 600Ω, f = 1KHz, NAB, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CCQ}	V_I = 0		2.0	6.0	mA
Open Loop Voltage Gain	G_{VO}		65	80		dB
Closed Loop Voltage Gain	G_{VC}	V_O = 0.2V	33	35	37	dB
Output Voltage	V_O	THD=1%	0.4	0.7		V
Total Harmonic Distortion	THD	V_O = 0.2V		0.1	0.3	%
Input Resistance	R_I			150		KΩ
Equivalent Input Noise Voltage	V_{NI}	R_G = 2.2KΩ BW (−3dB)=15Hz ~ 30KHz		1.0	2.0	μV
Cross Talk	CT	R_G = 2.2KΩ	50	65		dB

TEST CIRCUIT

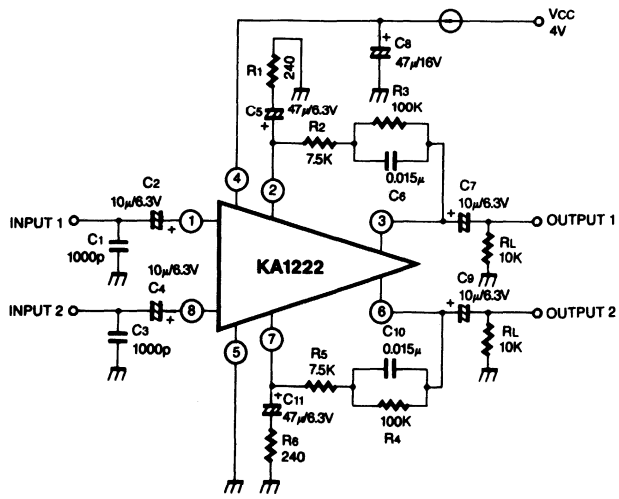
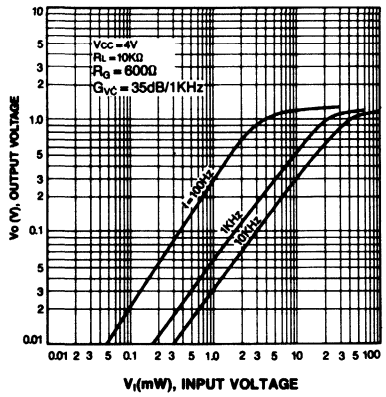
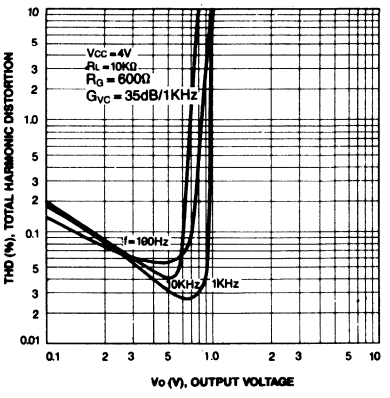


Fig. 2

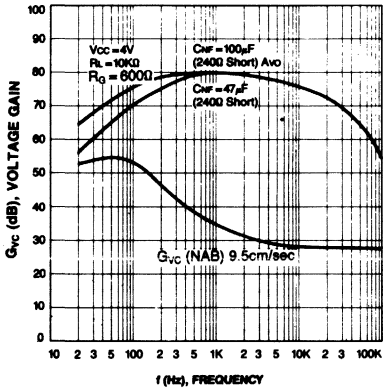
OUTPUT VOLTAGE-INPUT VOLTAGE



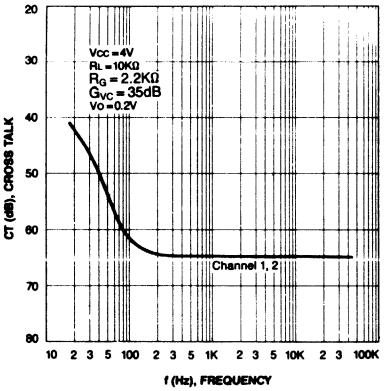
TOTAL HARMONIC DISTORTION-OUTPUT VOLTAGE



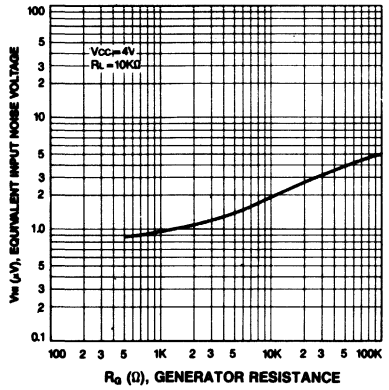
VOLTAGE GAIN-FREQUENCY



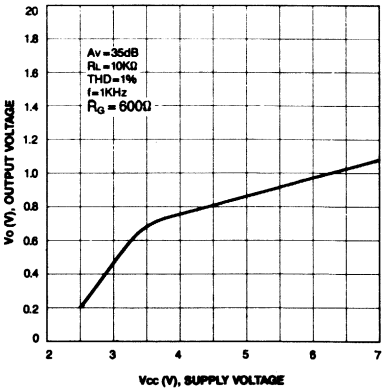
CROSS TALK-FREQUENCY

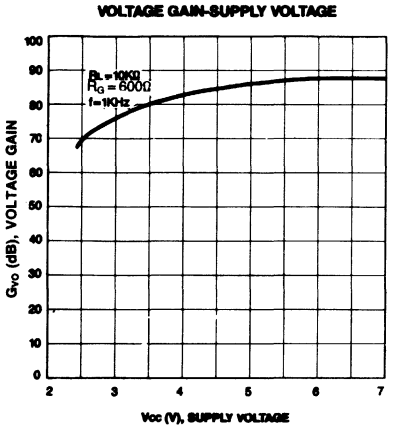


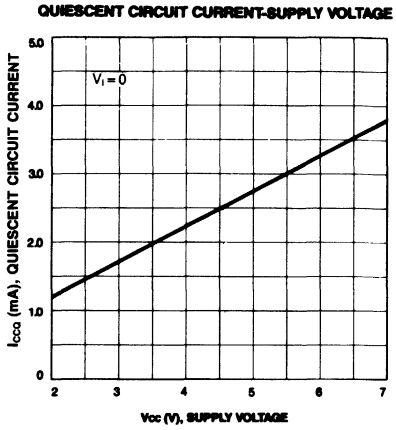
EQUIVALENT INPUT NOISE VOLTAGE GENERATOR RESISTANCE



OUTPUT VOLTAGE-SUPPLY VOLTAGE







APPLICATION CIRCUIT

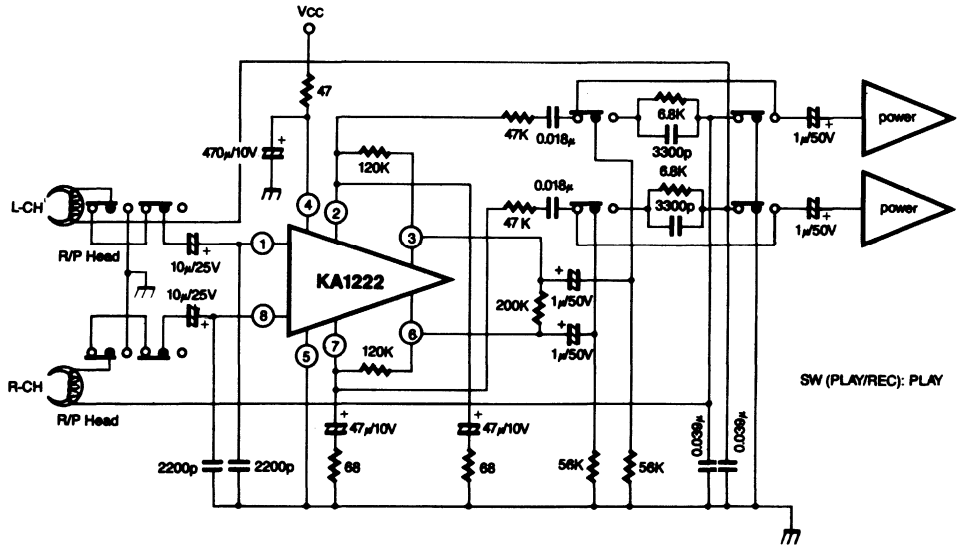


Fig. 3

1.2W AUDIO POWER AMPLIFIER

The KA2201 is a monolithic integrated audio amplifier. It is designed for audio frequency class B amplifiers.

8 DIP

FEATURES

- **Wide operating supply voltage: V_{CC} = 3V ~ 14V**
- **Medium output power.**
  P_O = 1.2W at V_{CC} = 9V, R_L = 8Ω, THD = 10%.
- **Low quiescent circuit current (I_{CCQ} = 4mA: Typ).**
- **Good ripple rejection.**
- **Minimum number of external parts required.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2201	8 DIP	-20°C ~ 70°C

BLOCK DIAGRAM

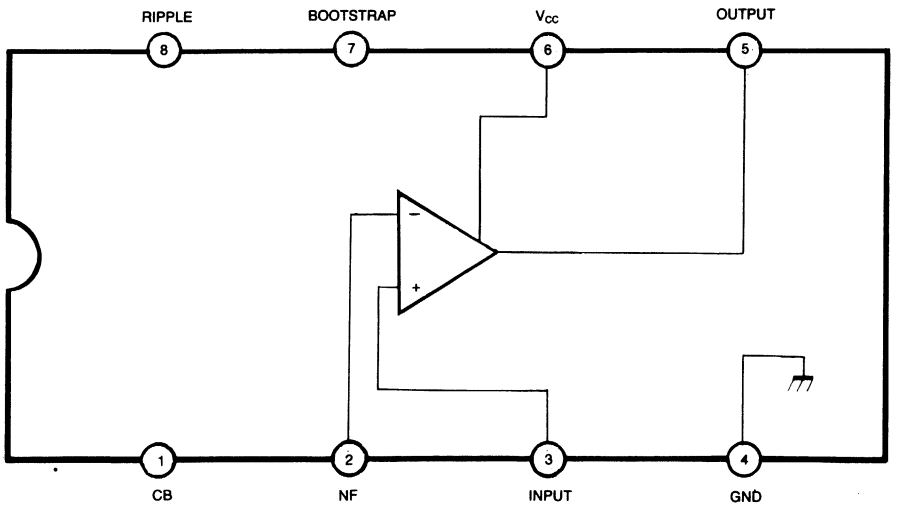


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Output Peak Current	I_{PK}	1.5	A
Power Dissipation	P_D	1.25	W
Operating Temperature	T_{OPR}	−20 ~ +70	°C
Storage Temperature	T_{STG}	−40 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 9V, f = 1KHz, R_G = 600Ω, R_F = 120Ω, R_L = 8Ω, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CCQ}	V_i = 0		4	12	mA
Output Power	P_O	V_{CC} = 9V, R_L = 4Ω, THD = 10% V_{CC} = 9V, R_L = 8Ω, THD = 10% V_{CC} = 6V, R_L = 4Ω, THD = 10% V_{CC} = 6V, R_L = 8Ω, THD = 10% V_{CC} = 12V, R_L = 8Ω, THD = 10%	 0.9 0.4 	1.6 1.2 0.75 0.5 2		W
Total Harmonic Distortion	THD	P_O = 500mW		0.3	1.0	%
Open Loop Voltage Gain	G_{VO}	R_F = 0		75		dB
Closed Loop Voltage Gain	G_{VC}	R_F = 120Ω	33	36	39	dB
Input Resistance	R_I			5		MΩ
Output Noise Voltage	V_{NO}	R_G = 10KΩ BW (−3dB) = 50Hz ~ 20KHz		0.3	1.0	mV

TEST CIRCUIT

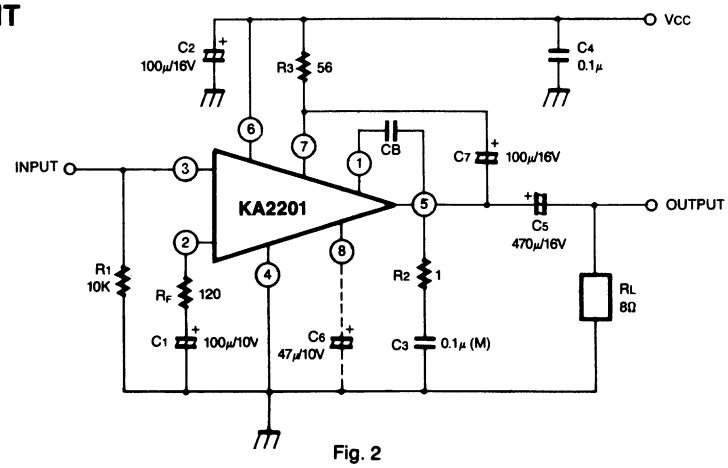
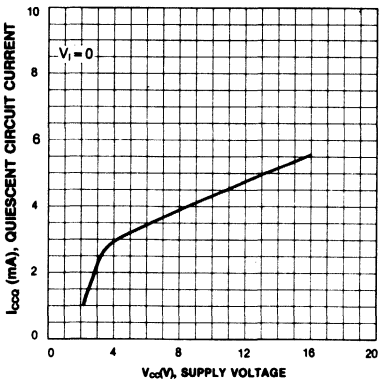
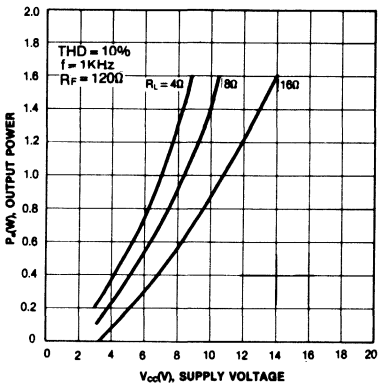


Fig. 2

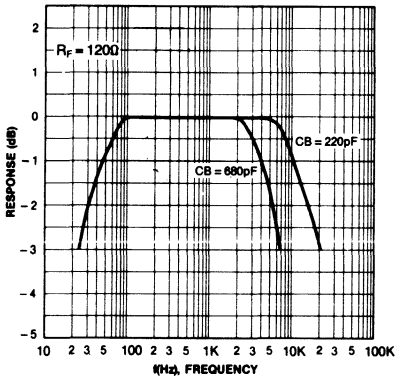
QUIESCENT CIRCUIT CURRENT—SUPPLY VOLTAGE



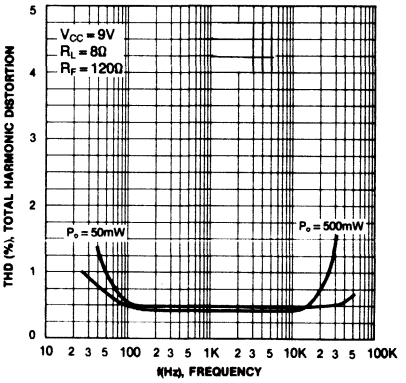
OUTPUT POWER-SUPPLY VOLTAGE



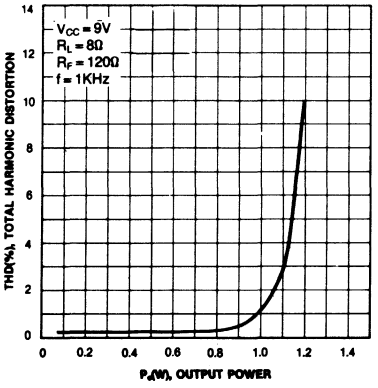
FREQUENCY RESPONSE



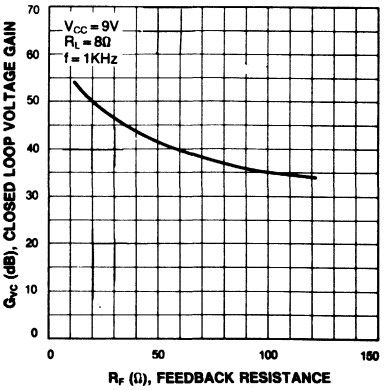
TOTAL HARMONIC DISTORTION-FREQUENCY



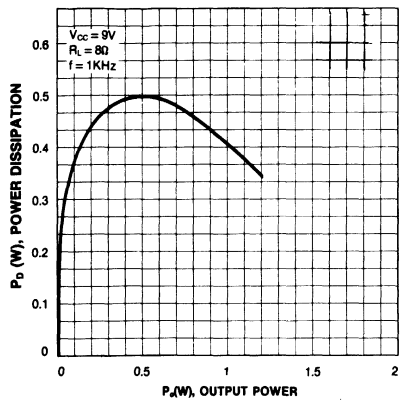
TOTAL HARMONIC DISTORTION-OUTPUT POWER



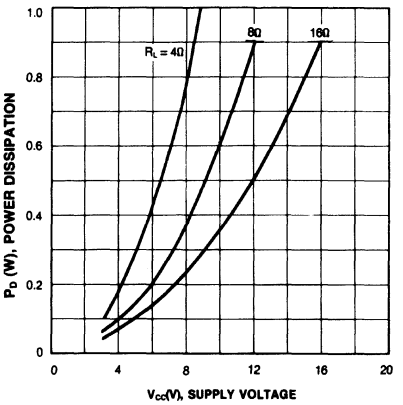
VOLTAGE GAIN-FEEDBACK RESISTANCE



POWER DISSIPATION-OUTPUT POWER



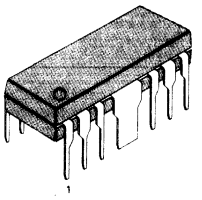
POWER DISSIPATION-SUPPLY VOLTAGE



2.3W DUAL AUDIO POWER AMPLIFIER

The KA2206 is a monolithic integrated circuit consisting of a 2-channel power amplifier. It is suitable for stereo and bridge amplifier application of radio cassette tape recorders.

12 DIP/F



FEATURES

- **High output power**
  Stereo: P_O =2.3W (Typ) at V_{CC} =9V, R_L =4Ω.
  Bridge: P_O =4.7W (Typ) at V_{CC} =9V, R_L =8Ω.
- **Low switching distortion at high frequency.**
- **Small shock noise at the time of power on/off due to a built-in muting circuit**
- **Good ripple rejection due to a built-in ripple filter.**
- **Good channel separation.**
- **Soft tone at the time of output saturation.**
- **Closed loop voltage gain fixed 45dB (Bridge: 51dB) but availability with external resistor added.**
- **Minimum number of external parts required.**
- **Easy to design radiator fin.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2206	12 DIP/F	−20°C ~ 70°C

BLOCK DIAGRAM

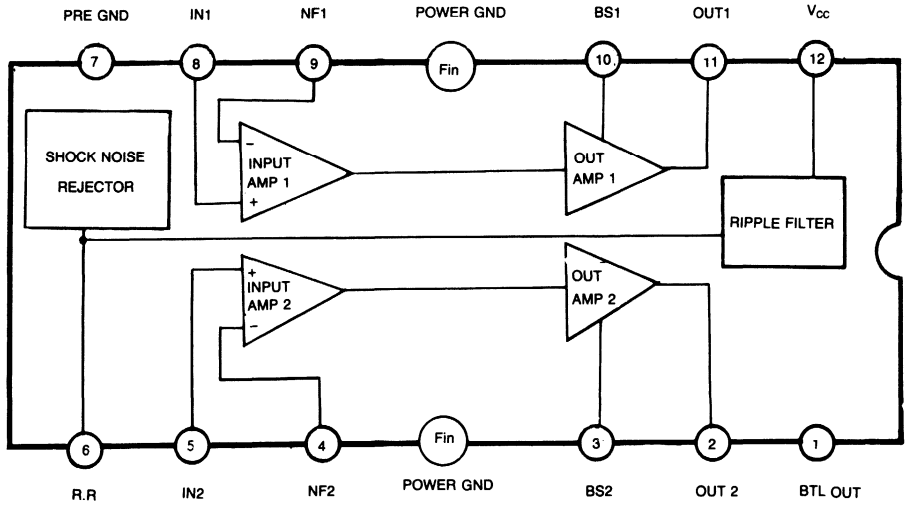


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	15	V
Power Dissipation	P_D	4*	W
Operating Temperature	T_{OPR}	−20 ~ +70	°C
Storage Temperature	T_{STG}	−40 ~ +150	°C

* Fin is soldering on the PCB

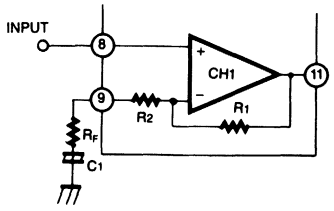
ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 9V, f = 1KHz R_G = 600Ω, unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Operating Supply Voltage	V_{CC}				9	11	V
Quiescent Circuit Current	I_{CCQ}	V_I=0, Stereo			40	55	mA
Closed Loop Voltage Gain	G_{VC}	Stereo	V_I=−45dBm	43	45	47	dB
		Bridge		49	51	53	dB
Channel Balance	CB	Stereo		−1	0	+1	dB
Output Power	P_O	Stereo	R_L=4Ω, THD=10%,	1.7	2.3		W
			R_L=8Ω, THD=10%		1.3		W
		Bridge	R_L=8Ω, THD=10%		4.7		W
Total Harmonic Distortion	THD	Stereo	P_O=250mW, R_L=4Ω		0.3	1.5	%
		Bridge			0.5		%
Input Resistance	R_I			21	30		KΩ
Ripple Rejection Ratio	RR	Stereo, R_g=0Ω, V_r=150mV f=100Hz		40	46		dB
Output Noise Voltage	V_{NO}	Stereo, R_g=0Ω			0.3	1.0	mV
		Stereo, R_g=10KΩ			0.5	2.0	mV
Cross Talk	CT	Stereo, R_g=10KΩ, V_o=0dBm		40	55		dB

APPLICATION INFORMATION

1. Stereo application



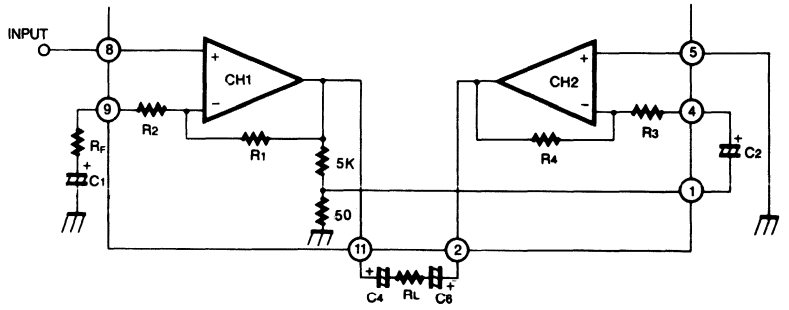
i) Fixed voltage gain
(Pin 9 connected to GND directly)

$$G_V = 20 \log \frac{R_1}{R_2} (dB)$$

ii) Variable voltage gain
(Rf and C1 connected with pin 9)

$$G_V = 20 \log \frac{R_1}{R_2 + R_F} (dB)$$

2. Bridge application



i) Fixed voltage gain (Pin 9 connected to GND directly)

$$G_V = 20 \log \frac{R_1}{R_2} + 6 (dB)$$

ii) Variable voltage gain R_F and C_1 connected with pin 9)

$$G_V = 20 \log \frac{R_1}{R_2 + R_F} + 6 (dB)$$

APPLICATION CIRCUIT

1. Stereo Amplifier

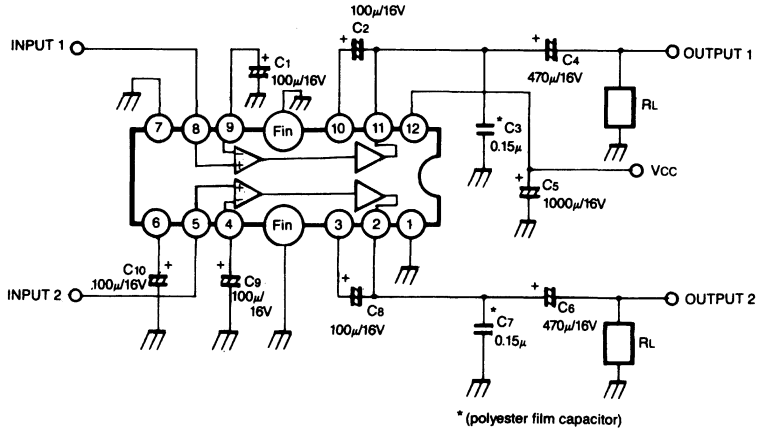


Fig. 2

2. Bridge Amplifier

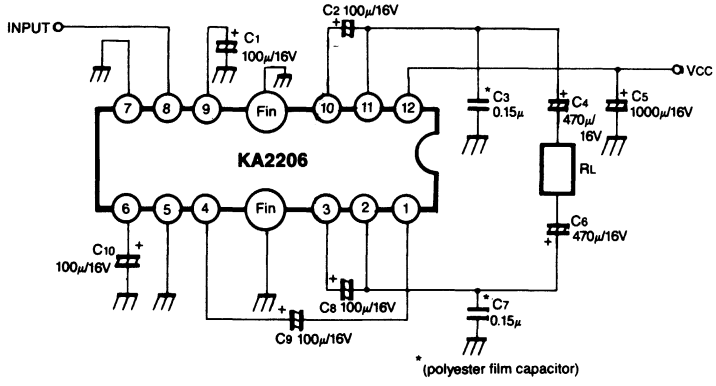
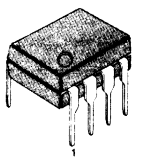


Fig. 3

DUAL LOW VOLTAGE POWER AMPLIFIER

The KA2209 is a monolithic integrated audio amplifier in a 8-pin plastic dual in line package. It is designed for portable cassette players and radios.

8 DIP



FEATURES

- **Wide operating supply voltage: V_{CC} = 1.8V ~ 9V**
- **Low crossover distortion**
- **Low quiescent circuit current**
- **Bridge/stereo configuration**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2209	8 DIP	− 20°C ~ + 70°C

BLOCK DIAGRAM

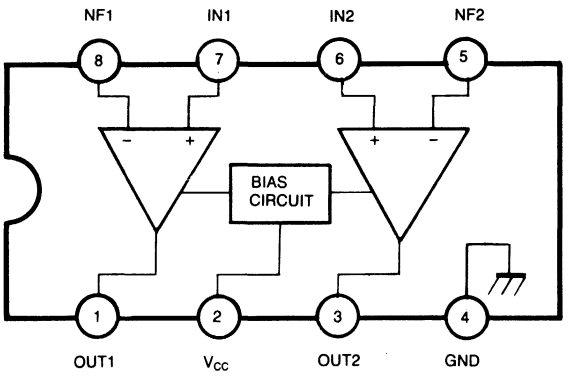


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	15	V
Output Peak Current	I_{PK}	1	A
Power Dissipation	P_D	at T_{AMB} = 50°C 1.0 at T_{CASE} = 50°C 1.4	W
Operating Temperature	T_{OPR}	−20 ~ +70	°C
Storage Temperature	T_{STG}	−40 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(T_a = 25°C, V_{CC} = 6V, f = 1KHz, unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Operating Voltage	V_{CC}			1.8		9	V
Quiescent Circuit Current	I_{CCQ}	V_I = 0			9		mA
Closed Loop Voltage Gain	G_{VC}	Stereo			40		dB
		Bridge			40		dB
Channel Balance	CB	Stereo		−1	0	1	dB
Output Power	P_O	Stereo	V_{CC} = 6V, R_L = 4Ω, THD = 10%	0.4	0.65		W
			V_{CC} = 3V, R_L = 4Ω, THD = 10%		0.11		W
		Bridge	V_{CC} = 6V, R_L = 8Ω, THD = 10%	0.9	1.35		W
			V_{CC} = 3V, R_L = 4Ω, THD = 10%		0.35		W
Total Harmonic Distortion	THD	Stereo, R_L = 8Ω, P_O = 0.2W			0.5		%
		Bridge, R_L = 8Ω, P_o = 0.5W			0.5		%
Ripple Rejection Ratio	RR	Stereo, f = 100Hz, C_3 = 100μF		24	30		dB
Output Noise Voltage	V_{NO}	Stereo, BW(−3dB) = 20Hz ~ 20KHz			0.5	2.0	mV
Cross Talk	CT	Stereo, f = 1KHz			50		dB
Input Resistance	R_I			100			KΩ

APPLICATION CIRCUIT

1. STEREO

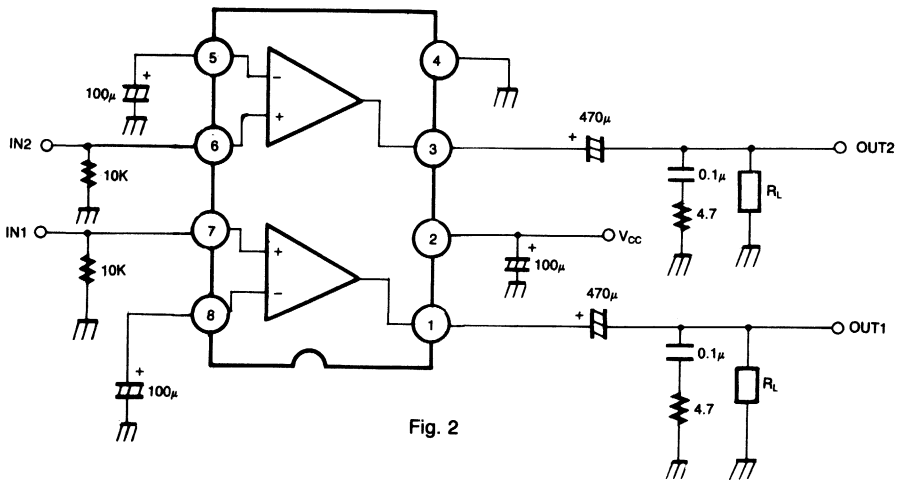


Fig. 2

2. BRIDGE

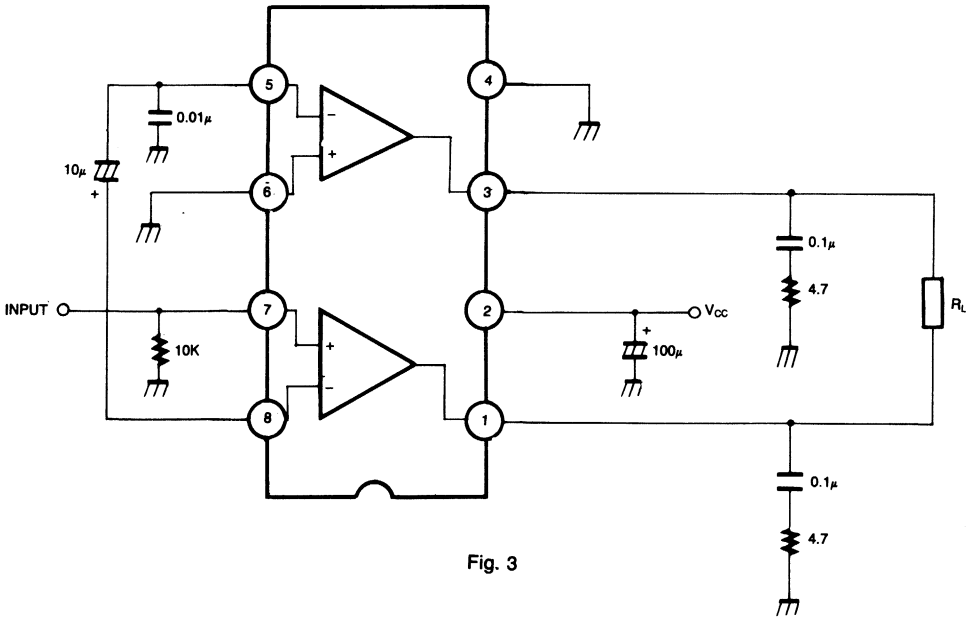
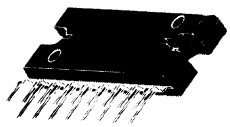


Fig. 3

19W DUAL POWER AMP

The KA22103 is a monolithic integrated circuit consisting of a 2-channel 19W power amplifier for car stereos. It is designed for high power, low distortion and multi functions. Since it uses an excellent 17-pin package, thermal characteristics are good with high performance.

17ZSIP H/S



FEATURES

- **High power: 19W/2-Ch**
  (V_{CC} = 13.2V, f = 1KHz, THD = 10%, R_L = 4Ω)
- **Minimum number of external parts required**
- **Low distortion: THD = 0.04%**
- **Low noise.** V_{NO} = 0.25mVrms
  (V_{CC} = 13.2V, R_L = 4Ω, R_G = 10KΩ, G_{VC} = 40dB, BW = 20Hz ~ 20KHz)
- **Built-in stand-by and mute function**
- **Protector: Thermal shut down**
  Over voltage protection
  DC short protection with V_{CC}-output and GND
  AC short protection with each output channel
- Operating supply voltage range: V_{CC} = 9V ~ **18V**
- **Connect H/S to GND**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA22103	17ZSIP H/S	−30 ~ +85°C

BLOCK DIAGRAM

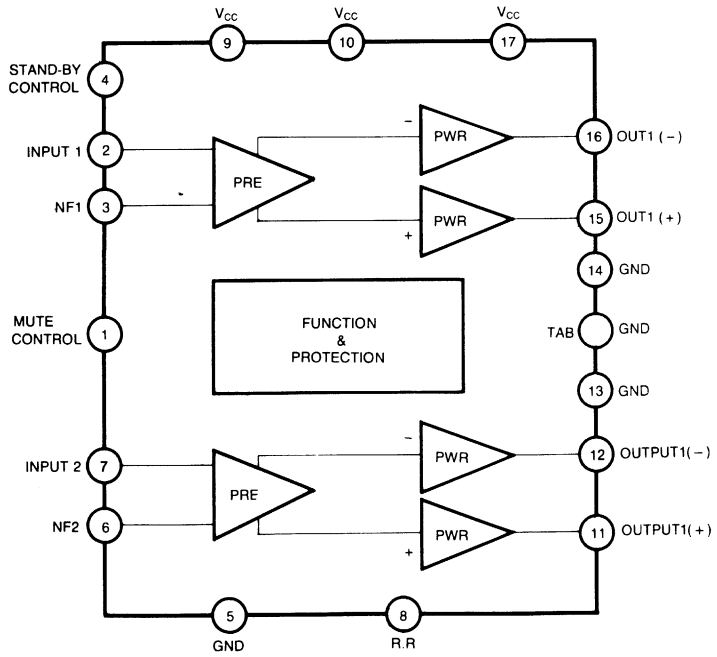


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Surge Voltage	$V_{CC\ (SURGE)}$	50	V
Supply Voltage	V_{CC}	25	V
Output Peak Current	I_{PK}	18	V
Power Dissipation	P_D	50	W
Operating Temperature	T_{OPR}	−30 ~ +85	°C
Storage Temperature	T_{STG}	−55 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 13.2V, R_L = 4Ω, f = 1KHz, Ta = 25°C)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CCQ}	V_I = 0		100	180	mA
Output Power	Po	THD = 10%	16	19		W
Total Harmonic Distortion	THD	Po = 1W		0.04	0.3	%
Closed Loop Voltage Gain	G_{VC}	R_F = 0	48	50	52	dB
Output Noise Voltage	V_{NO}	R_G = 10KΩ, BPF		0.25	1	mV
Ripple Rejection Ratio	RR	f_R = 120Hz, R_G = 0	43	50		dB
Input Resistance	R_I			30		KΩ
Output Offset Voltage	V_{OO}	V_I = 0	−80	0	+80	mV
Standby Current	I_{SB}	At stand-by		1		μA
Cross Talk	CT	R_G = 0	65	75		dB
Saturation Voltage	$V_{SAT\ (SB)}$	Pin 4, Po = 1W > 100mW	1.8	2.1	2.4	V
Saturation Voltage	$V_{SAT\ (MUTE)}$	Pin 1, Po = 1W > 100mW	1.4	1.7	3.0	V

TEST CIRCUIT

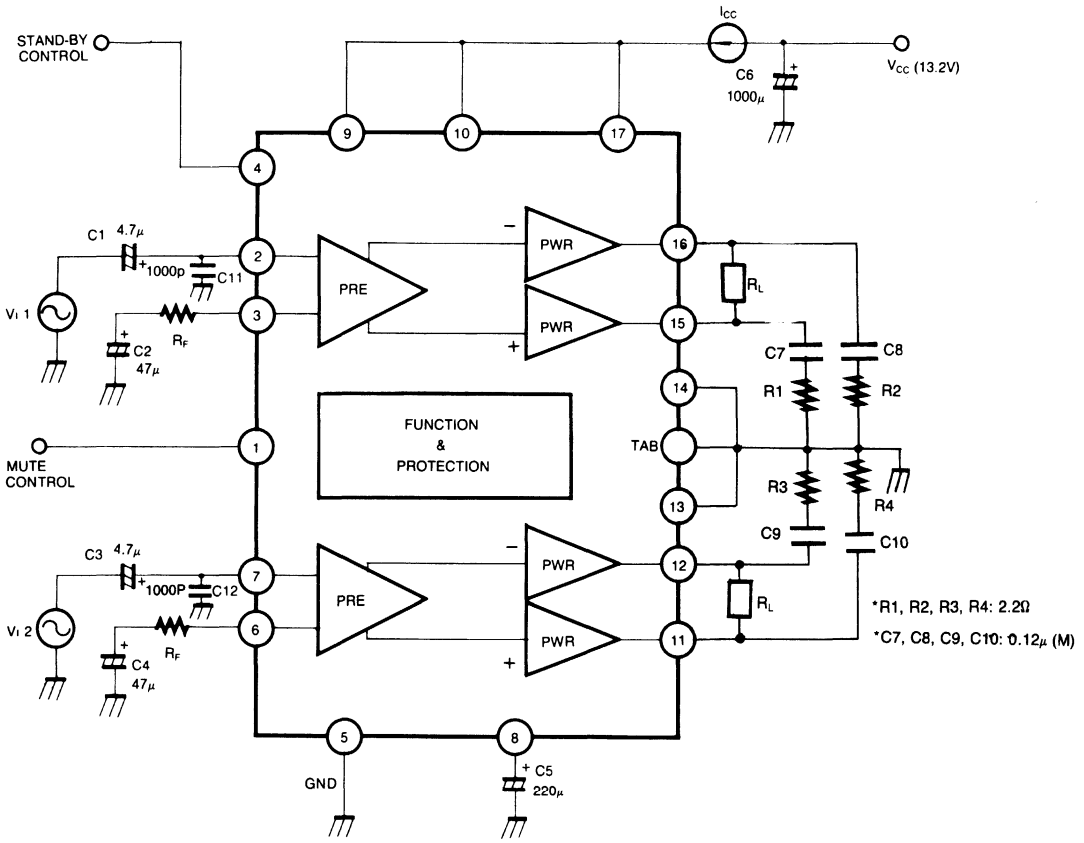


Fig. 2

APPLICATION INFORMATION

Parts	Recommended Value	Used for	Condition		Remark
			Small value	Large value	
C1, C3	4.7μF	DC coupling	Reduce the pop noise at V_{CC}-ON		Caution with gain
C2, C4	47μF	Feedback capacitor	Reduce the pop noise at V_{CC}-ON		
			Concerned with the low cut-off frequency $C2 = 1/(6.28 \times f_L = R_F)$		
C5	220μF	Reduce the ripple			
C7, C8, C9, C10	0.12μF	Compensation osc.	Easy to get oscillation	Increase the compensation	
C6	1000μF	Ripple filter	Used for ripple filter and Hum noise filter		
C11, C12	1000pF	Compensation osc	Reduction of noise increase the compensation		

FUNCTION DESCRIPTION

1. SELECTION OF FEEDBACK RESISTANCE

Since the KA22103 has a built-in pre-amp and power-amp, the amp gain is similar to the following equation.

Pre-amp gain = G_V (PRE)
Power-amp gain = G_V (PWR)
$G_V = G_V$ (PRE) + G_V (PWR)

So, that voltage gain in next equation at BTL type.
G_V total = G_V (PRE) + G_V (PWR) + 6 (dB)

Depending on the internal circuit.
G_V (PRE) = 20 log [(3.2K + R_F) / (R_F + 200)] (dB)
G_V (PWR) = 20 (dB)

So, G_V total is
G_V total = 20 log [(3.2K + R_F) / (R_F + 200)] + 20 (dB)

By using the last equation, R_F for total gain can be selected.

2. STAND-BY FUNCTION

It is available with supply voltage ON and OFF by using pin 4.
Because of the small control current, it can use a small capacitance switching relay and it can be controlled by micom directly (except the relay).
Operating voltage of pin 4 is 2.1 V typically and operating supply current is 1 μA typically in stand-by ON mode.

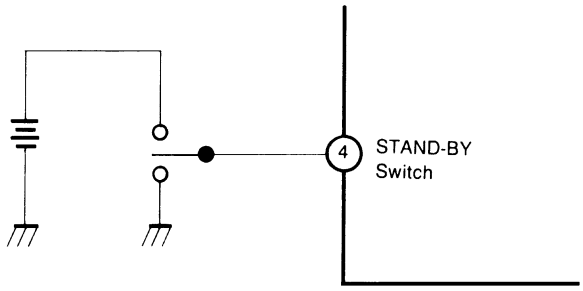


Fig. 3 STAND-BY FUNCTION

3. PREVENTION OF OSCILLATION

The sources of oscillation are listed bellow:

1. Gain of amplifier
2. Capacitance of capacitor
3. Kind of capacitor
4. Location of external components on the printed circuit board

Capacitor C4 for compensation of the OSC must use a polyester film capacitor to get better temperature and frequency variation characteristics.
Especially, if the feedback capacity is higher at low gain; the oscillation at high frequency of audio must be watched.

4. PREVENTION OF INPUT OFFSET AT V_{CC}-ON.

The input pin and negative feedback pin are the same voltage level with each pre-amp at V_{CC}-ON.
The KA22103 presses the offset voltage of the input stage and prevents pop noise of the supply voltage. So, C1 and C2 of the input stage and the NFB capacitor are varied by amp-gain.

<Example> At $G_V = 53.5$ (dB) ($R_F = 0$)
C1 = 4.7μF, C2 = 47μF
At $G_V = 40.5$dB ($R_F = 470\Omega$)
C1 = 3.3μF, C2 = 33μF.

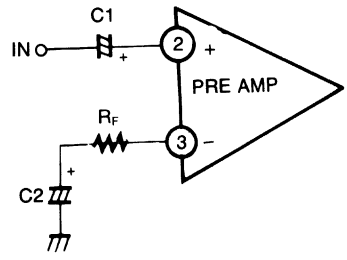


Fig. 4

5. PROTECTION CIRCUIT

The KA22103 consists of a short protection circuit between the output and GND, output-V_{CC}, output-output (each CH).

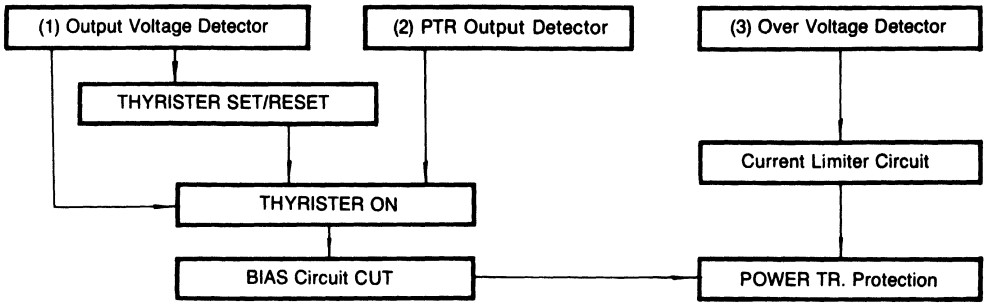


Fig. 5 FLOW CHART OF PROTECTION CIRCUIT

At Fig. 5, the output voltage detector divides the THYRISTER SET with RESET areas and sets on-mode by setting the THYRISTER circuit. When of released because of an output shortage the THYRISTER returns to the reset mode again and KA22103 is returned to the normal mode.

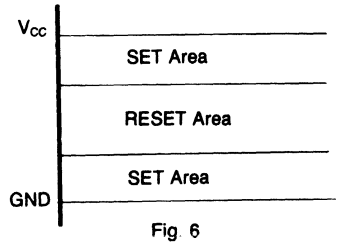


Fig. 6

6. MUTE FUNCTION

Mute is available by setting pin 1 at low level.
In Fig. 6 when the level is low, Q1 and Q2 is in turn-on and the ripple capacitor of Pin 8 is discharged. So, it cuts the bias voltage in the internal circuit. The mute attenuation radio is above 60 dB.

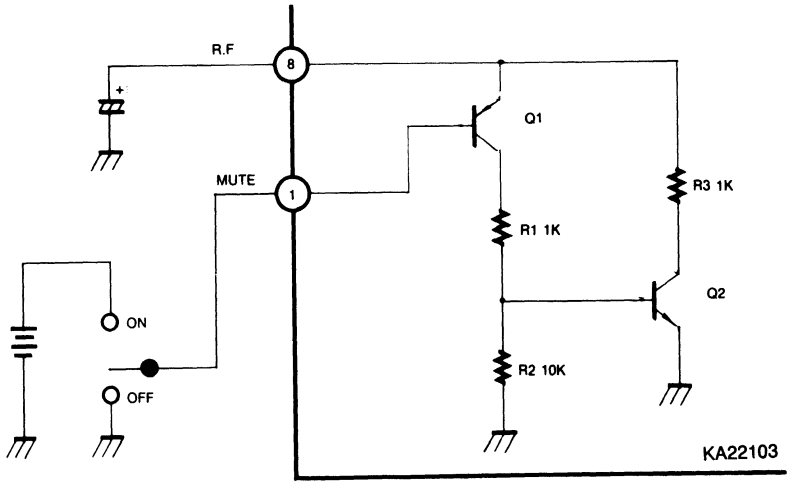
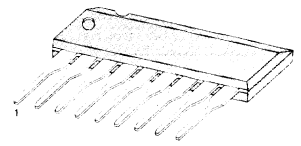


Fig. 7 MUTE Circuit

0.5W AUDIO POWER AMPLIFIER

The KA2212 is a monolithic integrated audio power amplifier in a 9-pin plastic single in line package, designed for audio frequency class B amplifiers.

9 SIP



FEATURES

- **Suitable for portable radios, cassette tape recorders.**
- **Medium output power.**
  P_O=0.5W (Typ) at V_{CC}=6V, R_L=8Ω, THD=10%.
- **Wide operating supply voltage range: V_{CC}=3.5V ~ 12V**
- **Low quiescent circuit current.**
- **Excellent thermal stability.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2212	9 SIP	−20°C ~ +70°C

BLOCK DIAGRAM

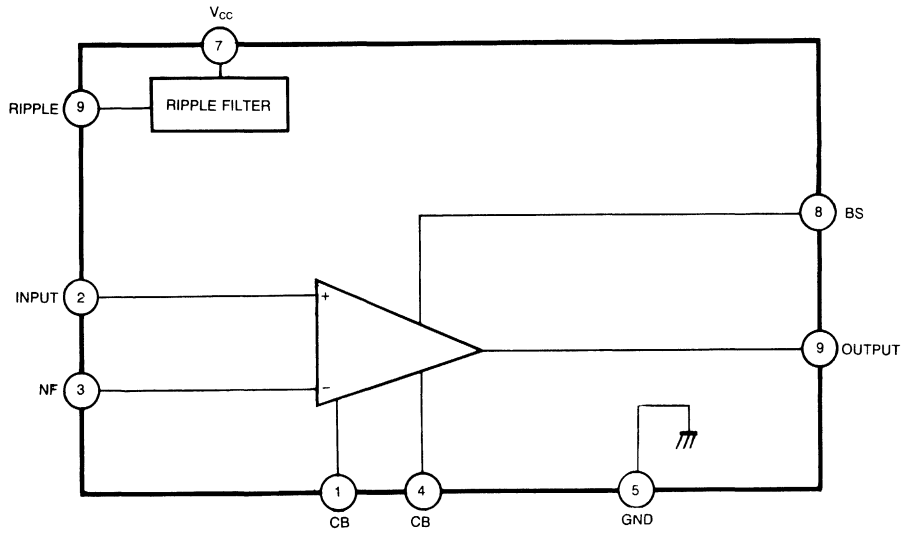


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	14	V
Power Dissipation	P_D	750	mW
Operating Temperature	T_{OPR}	−20 ~ +70	°C
Storage Temperature	T_{STG}	−40 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 6V, R_L = 8Ω, R_G = 600Ω, R_F = 68Ω, f = 1KHz, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CCQ}	V_i = 0		14		mA
Open Loop Voltage Gain	G_{VO}	R_F = 0Ω	60	75		dB
Closed Loop Voltage Gain	G_{VC}	R_F = 68Ω	47	50	52	dB
Output Power	P_O	THD=10%	0.45	0.5		W
Total Harmonic Distortion	THD	P_O = 100mW		0.3	1.0	%
Input Resistance	R_I			15		KΩ
Output Noise Voltage	V_{NO}	R_G = 10KΩ BW (−3dB)=50Hz ~ 20KHz		0.4	1.0	mV

TEST CIRCUIT

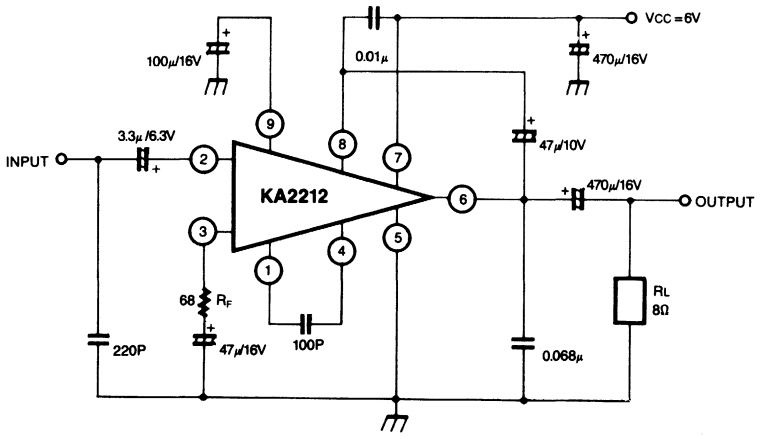
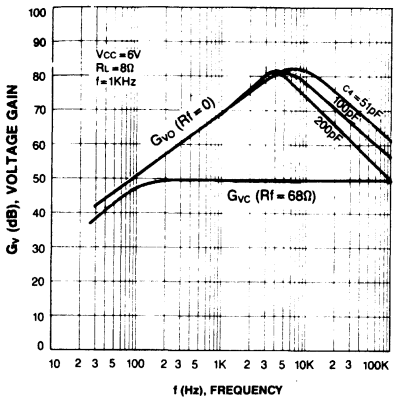
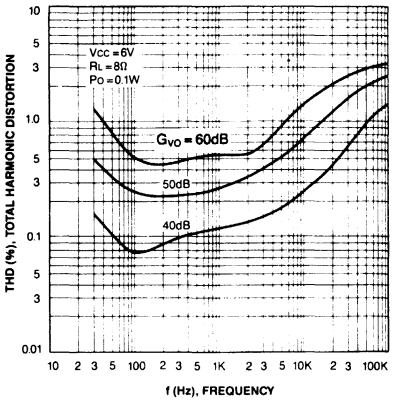


Fig. 2

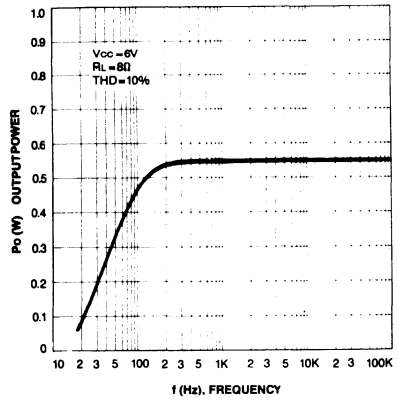
VOLTAGE GAIN-FREQUENCY



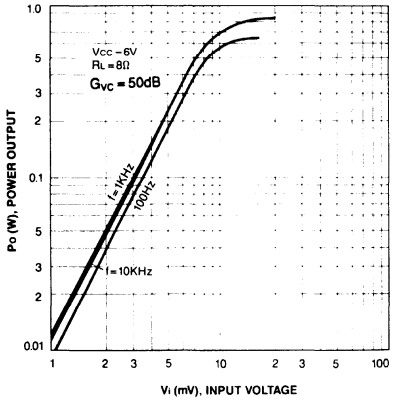
TOTAL HARMONIC DISTORTION-FREQUENCY



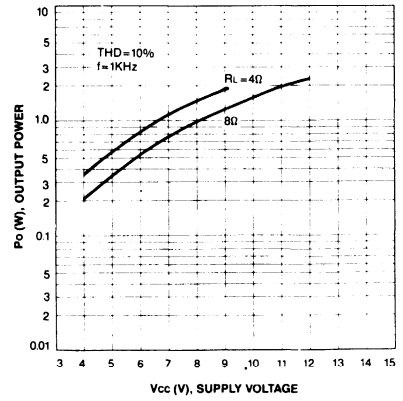
OUTPUT POWER-FREQUENCY



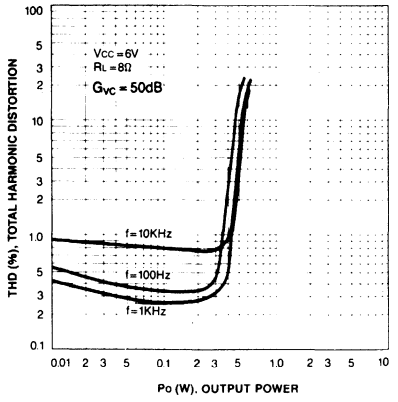
OUTPUT POWER-INPUT VOLTAGE



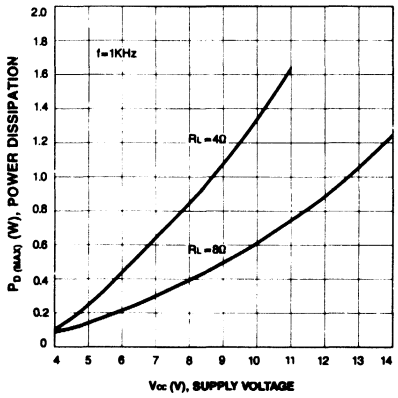
OUTPUT POWER-SUPPLY VOLTAGE



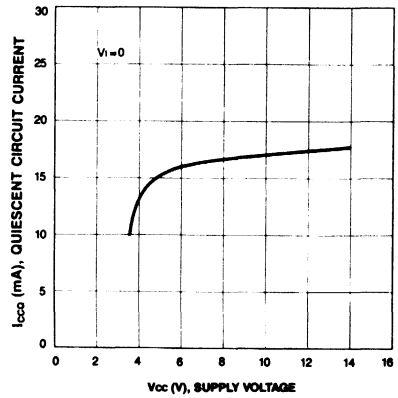
TOTAL HARMONIC DISTORTION-OUTPUT POWER



POWER DISSIPATION-SUPPLY VOLTAGE



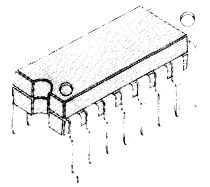
QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE



ONE-CHIP TAPE RECORDER SYSTEM

The KA2213 is a monolithic integrated circuit consisting of a preamplifier, ALC circuit, power amplifier in a 14-pin plastic dual in line package with heat sink.

14 DIP H/S



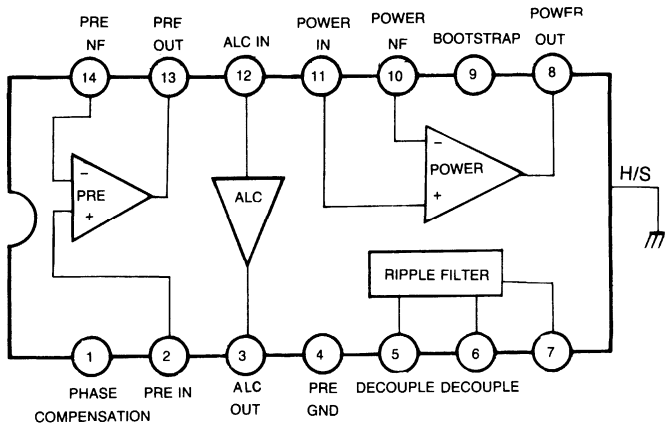
FEATURES

- Suitable for the play and recording functions of mono cassette tape recorders.
- Wide operating supply voltage range: V_{CC} = 4V ~ 12V
- **High gain preamplifier and power amplifier.**
- **Output power of power amplifier state P_O = 1W at V_{CC} = 6V, R_L = 4Ω, THD = 10%.**
- **Soft tone quality at the time of output saturation.**
- **Wide ALC range and small variation in output voltage.**
- **Small shock noise at the time of power on/off due to built-in prevention circuit.**
- **Variable monitor capability due to recording amplifier consisting of preamplifier alone.**
- **Minimum number of external parts required.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2213	14 DIP H/S	−20°C ~ +70°C

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	13	V
Power Dissipation	P_D	1.2	W
		2.25*	W
Operating Temperature	T_{OPR}	−20 ~ +70	°C
Storage Temperature	T_{STG}	−40 ~ +150	°C

* Mounted and soldered on a 50mm x 50mm copper foil of PCB

ELECTRICAL CHARACTERISTICS

(T_a = 25°C, V_{CC} = 6V, f = 1KHz, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CCQ}	V_{CC} = 6V, V_I = 0		18	30	mA
		V_{CC} = 9V, V_I = 0		23	40	mA
Pre Amplifier						
Open Loop Voltage Gain	G_{VO}	Open loop		85		dB
Closed Loop Voltage Gain	G_{VC}	Closed loop, Play		40		dB
Output Voltage	V_O	THD=1%, Play	0.9	1.2		V
Input Resistance	R_I		21	30		KΩ
Equivalent Input Noise Voltage	V_{NI}	Play		1.0	2.0	μV
ALC Input Level	$V_{I(ALC)}$	THD = 1%, Rec	−20	−12		dBm
Power Amplifier						
Closed Loop Voltage Gain	G_{VC}	R_F = 51Ω	43	45	47	dB
Output Power	P_O	V_{CC} =6V, R_L =4Ω, THD=10%	0.7	1.0		W
		V_{CC} =7.5V, R_L =4Ω, THD=10%	1.0	1.5		W
		V_{CC} =9V, R_L =4Ω, THD=10%	1.7	2.2		W
Total Harmonic Distortion	THD	P_O =250mW		0.3	1.5	%
Input Resistance	R_I			30		KΩ
Output Noise Voltage	V_{NO}	R_G = 10KΩ		0.6	1.8	mV
Ripple Rejection Ratio	RR	R_G = 0Ω, V_R =150mV, f =100Hz	40	45		dB

TEST CIRCUIT

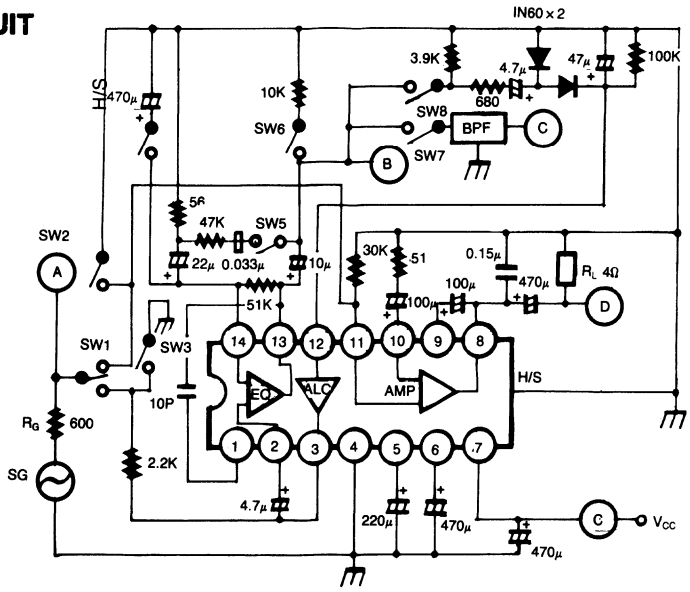


Fig. 2

TEST METHOD

Characteristic		SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	Test Point	Test Method
Power Amplifier	I_{CCQ}		on	on	off	on	on	off	off		Test circuit current
	G_{VC}	2	off	off	off	on	on	off	off	A.D	$G_{VC} = 20 \log V_O/V_I$ (dB)
	P_O	2	off	off	off	on	on	off	off	D	Test output voltage at THD = 10%
	THD	2	off	off	off	on	on	off	off	D	Test THD at output voltage $V_O = 1V$
	V_{NO}		on	off	off	on	on	off	off	D	Test output noise voltage
	RR		on	off	off	on	on	off	off	D	RR = 20 log V_{RO}/150 (dB) Test output ripple voltage (V_{RO})
Pre-Amplifier	G_{VO}	1	off	off	on	off	on	off	off	A.B	$G_{VO} = 20 \log V_O/V_I$ (dB)
	V_O	1	off	off	off	on	on	off	off	B	Test output voltage at THD = 1%
	V_{NI}		off	on	off	on	on	on	off	C	Convert output noise voltage at $R_G = 2.2K\Omega$, $V_{NI} = V_{NO}/G_V$
	$V_{I\,(ALC)}$	1	off	off	off	off	off	off	on	A.B	Test input voltage at THD = 1%

TYPICAL APPLICATION CIRCUITS

1. Mono cassette tape recorder

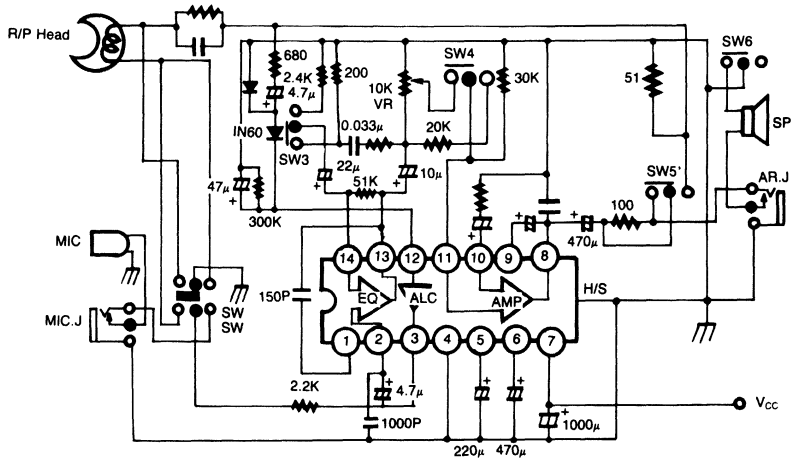


Fig. 3

2. Radio cassette tape recorder

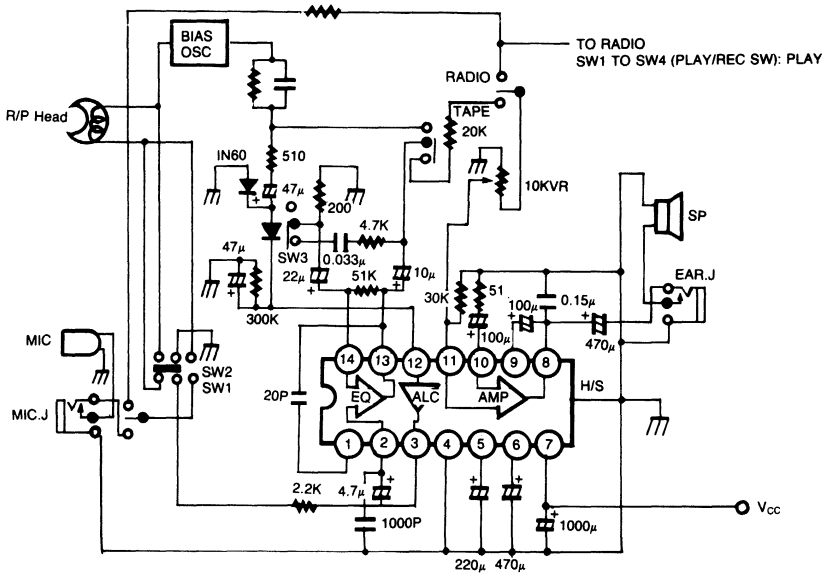
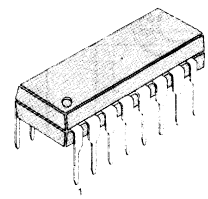


Fig. 4

ONE CHIP TAPE RECORDER SYSTEM

The KA22130 is a monolithic integrated circuit consisting of preamplifier, ALC circuit, power amplifier in 16 pin plastic dual in line package.

16 DIP



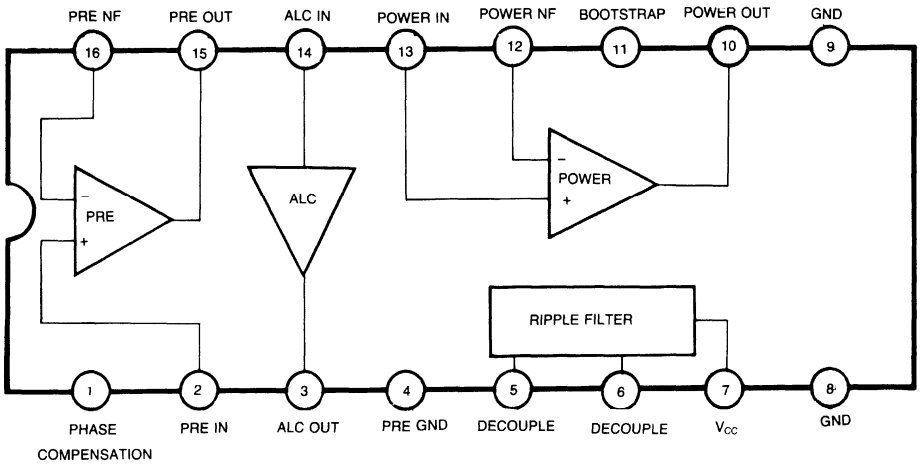
FEATURES

- **Suitable for play and recording mono cassette tape recorder.**
- **Wide operating supply voltage range: V_{CC} = 4V ~ 12V**
- **High gain preamplifier and power amplifier.**
- **Output power of power amplifier state P_O = 1W at V_{CC} = 6V, R_L = 4Ω, THD = 10%.**
- **Soft tone quality at the time of output saturation.**
- **Wide ALC range and small variation in output voltage.**
- **Small shock noise at the time of power on/off due to built-in prevention circuit.**
- **Variable monitor capability due to recording amplifier consisting of preamplifier alone.**
- **Minimum number of external parts required.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA22130	16 DIP	−20°C ~ 70°C

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	13	V
Power Dissipation	P_D	1.5	W
Operating Temperature	T_{OPR}	−20 ~ +70	°C
Storage Temperature	T_{STG}	−40 ~ +150	°C

ELECTRICAL CHARACTERISTIC

(T_a = 25°C, V_{CC} = 6V, f = 1KHz, unless otherwise specified)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CCQ}	V_{CC} = 6V, V_I = 0		18	30	mA
		V_{CC} = 9V, V_I = 0		23	40	mA
Pre Amplifier						
Open Loop Voltage Gain	G_{VO}	Open loop		85		dB
Closed Loop Voltage Gain	G_{VC}	Closed loop, Play		40		dB
Output Voltage	V_O	THD = 1%, Play	0.9	1.2		V
Input Resistance	R_I		21	30		KΩ
Equivalent Input Noise Voltag	V_{NI}	Play		1.0	2.0	μV
ALC Input Level	$V_{I(ALC)}$	THD = 1%, Rec	−20	−12		dBm
Power Amplifier						
Closed Loop Voltage Gain	G_{VC}	R_F = 51Ω	43	45	47	dB
Output Power	P_O	V_{CC} = 6V, R_L = 4Ω, THD = 10%	0.7	1.0		W
		V_{CC} = 7.5V, R_L = 4Ω, THD = 10%	1.0	1.5		W
		V_{CC} = 9V, R_L = 4Ω, THD = 10%	1.7	2.2		W
Total Harmonic Distortion	THD	P_O = 250mW		0.3	1.5	%
Input Resistance	R_I			30		KΩ
Output Noise Voltage	V_{NO}	R_G = 10KΩ		0.6	1.8	mV
Ripple Rejection Ratio	RR	R_G = 0Ω, V_R = 150mV, f = 100Hz	40	45		dB

TEST CIRCUIT

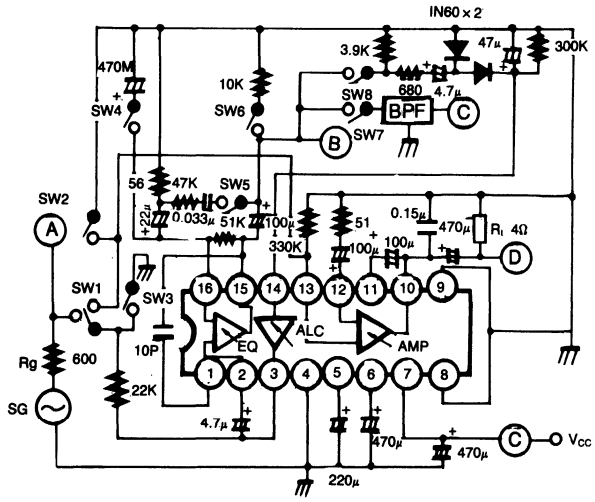


Fig. 2

TEST METHOD

Characteristic		SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	Test Point	Test Method
Power Amplifier	I_{CCQ}		on	on	off	on	on	off	off		Test circuit current
	G_{VC}	2	off	off	off	on	on	off	off	A.D.	$G_{VC} = 20 \log V_O/V_I$ (dB)
	P_O	2	off	off	off	on	on	off	off	D	Test output voltage at THD = 10%
	THD	2	off	off	off	on	on	off	off	D	Test THD at output voltage V_O = 1V
	V_{NO}		on	off	off	on	on	off	off	D	Test output noise voltage
	RR		on	off	off	on	on	off	off	D	RR = 20 log V_{RO}/150 (dB) Test output ripple voltage (V_{RO})
Pre Amplifier	G_{VO}	1	off	off	on	off	on	off	off	A.B	$A_{VO} = 20 \log V_O/V_I$ (dB)
	V_O	1	off	off	off	on	on	off	off	B	Test output voltage at THD = 1%
	V_{NI}		off	on	off	on	on	on	off	C	Convert output noise voltage at R_G = 2.2KΩ, $V_{NI} = V_{NO}/G_V$
	$V_{I(ALC)}$	1	off	off	off	off	off	off	on	A.B	Test input voltage at THD = 1%

APPLICATION CIRCUIT

1. Mono cassette tape recorder

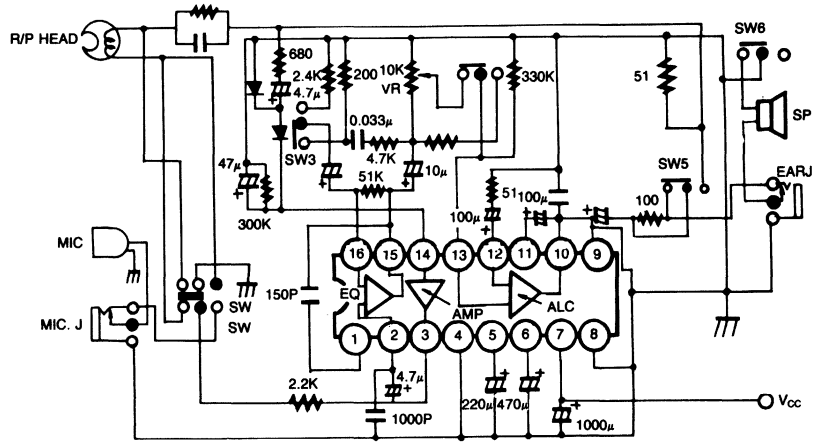


Fig. 3

2. Radio cassette tape recorder

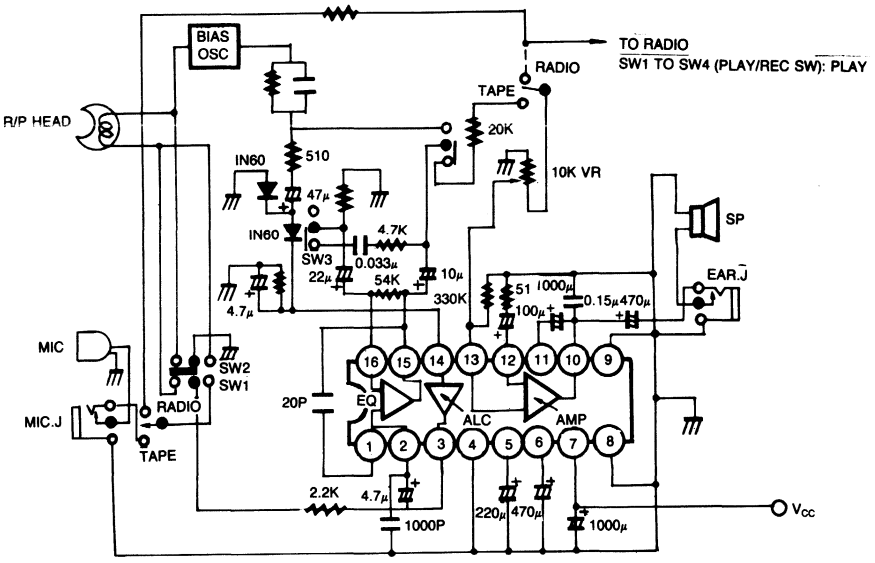
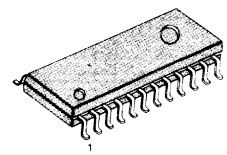


Fig. 4

DUAL PRE-POWER AMPLIFIER FOR AUTO REVERSE

The KA22131 is a monolithic integrated circuit consisting of an autoreverse dual pre and power amplifier. It is suitable for 3V portable radio cassettes with an auto-reverse function.

24 SOP



FEATURES

- **Dual pre-power amplifier on 1 chip**
- **Auto-reverse switch included**
- **Muting circuit included for Metal/Normal gain control**
- **LED drive circuit included for tape direction indication**
- **Power ON muting circuit inclued for suppression of shock-noise at the power ON time.**
- **Operating supply voltage range: V_{CC} = 1.8V ~ 3.6V**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA22131D	24 SOP	-20°C ~ +70°C

BLOCK DIAGRAM

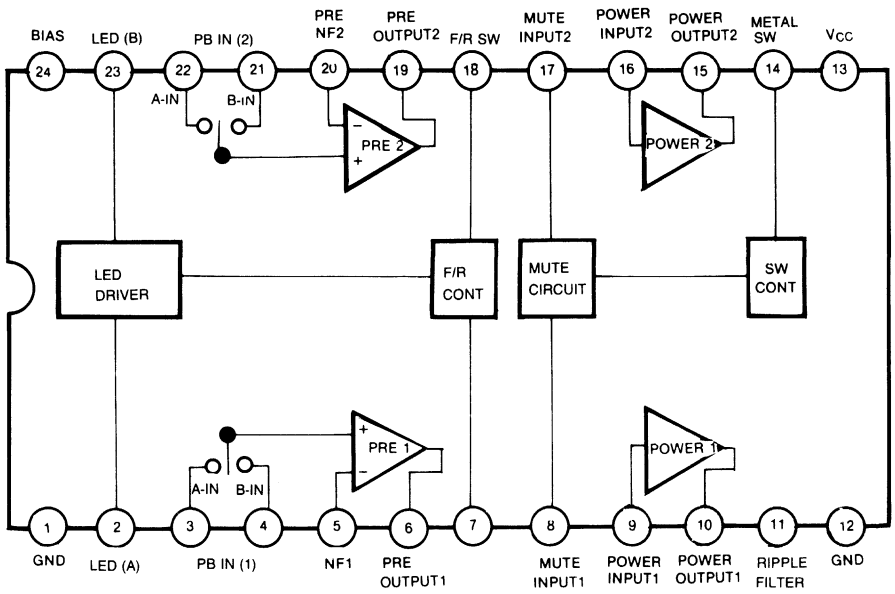


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	4.5	V
Power Dissipation	P_D	600	mW
Operating Temperature	T_{OPR}	−20 ~ +70	°C
Storage Temperature	T_{STG}	−55 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 3V, f = 1KHz, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CCQ}	V_I = 0V, Pin 14, 18: Open	4	9	15	mA
PRE-AMP (R_L = 10KΩ)						
Open Loop Voltage Gain	G_{VO}	V_o = −10dBm	72	83		dB
Output Voltage	V_o	THD = 1%	300	450		mV
Total Harmonic Distortion	THD	V_o = 0.2V, NAB = 33dB		0.03	0.08	%
Equivalent Input Noise Voltage	V_{NI}	R_G = 2.2KΩ BW(−3dB) = 20Hz ~ 20KHz		0.9	1.2	μV
Ripple Rejection Ratio	RR	V_R = −20dBm, f = 100Hz NAB = 33dB	43	53		dB
FWD-REV Cross Talk	CT_{F-R}	V_O = −10dBm, R_G = 2.2KΩ BW = 20Hz ~ 20KHz	65	75.5		dB
Input Bias Current	I_{BIAS}	V_I = 0V		130	500	nA
POWER-AMP (R_L = 16Ω)						
Output Power	P_o	THD = 10%	50	69		mW
Closed Loop Voltage Gain	G_{VC}	V_I = −40dBm	24.6	26.6	28.6	dB
Total Harmonic Distortion	THD	P_o = 1mW		0.27	0.5	%
Output Noise Voltage	V_{NO}	R_G = 0Ω, BW (−3dB) = 20Hz ~ 20KHz		27	39	μV
Ripple Rejection Ratio	RR	V_R = −20dBm, f = 100Hz, R_G = 0Ω	45	61		dB
Input Resistance	R_I		21.4	30	38.6	KΩ
Input Bias Current	I_{BIAS}	V_I = 0V, R_G = 100KΩ		10	90	nA
Channel Balance	CB	V_o = −10dBm		0.1	0.7	dB
LED Maximum Current	$I_{DR\ (MAX)}$	$V_{CE\ (SAT)}$ = 0.3V	5			mA
PRE + POWER AMP						
L-R Cross Talk	CT_{L-R}	VR: Max, PRE: R_G = 2.2KΩ BW = 20Hz ~ 20KHz, Power: V_o = −5dBm	40	48		dB
Signal Leakage	S_{LKG}	PRE: V_o = −12dBm VR: Min		−66	−60	dBm

TEST CIRCUIT

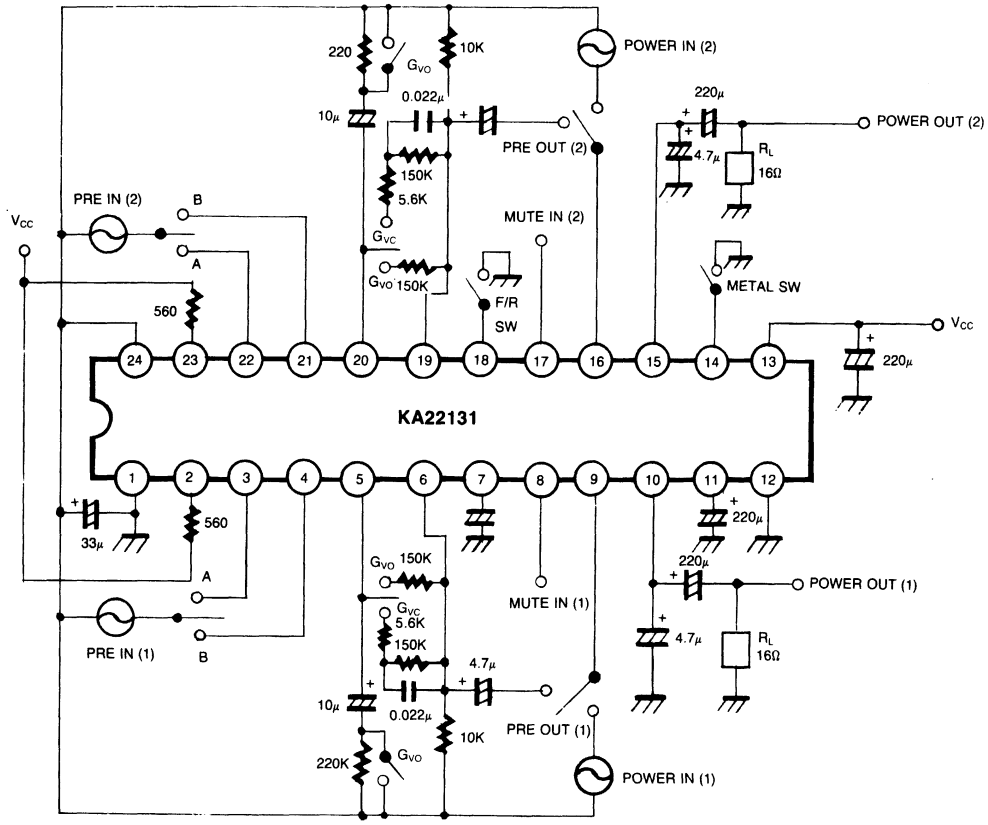


Fig. 2

APPLICATION CIRCUIT

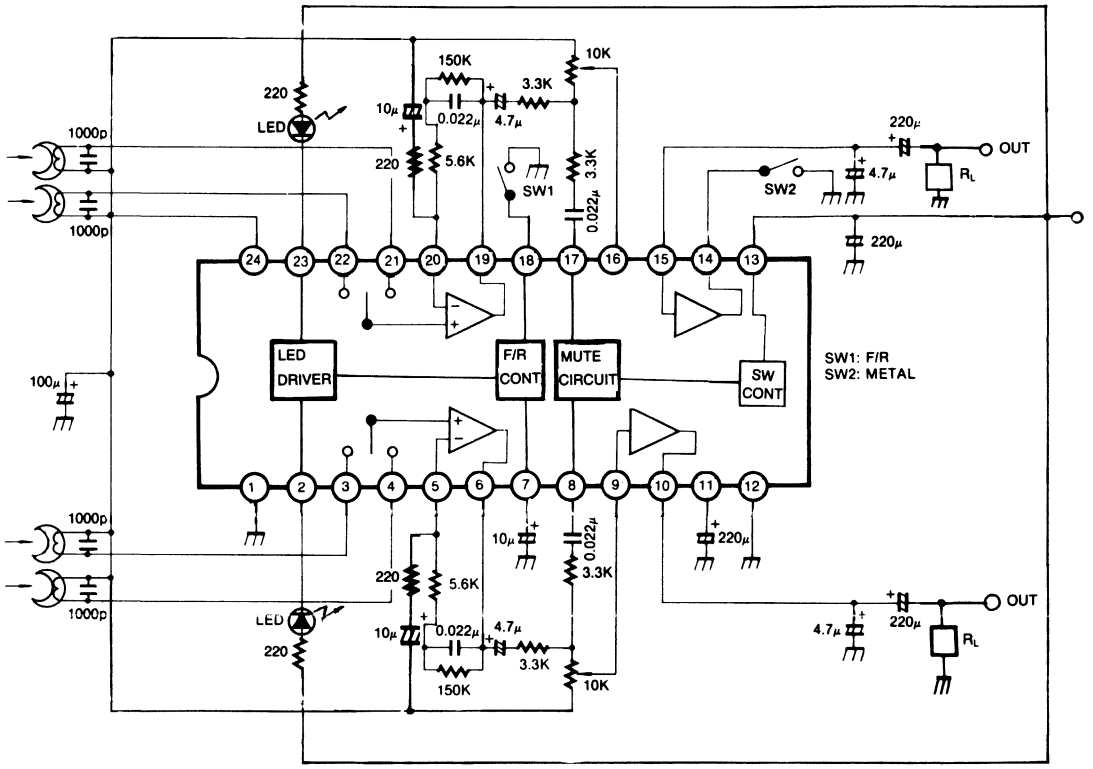


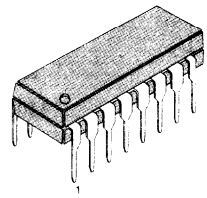
Fig. 3

DUAL PRE-POWER AMPLIFIER WITH DC VOLUME CONTROL

The KA22134 is a monolithic integrated circuit designed for use in low voltage and low power applications. It has all functions including a dual audio pre-power amplifier, DC volume control and headphone drive circuits.

It is suitable for portable tape recorders or headphone cassette recorders.

16 DIP



FEATURES

- **Built-in DC volume control circuit.**
- **Wide operation supply voltage: V_{CC} = 1.8 ~ 6V**
- **Only a few components to build headphone cassette tape recorders.**
- **Built-in ripple filter.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA22134	16 DIP	−20°C ~ +75°C

BLOCK DIAGRAM

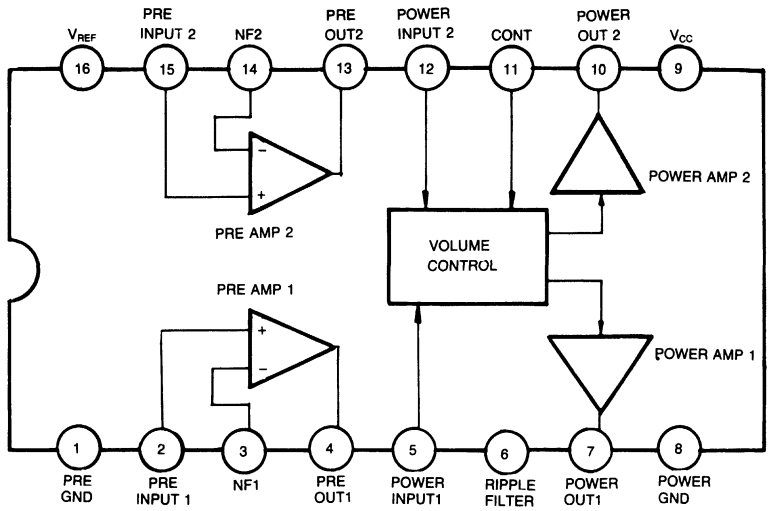


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	7	V
Power Dissipation	P_D	75Ω	mW
Operating Temperature	T_{OPR}	−20 ~ +75	°C
Storage Temperature	T_{STG}	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 3V, Ta = 25°C)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CCQ1}	V_I = 0, V_{OL} = MIN		9	13	mA
	I_{CCQ2}	V_I = 0, V_{OL} = MAX		11.0		mA
Cross Talk	CT	R_G = 2.2KΩ, V_O = −10dBm	34	40		dB

PRE-AMPLIFIER SECTION

(V_{CC} = 3V, Ta = 25°C, f = 1KHz, R_{L1} = 10KΩ, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Open Loop Voltage Gain	G_{VO}	V_I = 0.2mV	55	62		dB
Closed Loop Voltage Gain	G_{VC1}	V_O = −10dBm, NAB 1KHz		33		dB
Output Voltage	V_O	THD = 1%	600	720		mV
Total Harmonic Distortion	THD_1	V_O = −10dBm		0.04	0.1	%
Ripple Rejection Ratio	RR_1	R_G = 2.2KΩ V_R = −20dBm, f_R = 100Hz		46		dB
Equivalent Input Noise Voltage	V_{NI}	R_G = 2.2KΩ, BW = 30 ~ 20KHz Gain for NAB 1KHz		1.2	2.0	μV

POWER AMPLIFIER SECTION

(V_{CC} = 3V, Ta = 25°C, f = 1KHz, R_{L2} = 32Ω, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Power	P_{O1}	THD_2 = 10%	20	27		mW
	P_{O2}	THD_2 = 10%, R_L = 16Ω		39		mW
Total Harmonic Distortion	THD_2	P_O = 10mW, Volume: 100%		0.5	1.2	%
	THD_3	P_O = 10mW, Volume: 50%		0.3		%
Closed Loop Voltage Gain	G_{VC2}	V_O = −10dBm, Volume: 100%	28	30	32	dB
	G_{VC3}	V_O = −10dBm		15		dB
Channel Balance	CB	V_O = −10dBm	−1.5	0	−1.5	dB
Volume Rejection Ratio	VOL_{REJ}	V_O = −10dBm, Volume: 100% to 0%	66	72		dB
Output Noise Voltage	V_{NO}	BW = 30 − 20KHz, R_G = 600Ω		250	320	μV
Ripple Rejection Ratio	RR_2	R_G = 600Ω, f_R = 100Hz V_R = −20dBm		46		dB

TEST CIRCUIT

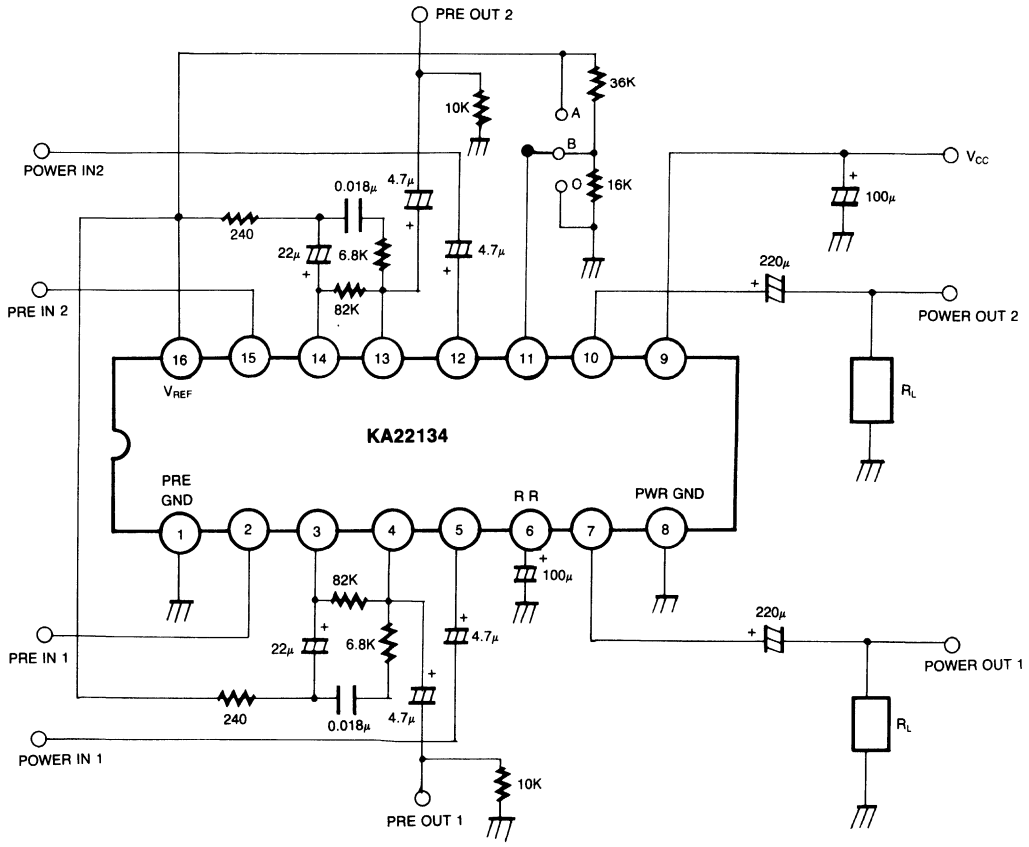


Fig. 2

APPLICATION CIRCUIT

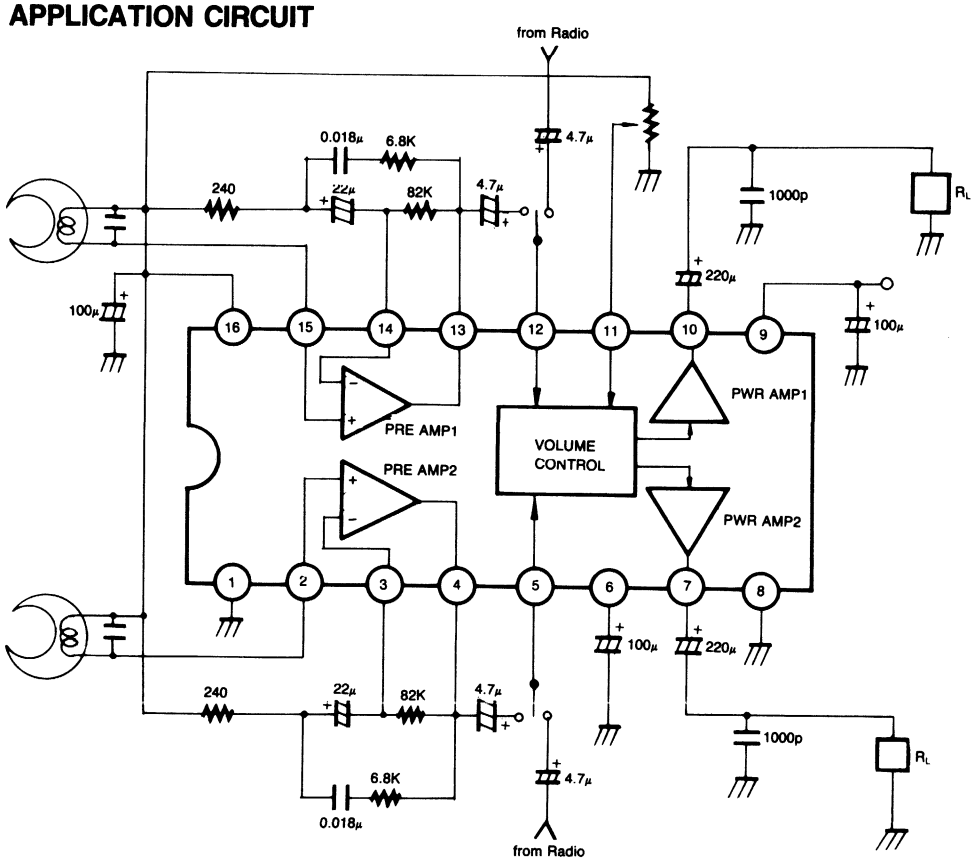
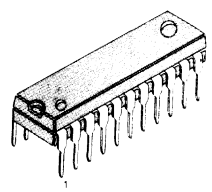


Fig. 3

DUAL PRE-POWER AMPLIFIER AND DC MOTOR SPEED CONTROLLER

The KA22135 is a monolithic integrated circuit designed for use in low voltage and low power applications. It has all functions including a dual audio pre-power amplifier and motor speed controller in a single chip. It is suitable for portable tape recorders, head phone cassette tape recorders or battery-powered radios.

22 SDIP



FEATURES

- **Low current consumption in a operating voltage range.**
- **Wide operating supply voltage range; V_{CC} = 2V ~ 7.5V.**
- **Only a few components to build headphone cassette tape recorders.**
- **Dual audio pre-power amplifier and motor speed controller in a single chip.**
- **Reduced input and output coupling capacitors because of 1/2 V_{CC} AMP adoption on chip as AC GND.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA22135	22 SDIP	-20°C ~ +70°C

BLOCK DIAGRAM

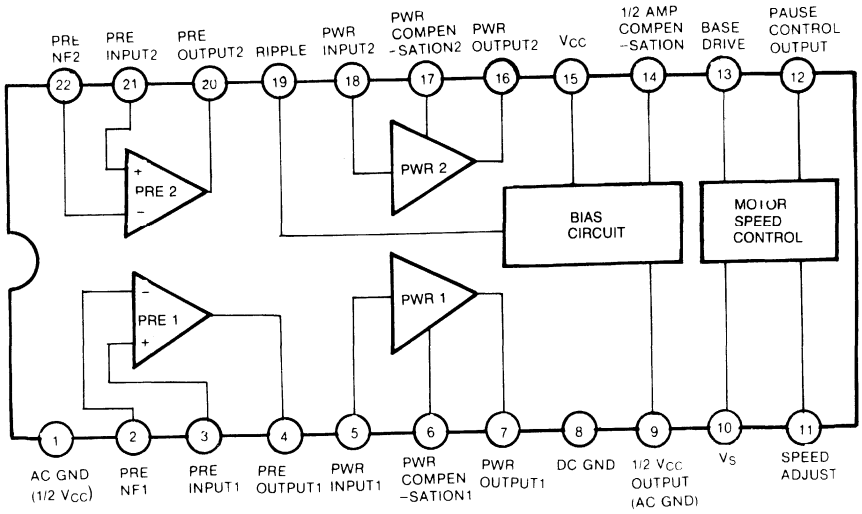


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	10	V
Power Dissipation	P_D	600	mW
Operating Temperature	T_{OPR}	−20 ~ +70	°C
Storage Temperature	T_{STG}	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS (Ta = 25°C)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CCQ}	V_{CC} = 3V, V_I = 0, I_M = 0mA		15	25	mA

PRE AMPLIFIER SECTION
(Ta = 25°C, V_{CC} = 3V, f = 1KHz, R_{L1} = 10KΩ, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Open Loop Voltage Gain	G_{VO}	V_O = −10dBm, R_L = ∞		72		dB
Closed Loop Voltage Gain	G_{VC}	V_o = −10dBm	40	42	44	dB
Output Voltage	V_o	THD = 1%	0.35	0.6		V
Total Harmonic Distortion	THD	V_o = 400mV		0.05	0.5	%
Output Noise Voltage	V_{NO}	V_I = 0, R_G = 2.2KΩ BW(−3dB) = 30Hz ~ 20KHz		70	300	μV
Input Resistance	R_I	V_o = −10dBm	18	22		KΩ
Cross Talk	CT	R_G = 2.2KΩ, V_O = −10dBm	45	62		dB

POWER AMPLIFIER SECTION
(Ta = 25°C, V_{CC} = 3V, f = 1KHz, R_{L2} = 32Ω, unless otherwise specified)

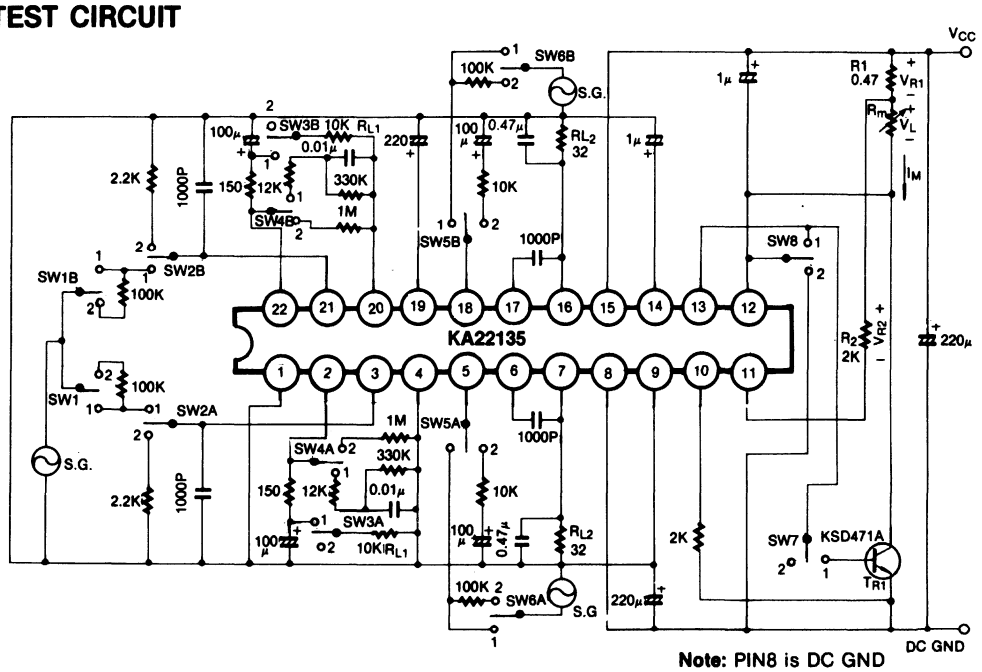
Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Closed Loop Voltage Gain	G_{VC}	P_o = 5mW	26	28	30	dB
Output Power	P_o	THD = 10%	20	28		mW
Total Harmonic Distortion	THD	P_o = 5mW		0.2	2.0	%
Output Noise Voltage	V_{NO}	R_G = 10KΩ, BW (−3dB) = 30Hz ~ 20KHz		0.25	1.0	mV
Input Resistance	R_I	P_o = 5mW	10	20		KΩ
Cross Talk	CT	P_O = 5mW, R_G = 10KΩ	35	50		dB

MOTOR SPEED CONTROLLER SECTION

(Ta = 25°C, V_{CC} = 3V, I_M = 10umA, unless otherwise specified)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Base Driving Current	I_B		10	18		mA
Reference Voltage	V_{REF}		0.22	0.26	0.30	V
Reference Voltage Regulation 1	ΔV_{REF1}	V_{CC} = 2.0 ~ 6.5V		0.05		%/V
Reference Voltage Regulation 2	ΔV_{REF2}	I_M = 25 ~ 200mA		0.1		%/mA
Reference Voltage Regulation 3	ΔV_{REF3}	Ta = −10 ~ +60°C		0.01		%/°C
Current Coefficient	K	$K = \frac{V_L - V_{R2}}{V_{R1} + V_{R2}}$	3.7	4	4.3	
Current Coefficient Regulation 1	ΔK_1	V_{CC} = 2.0 ~ 6.5V		0.05		%/V
Current Coefficient Regulation 2	ΔK_2	I_M = 25 ~ 200mA		0.1		%/mA
Current Coefficient Regulation 3	ΔK_3	Ta = −10 ~ +60°C		0.1		%/°C

TEST CIRCUIT



Note: PIN8 is DC GND
PIN9 is AC GND

Fig. 2

TEST METHOD

TEST ITEM \ SWITCH		SW1 A/B	SW2 A/B	SW3 A/B	SW4 A/B	SW5 A/B	SW6 A/B	SW7	SW8
I_{CCQ}		1	2	1	1	2	1	1	2
Pre-Amplifier	CH1 G_{VO}	"	1	2	2	"	"	"	"
	CH1 G_{VC}	"	"	1	1	"	"	"	"
	CH1 V_O	"	"	"	"	"	"	"	"
	CH1 THD	"	"	"	"	"	"	"	"
	CH1 V_{NO}	"	2	"	"	"	"	"	"
	CH1 R_I	2	1	"	"	"	"	"	"
	CH2 G_{VO}	1	2	"	"	"	"	"	"
	CH2 G_{VC}	"	"	"	"	"	"	"	"
	CH2 V_O	"	"	"	"	"	"	"	"
	CH2 THD	"	"	"	"	"	"	"	"
	CH2 V_{NO}	"	"	"	"	"	"	"	"
	CH2 R_I	"	"	"	"	"	"	"	"
	CT_1 (2→1)	"	"	"	"	"	"	"	"
	CT_2 (1→2)	"	1	"	"	"	"	"	"
Power-Amplifier	CH1 G_V	"	2	"	"	"	"	"	"
	CH1 P_O		"	"	"	"	"	"	"
	CH1 THD	"	"	"	"	"	"	"	"
	CH1 V_{NO}	"	"	"	"	2	"	"	"
	CH1 R_I	"	"	"	"	1	2	"	"
	CH2 G_V	"	"	"	"	2	1	"	"
	CH2 P_O	"	"	"	"	"	"	"	"
	CH2 THD	"	"	"	"	"	"	"	"
	CH2 V_{NO}	"	"	"	"	"	"	"	"
	CH2 R_I	"	"	"	"	"	"	"	"
	CT_1 (2→1)	"	"	"	"	"	"	"	"
	CT_2 (1→2)	"	"	"	"	1	"	"	"
M.S.C	I_B	"	"	"	"	2	"	2	1
	V_{REF}	"	"	"	"	"	"	1	"
	ΔV_{REF}	"	"	"	"	"	"	"	"
	K	"	"	"	"	"	"	"	"
	ΔK	"	"	"	"	"	"	"	"

APPLICATION CIRCUIT

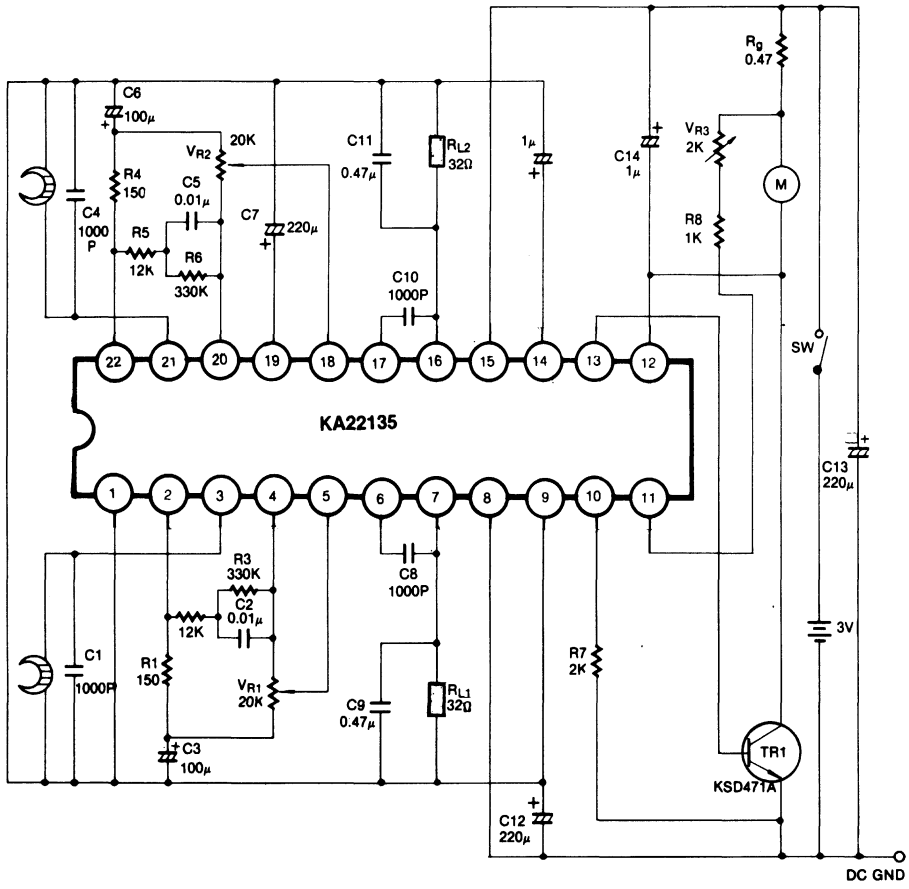


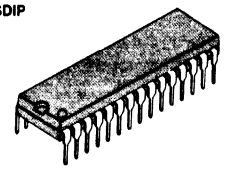
Fig. 3

Note: 1. For C12, use a capacitor of Low TANδ
2. For C9 and C11, use solid state capacitors with better characteristics at low temperature
3. Locate C7 just around the emitter TR1; KSD471A.

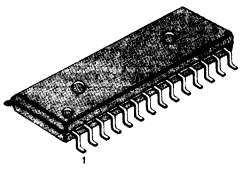
DUAL PRE-POWER AMPLIFIER, VOLUME CONTROLLER AND DC MOTOR SPEED CONTROLLER

The KA22136 is a molithic integrated circuit designed for use in low voltage and low power applications. It has all functions including dual audio pre-power amplifier, electronic volume controller and DC motor speed controller in a single chip. It is suitable for portable tape recorders headphone cassette tape recorders or radios by batteries.

28 SDIP



28 SOP



FEATURES

- **Low current consumption in a operating voltage range.**
- **Operating supply voltage range: V_{CC} = 2.1V ~ 5V**
- **Only a few components in composing headphone cassette tape recorder.**
- **Dual audio pre-power amplifier, electronic volume controller and DC motor speed controller in a single chip.**
- **Reduced input and output coupling capacitors because of ½ V_{CC} AMP adoption on chip as AC GND.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA22136	28SDIP	-20°C ~ +65°C
KA22136D	28SOP	

BLOCK DIAGRAM

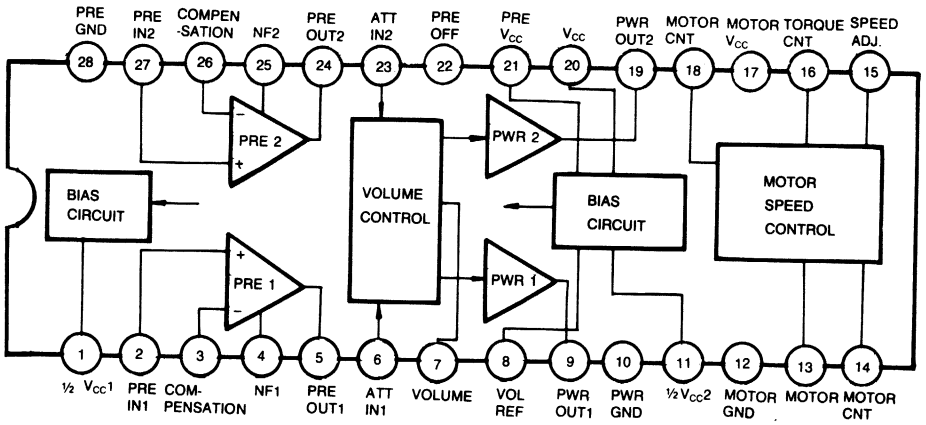


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	7.5	V
Power Dissipation	P_D	450	mW
Operating Temperature	T_{OPR}	−20 ~ +70	°C
Storage Temperature	T_{STG}	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 3V, unless otherwise specified)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Quiescent circuit current	I_{CCQ}	V_{CC} = 3V, V_I = 0, I_M = 0		18	25	mA

PRE AMPLIFIER SECTION (V_{CC} = 3V, f = 1KHz, R_{L1} = 10KΩ, unless otherwise specified)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Open Loop Voltage Gain	G_{VO}	V_O = −10dBm, R_L = ∞		72		dB
Closed Loop Voltage Gain	G_{VC1}	V_O = −10dBm	40	42	44	dB
Output Voltage	V_O	THD = 10%	0.45	0.6		V
Total Harmonic Distortion	THD_1	V_O = 400mV		0.05	0.5	%
Output Noise Voltage	V_{NO1}	V_i = 0, R_g = 2.2KΩ, BPF (30 ~ 20KHz)		150	300	μV
Input Resistance	R_I	Vo = 10dBm	18	22		KΩ
Cross Talk	CT_1	R_G = 2.2KΩ, V_O = −10dBm	30			dB
Output Voltage In Pre OFF	$V_{O(OFF)}$	V_I = 100mV Pre OFF (pin 22) = V_{CC}			−50	dB

POWER AMPLIFIER SECTION (Ta = 25°C, V_{CC} = 3V, f = 1KHz, R_L2 = 16Ω, unless otherwise specified)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Closed Loop Voltage Gain	G_{VC2}	Po = 5mW	26	28	30	dB
Voltage Gain Difference	ΔG_V	V_{CONT} = Max		0	3	dB
Output Power 1	P_{O1}	THD = 10%, R_L = 32Ω	20	28		mW
Output Power 2	P_{O2}	THD = 10%, R_L = 16Ω	30			mW
Total Harmonic Distortion	THD_2	Po = 5mW		0.2	2.0	%
Pre + Power Output Noise Voltage	V_{NO2}	V_I = 0, R_G = 2.2KΩ, V_{CONT} = Max		6	10	mV
Output Noise Voltage	V_{NO3}	R_G = 2.2KΩ, V_{CONT} = Min		0.25	1.0	mV
Cross Talk	CT_2	Po = 5mW	20	30		dB
Ripple Rejection Ratio	RR	Vcc = 3V, 100Hz, 100mVp-p	34	40		dB

ATTENUATOR SECTION (Ta = 25°C, V_{CC} = 3V, f = 1KHz, unless otherwise specified)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Maximum Input Voltage	$V_{I\,(MAX)}$		0.2			V
Maximum Attenuation	$V_{ATT\,(MAX)}$	V_{CONT} = Min	66			dB
Attenuation Error	$V_{ATT\,(ERR)}$	V_{CONT} = Max		0		dB
Input Impedance	Z_I		15	20		KΩ

MOTOR SPEED CONTROLLER (Ta = 25°C, V_{CC} = 3V, I_M = 100mA, unless otherwise specified)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Circuit Current	I_{CCQ}			3.0	5.0	mA
Starting Current	I_{ST}		500			mA
Reference Voltage	V_{REF}	V (pin 15, 16)	0.72	0.80	0.87	V
Reference Voltage Regulation 1	ΔV_{REF1}	* V_{CC} = 2.1 ~ 5.0V		0.05		%/V
Reference Voltage Regulation 2	ΔV_{REF2}	I_M = 25 ~ 250mA		0.01		%/mA
Reference Voltage Regulation 3	ΔV_{REF3}	Ta = − 10 ~ 50°C		0.01		%/°C
Current Coefficient	K		32	38	43	
Current Coefficient Regulation 1	ΔK_1	V_{CC} = 2.1 ~ 5.0V		0.50		%/V
Current Coefficient Regulation 2	ΔK_2	I_M = 25 ~ 250mA		0.05		%/mA
Current Coefficient Regulation 3	ΔK_3	Ta = − 10 ~ 50°C		0.02		%/°C
Saturation Voltage	V_{SAT}	I_M = 200mA, Pin14 = V_{CC}			0.6	V
Leakage Current	I_{LKG}	Pin 18 = V_{CC}		50	200	μA

*Voltage across Pin 13, 17

TEST CIRCUIT

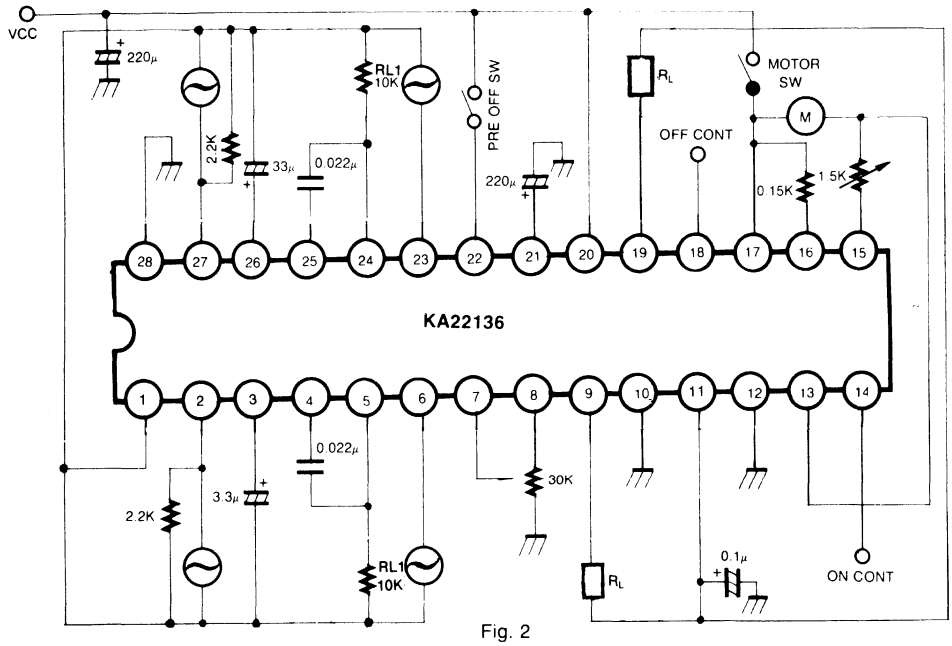


Fig. 2

APPLICATION CIRCUIT

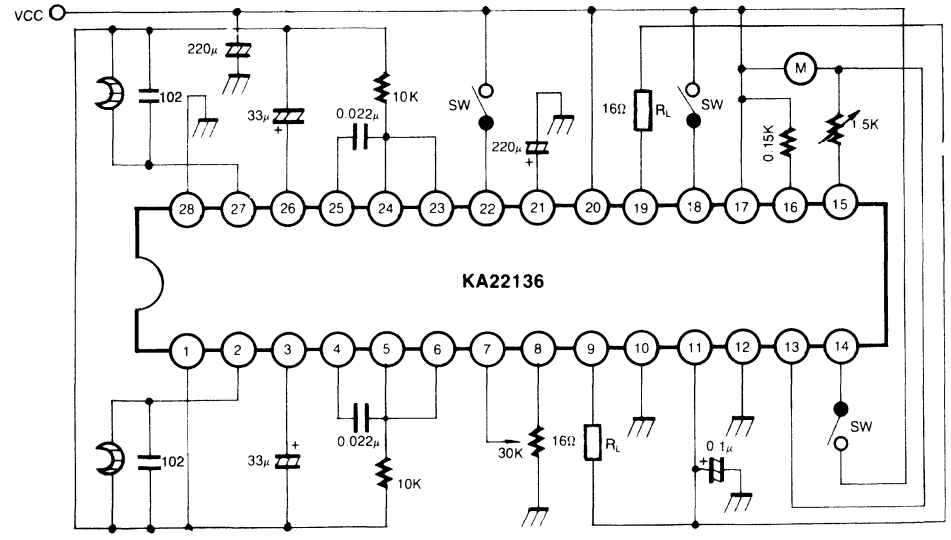
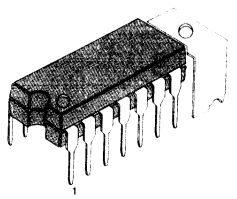


Fig. 3

1.2W DUAL POWER AMPLIFIER

The KA2214 is a monolithic integrated dual audio power amplifier in a 14-pin plastic dual in line package. It is designed for portable audio sets.

14 DIP H/S



FEATURES

- **Wide operating supply voltage range: V_{CC} = 3V ~ 13V**
- **Output power: P_O = 1.2W at 9V/8Ω/THD = 10%**
  P_O = 1.6W at 9V/4Ω/THD = 10%
  P_O = 2W at 12V/8Ω/THD = 10%
- **Good ripple rejection ratio: 50dB (Typ)**
- **Low quiescent circuit current: 10mA (V_{CC} = 9V)**
- **Minimum number of external parts required**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2214	14 DIP H/S	- 20°C ~ + 70°C

BLOCK DIAGRAM

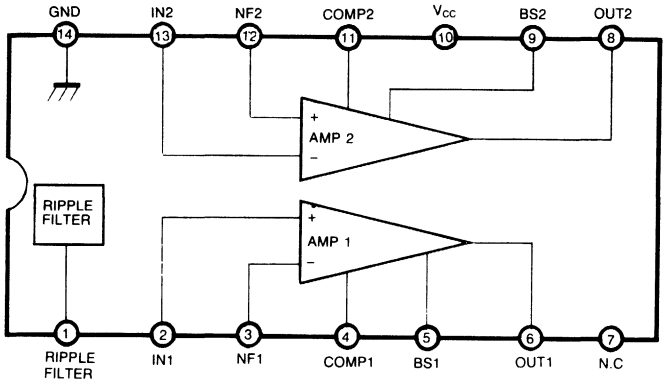


Fig. 1.

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage (No Signal)	V_{CC}	18	V
Supply Voltage (Operating)	V_{CC}	16	V
Power Dissipation ·	P_D	2.4	W
Operating Temperature	T_{OPR}	− 20 ~ + 70	°C
Storage Temperature	T_{STG}	− 40 ~ + 150	°C

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 9V, R_F = 33Ω, f = 1KHz, R_L = 8Ω, R_G = 600Ω, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CCQ}	V_I = 0		10		mA
Voltage Gain	G_{V1}	P_O = 0.25W, R_F = 33Ω		44		dB
	G_{V2}	P_O = 0.25W, R_F = 120Ω		34		dB
Output Power	P_{o1}	V_{CC} = 12V, R_L = 8Ω, THD = 10%		2		W
	P_{o2}	V_{CC} = 9V, R_L = 4Ω, THD = 10%		1.6		W
	P_{o3}	V_{CC} = 9V, R_L = 8Ω, THD = 10%	0.9	1.2		W
	P_{o4}	V_{CC} = 6V, R_L = 4Ω, THD = 10%		0.7		W
	P_{o5}	V_{CC} = 6V, R_L = 8Ω, THD = 10%		0.5		W
	P_{o6}	V_{CC} = 4.5V, R_L = 32Ω, THD = 10%		50		mW
Total Harmonic Distortion	THD_1	P_O = 0.5W, R_F = 33Ω		0.8		%
	THD_2	P_O = 0.5W, R_F = 120Ω		0.4		%
Output Noise Voltage	V_{NO}	R_G = 10KΩ, BW (− 3dB) = 20Hz ~ 20KHz		0.6		mV
Ripple Rejection Ratio	RR	R_G = 0, f = 120Hz, V_R = 0.3V		50		dB
Cross Talk	CT	R_G = 0, P_O = 0.25W		55		dB
Channel Balance	CB	P_o = 0.25W	− 2	0	2	dB
Input Resistance	R_I			5		MΩ

APPLICATION CIRCUIT

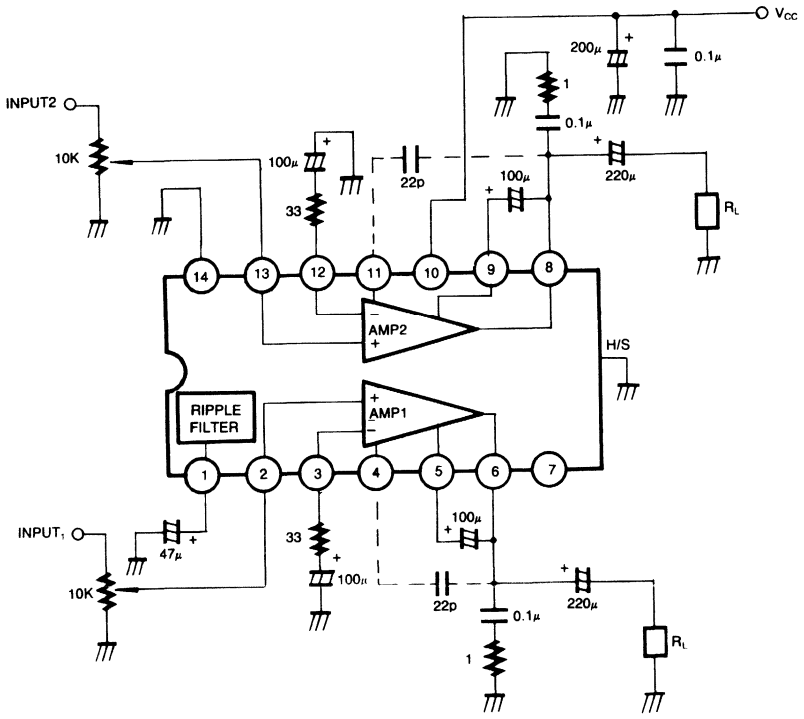
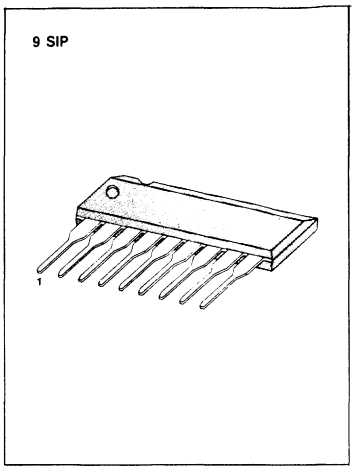


Fig. 2

EQUALIZER AMPLIFIER WITH ALC

The KA2220 is a monolithic integrated circuit consisting of a preamplifier and ALC circuit for cassette tape recorders.



FEATURES

- **Low noise amplifier.**
- **Wide operating supply voltage range: V_{CC} = 3.5V ~ 14V**
- **High output voltage.**
- **Low distortion.**
- **Wide ALC range.**
- **KA2220 ST: Good ALC pair characteristic for stereo tape recorders**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2220	9 SIP	-20°C ~ +70°C

BLOCK DIAGRAM

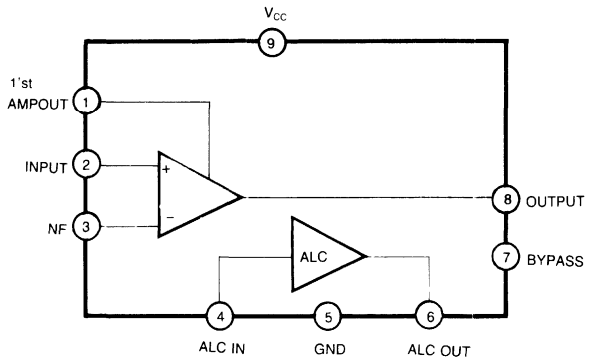


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	15	V
Power Dissipation	P_D	200	mW
Operating Temperature	T_{OPR}	−20 ~ +70	°C
Storage Temperature	T_{STG}	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 5V, R_L = 5.1KΩ, R_G = 600Ω, f = 1KHz, NAB, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CCQ}	V_I = 0, ALC OFF		1.4	2.0	mA
Open Loop Voltage Gain	G_{VO}		66	69		dB
Closed Loop Voltage Gain	G_{VC}	V_O = 0.7V	33	35	37	dB
Output Voltage	V_O	THD = 1%	0.7	1.0		V
Total Harmonic Distortion	THD	V_O = 0.2V		0.1		%
Input Resistance	R_I		60	100		KΩ
Equivalent Input Noise Voltage	V_{NI}	R_G = 2.2KΩ, NAB BW (−3dB) = 15Hz ~ 30KHz		1.0		μV
ALC Transistor Saturation Voltage	V_{SAT}			75	100	mV

TEST CIRCUIT

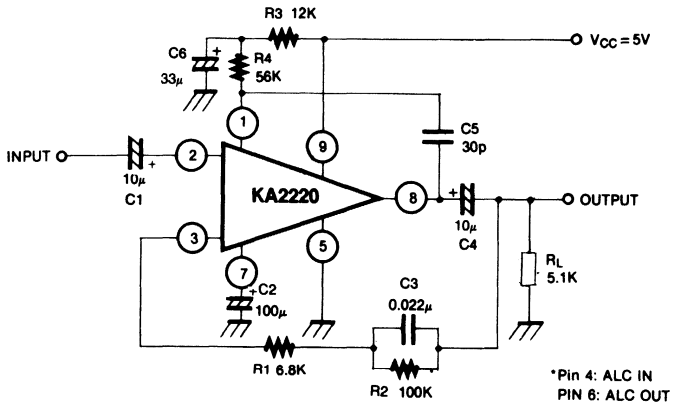
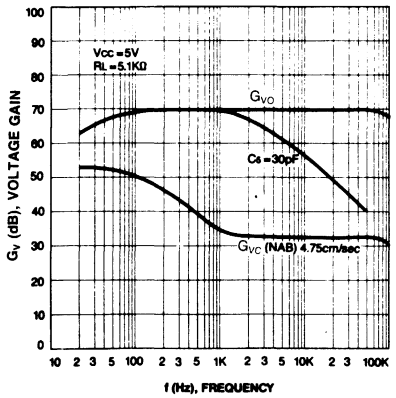
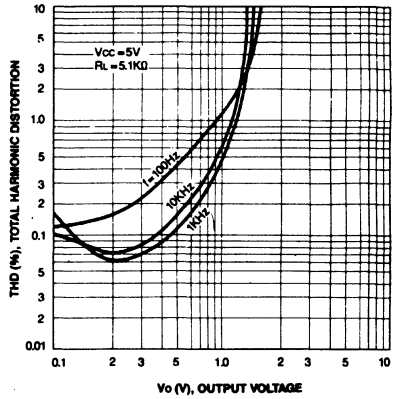


Fig. 2

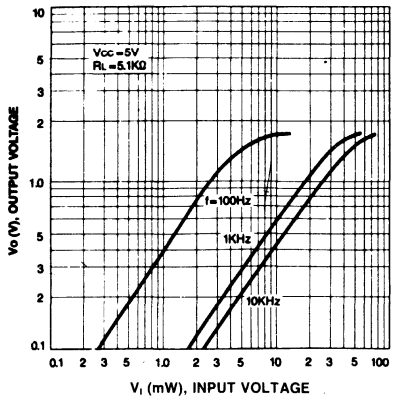
VOLTAGE GAIN-FREQUENCY



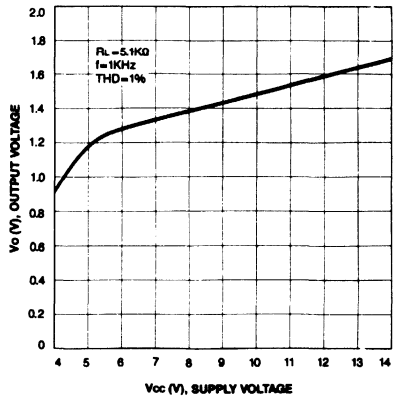
TOTAL HARMONIC DISTORTION-OUTPUT VOLTAGE



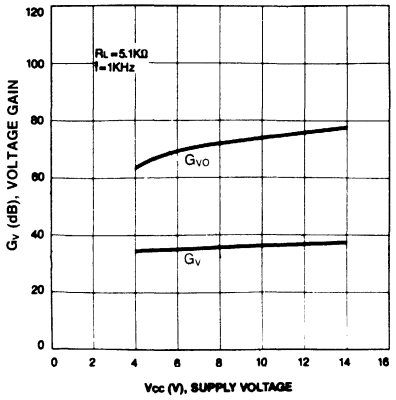
OUTPUT VOLTAGE-INPUT VOLTAGE



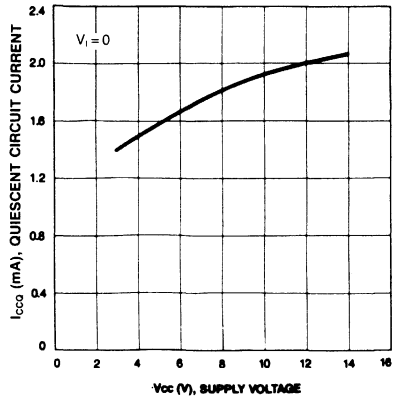
OUTPUT VOLTAGE-SUPPLY VOLTAGE

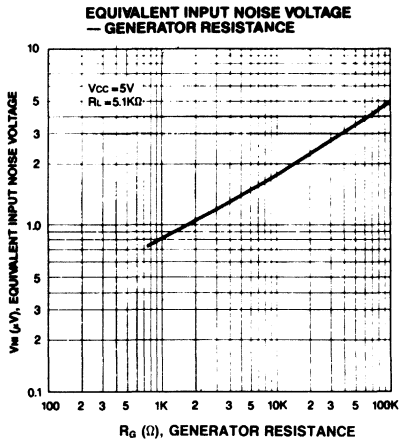


VOLTAGE GAIN-SUPPLY VOLTAGE



QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE





APPLICATION INFORMATION
ACL Grade Binning Table

Symbol	A_V (dB)		ALC Grade (dB)	
	Min	Max	Min	Max
KA2220 J	34	36	-16.0	-27.0
KA2220 M			-25.0	-34.0

External Components (Refer to test circuits)

C_1: Input coupling capacitor
The recommended value is 10μF. If made too small the low frequency characteristics will change for the worse, and too large a capacitance value will increase the risting time when power is applied.

C_2: Bypass capacitor
Short emitter resistor on the AC and prevents an AC signal from feedback to input.

C_3, R_1, R_2: Equalizer network
The closed loop voltage gain is determined by these components in relation to the internal resistance at Pin 3.

C_4: Output coupling capacitor
C_2 is determined as follows:

$$C_4 = \frac{1}{2\pi \cdot f_L \cdot R_L}$$

f_L: low cut-off frequency
R_L: load resistance

C_5: Phase compensation capacitor.
Prevents high frequency oscillation by phase error when feedback is heavy.

C_6: Ripple filter for power supply
A large value is required to get an excellent ripple characteristic under the line operation, but must be made smaller to shorten the starting time.

R_3: Filter resistance.

R_4: Collector resistor of first stage transistor of the IC
Low voltage characteristic can be improved by adjusting this resistance.

ALC GRADE BINNING TEST CIRCUIT

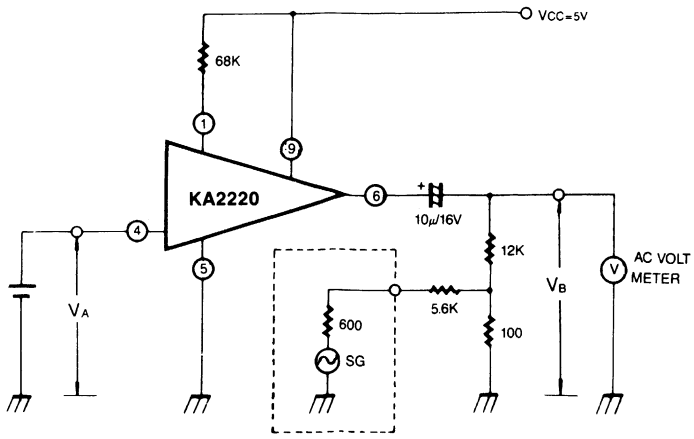


Fig. 3

Test condition: S.G output level should be adjusted to be 13.8mV of the AC voltmeter reading (V_B) when the D.U.T is not connected from the test circuit (V_{CC} = 5V, V_A = 1.16V, T_a = 25°C)
ALC RANK is defined as ALC-G.R = 20log V_{B2}/V_{B1}
where
V_{B1}: AC voltmeter reading when the D.U.T is not connected
V_{B2}: AC voltmeter reading whn the D.U.T is connected

APPLICATION CIRCUIT

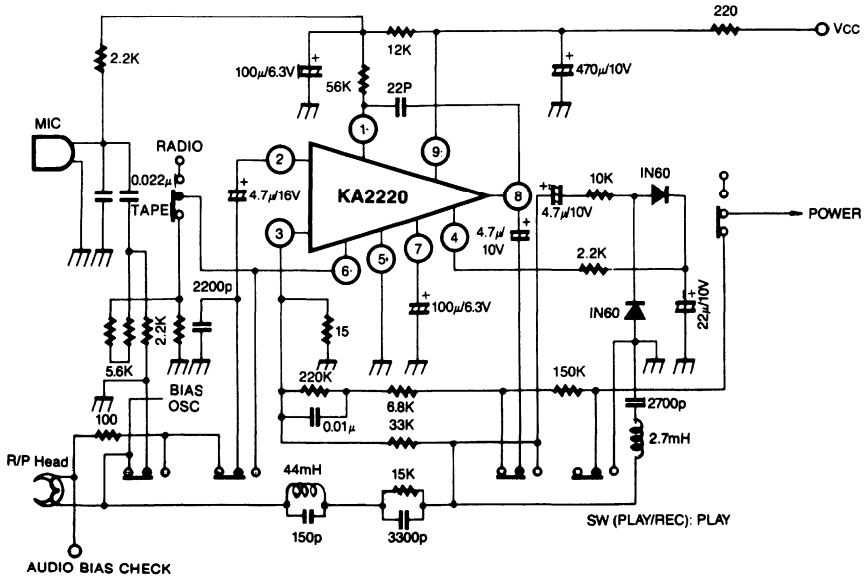
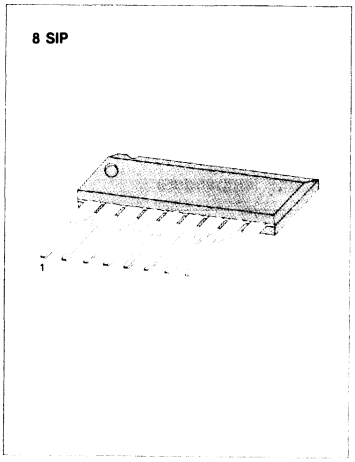


Fig. 4

DUAL LOW NOISE EQUALIZER AMPLIFIER

The KA2221 is a monolithic integrated circuit consisting of 2-channel low noise amplifiers and regulated power supply for car stereos.



FEATURES

- **Suitable for car stereos.**
- **Low noise amplifier.**
- **Voltage regulator included.**
- **Good ripple rejection.**
- **High channel separation (65dB Typ).**
- **Minimum number of external parts required.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2221	8 SIP	−20°C ~ +70°C

BLOCK DIAGRAM

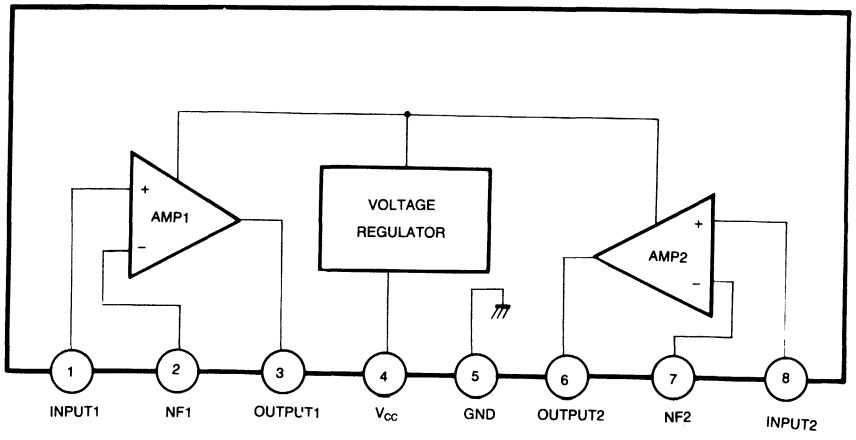


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	18	V
Power Dissipation	P_D	200	mW
Operating Temperature	T_{OPR}	−20 ~ +70	°C
Storage Temperature	T_{STG}	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(T_a = 25°C, V_{CC} =12V, R_L =10KΩ, f=1KHz, NAB, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CCQ}	V_I = 0		6.0	9.0	mA
Open Loop Voltage Gain	G_{VO}		65	80		dB
Closed Loop Voltage Gain	G_{VC}	V_O =0.5V	33	35	37	dB
Output Voltage	V_O	THD=1%	0.6	1.0		V
Total Harmonic Distortion	THD	V_O =0.5V		0.1	0.3	%
Input Resistance	R_I			150		KΩ
Equivalent Input Noise Voltage	V_{NI}	R_G = 2.2KΩ BW (−3dB) = 15Hz ~ 30KHz		1.0	2.0	μV
Cross Talk	CT	R_G = 2.2KΩ	50	65		dB

TEST CIRCUIT

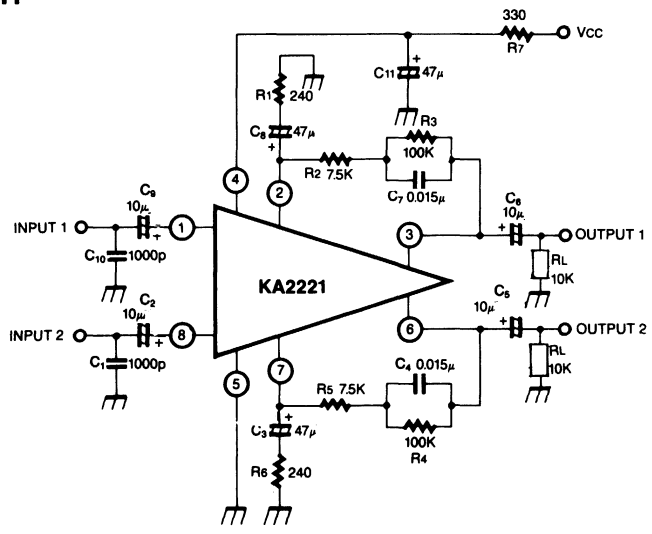
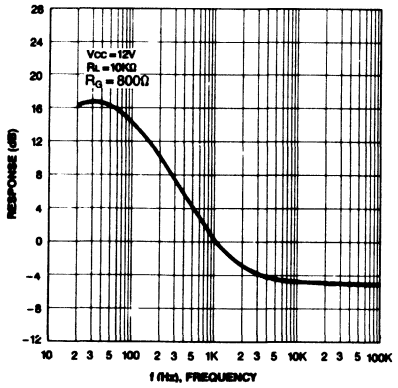
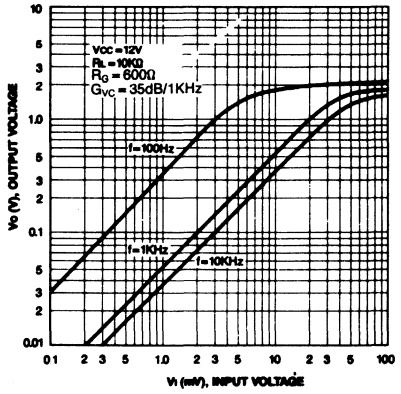


Fig. 2

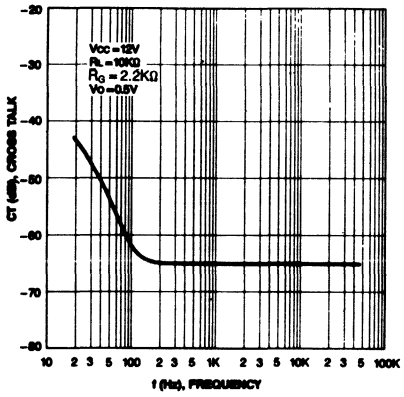
FREQUENCY RESPONSE



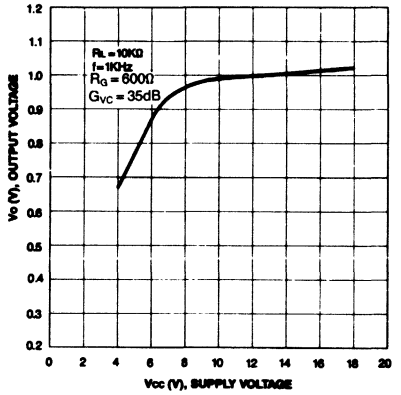
OUTPUT VOLTAGE-INPUT VOLTAGE



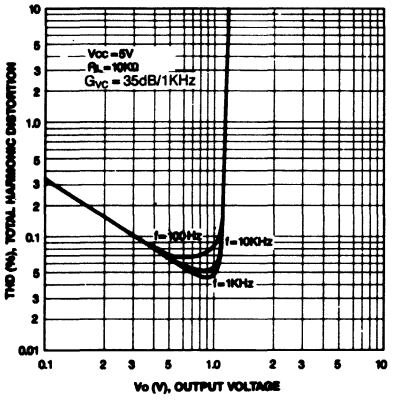
CROSS TALK-FREQUENCY



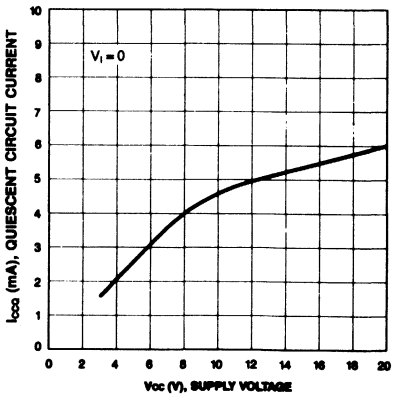
OUTPUT VOLTAGE-SUPPLY VOLTAGE



TOTAL HARMONIC DISTORTION-OUTPUT VOLTAGE



QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE



APPLICATION INFORMATION

External Components (Refer to test circuits)

C_1 (C_{10}): Noise filter
These capacitors prevent radio interference in strong electric fields. The recommended value is 1000pF.

C_2 (C_9): Input coupling capacitor
The recommended value is 10μF. If made too small, the low frequency characteristics will change for the worse, but too large a value will increase the rising time when power is applied.

C_3 (C_8): Negative feedback capacitor
The lower cut-off frequency depends on the value of these capacitors and is determined as follows:

$$C_3\ (C_8) = \frac{1}{2\pi f_L \cdot R_1\ (R_6)}$$

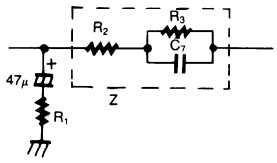
f_L: Low cut-off frequency
If the value of these capacitors is made larger, the starting time of amplifier is delayed further.

C_5 (C_6): Output coupling capacitor
The recommended value is 10μF.

R_2, R_3, C_7 (R_4, R_5, C_4): Equalizer network
The time constants of standard NAB characteristic are follow.

Tape speed	9.5cm/sec	4.75cm/sec
C_7 ($R_2 + R_3$)	3180μsec	1590μsec
R_2, C_7	90μsec	120μsec

R_1 (R_6): Feedback component
The closed loop gain is determined approximately by the following relationship.



$$G_{VC} = 20 \log \frac{Z + R_1}{R_1} \quad (dB)$$

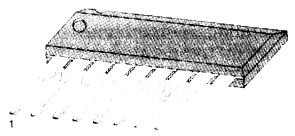
$$Z = R_2 + R_3 // C_7$$

* Choose R_2, R_3, (DC resistance of NAB element) as 100KΩ approximately.

DUAL LOW NOISE EQUALIZER AMPLIFIER

The KA22211 is a monolithic integrated circuit consisting of a 2-channel pre-amplifier in a 8-pin plastic single in-line package.

8 SIP



FEATURES

- **Recommended operating supply voltage range: V_{CC} = 5V ~ 14V**
- **Low noise (V_{NI} = 1.0μV: Typ)**
- **High channel separation**
- **Minimum number of external parts required**

SCHEMATIC DIAGRAM

ORDERING INFORMATION

Device	Package	Operating Temperature
KA22211	8 SIP	– 20°C ~ + 70°C

BLOCK DIAGRAM

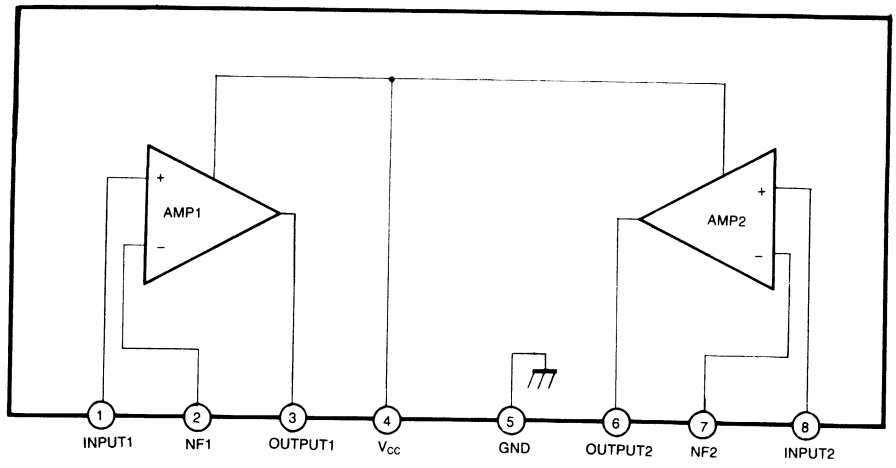


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	18	V
Power Dissipation	P_D	200	mW
Operating Temperature	T_{OPR}	−20 ~ +70	°C
Storage Temperature	T_{STG}	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 9V, R_L = 10KΩ, R_G = 600Ω, f = 1KHz, NAB, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CCQ}	V_I = 0		4.0	6.0	mA
Open Loop Voltage Gain	G_{VO}		65	80		dB
Closed Loop Voltage Gain	G_{VC}	V_o = 0.5V	33	35	37	dB
Output Voltage	V_o	THD = 1%	1.1	1.3		V
Total Harmonic Distortion	THD	V_o = 0.5V		0.1	0.3	%
Input Resistance	R_I		70	100		KΩ
Equivalent Input Noise Voltage	V_{NI}	R_G = 2.2KΩ BW (−3dB) = 15Hz ~ 30KHz		1.0	2.0	μV
Cross Talk	CT	R_G = 2.2KΩ	50	65		dB

TEST CIRCUIT

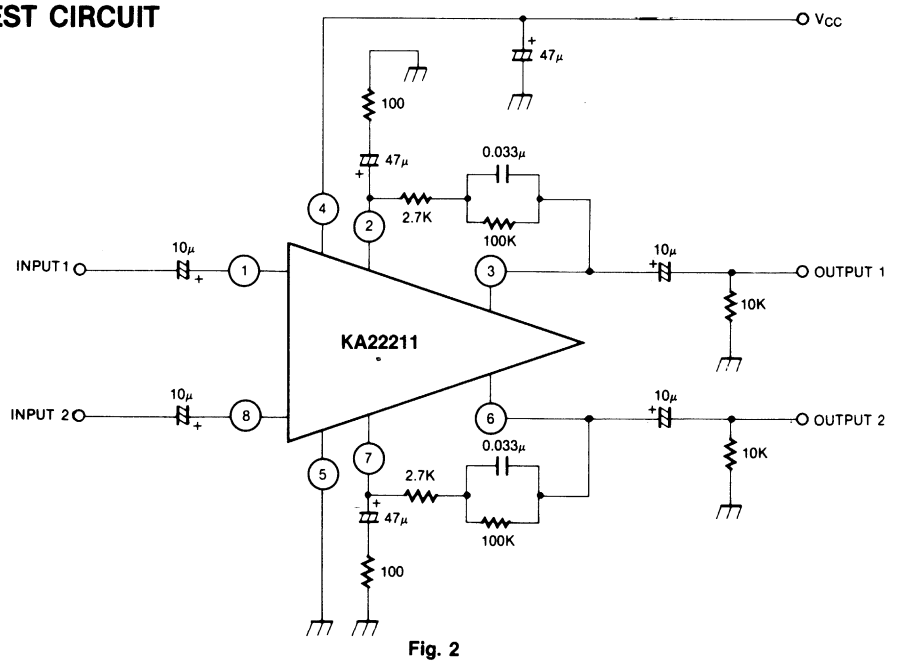


Fig. 2

APPLICATION INFORMATION

External Components

C_2 (C_9): Input coupling capacitor
These components are concerned with the output noise and operation starting time, and its capacitance is adequate for 10μF.
As C_2 (C_9) below 4.7μF extends the operation starting time, a capacitance of over 4.7μF is recommended.

C_3 (C_8): Negative feedback capacitor
These components decide the low cut-off frequency. which is determined as follows:

$$C_3\ (C_8) = \frac{1}{2\pi\ f_L \cdot R_2\ (R_7)}$$ where, f_L: low cut-off frequency.

A large C_3 (C_8) makes the operation starting time of an amplifier late. It's capacitance is adequate for 47μF.

C_4, R_3, R_2 (C_7, R_4, R_5): Equalizer network
This components decide the frequency response of an equalizer amplifier. The time constant of standard NAB characteristic is as follows:

Tape Speed / Time Constant	9.5cm/sec	4.75cm/sec
$C_4\ (R_2 + R_3)$	3,180μsec	1,590μsec
C_4, R_2	90μsec	120μsec

C_{11} Filter capacitor of the power line
This should be located as close to the supply voltage pin (Pin 4) as possible. The recommended value is 47μF:

C_1 (C_{10}): Protection capacitor
These components protect against wave damage is strong electric fields and engine noise damage and block oscillation at high amplifying operation.

C_5 (C_6): Output coupling capacitor
The recommended value is 10μF.

APPLICATION CIRCUIT

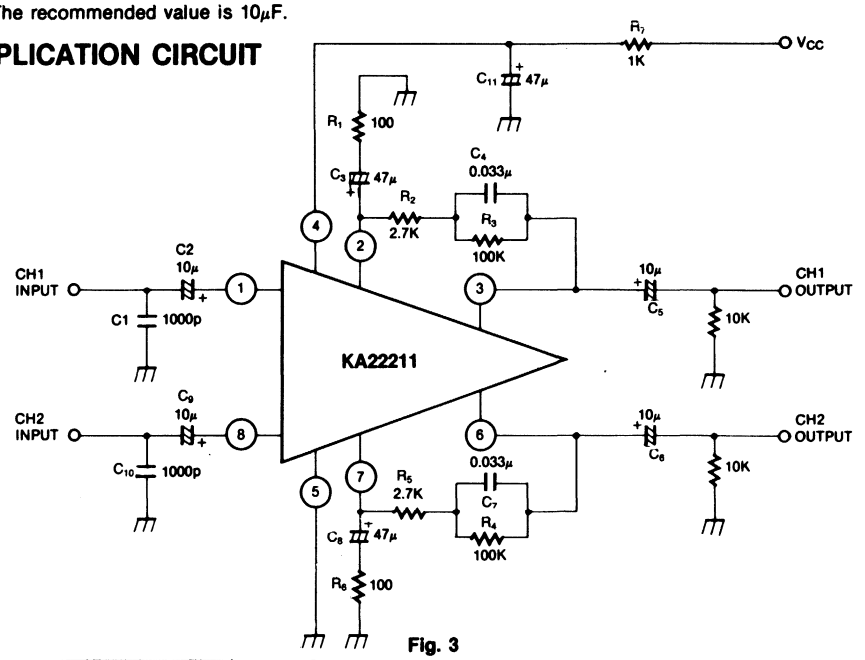
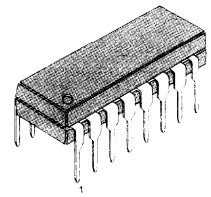


Fig. 3

5-BAND GRAPHIC EQUALIZER AMPLIFIER

The KA2223 is a monolithic integrated circuit consisting of an operational amplifier with five resonant circuits and a active filter, and it is suitable for radio-cassette tape recorders, car stereos or music center audio systems.

16 DIP



FEATURES

- **Tone control with independent adjustment of each band through an external capacitor.**
- **Gain control through an external variable resistor.**
- **Increasing the bands by adding resonant circuit or using two KA2223 in series.**
- **Low noise (V_{NO} = 7μV: Typ. Flat).**
- **Low distortion (THD=0.02% Typ. f=1KHz Flat).**
- **Large allowable input (V_I = 2.3V: Typ, V_{CC} = 9V, f = 1KHz Flat).**
- **Operating supply voltage range: V_{CC} = 5V ~ 13V**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2223	16 DIP	− 20°C ~ + 70°C

BLOCK DIAGRAM

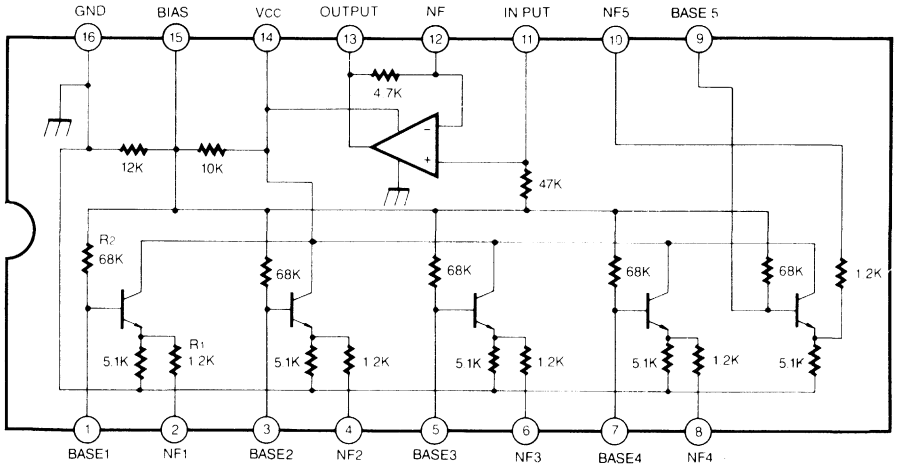


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	20	V
Power Dissipation	P_D	700	mW
Operating Temperature	T_{OPR}	−20 ~ +70	°C
Storage Temperature	T_{STG}	−55 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(T_a = 25°C, V_{CC} = 9V unless otherwise specified)

Characteristic		Symbol	Test		Min	Typ	Max	Unit
			f(Hz)	Conditions				
Quiescent Circuit Current		I_{CCQ}		V_I = 0	3.0	5.2	8.0	mA
Voltage Gain	Flat	G_V (Flat)	1K	V_I = −10dBm	−3.8	−0.8	2.2	dB
	Boost	G_V (Boost)	108	V_I = −10dBm	8	10.5	12	dB
			343					dB
			1.08K					dB
			3.43K					dB
			10.8K					dB
	Cut	G_V (Cut)	108	V_I = −10dBm	−12	−10.5	−8	dB
			343					dB
			1.08K					dB
			3.43K					dB
			10.8K					dB
Total Harmonic Distortion		THD	1K	V_I = 1V		0.02	0.1	%
Output Noise Voltage		V_{NO}	Flat, Input Short BW(−3dB) = 10Hz ~ 30KHz			7.0	30	μV

TEST CIRCUIT

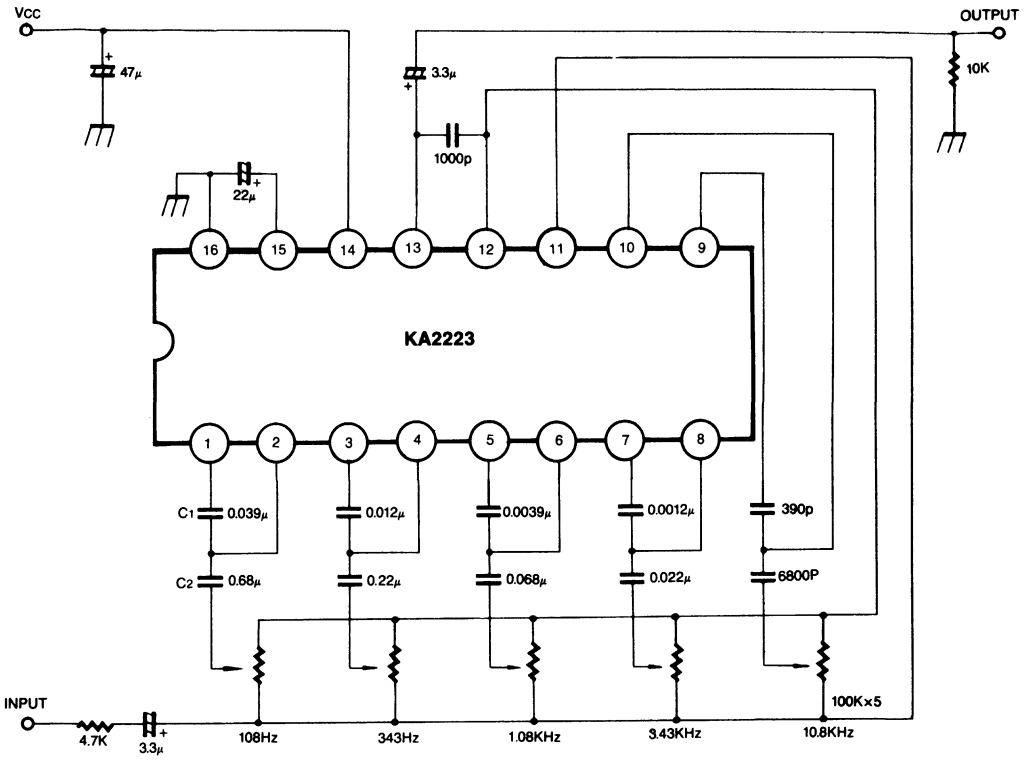


Fig. 2

$$\text{Resonant frequency } f_O = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}$$

(R_1 =1.2K, R_2=68K on-chip resistor)

APPLICATION CIRCUIT

1. 7 BAND

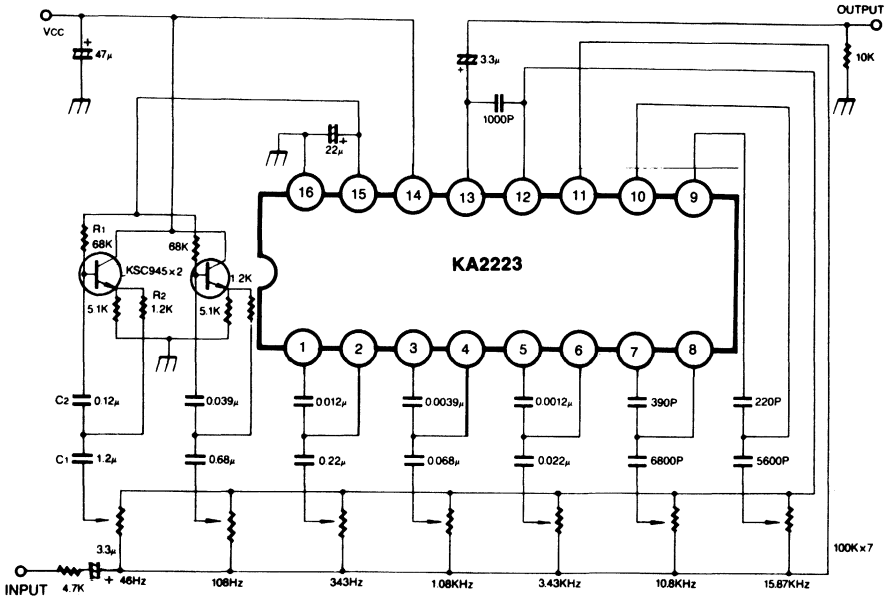


Fig. 3

2. 10 BAND

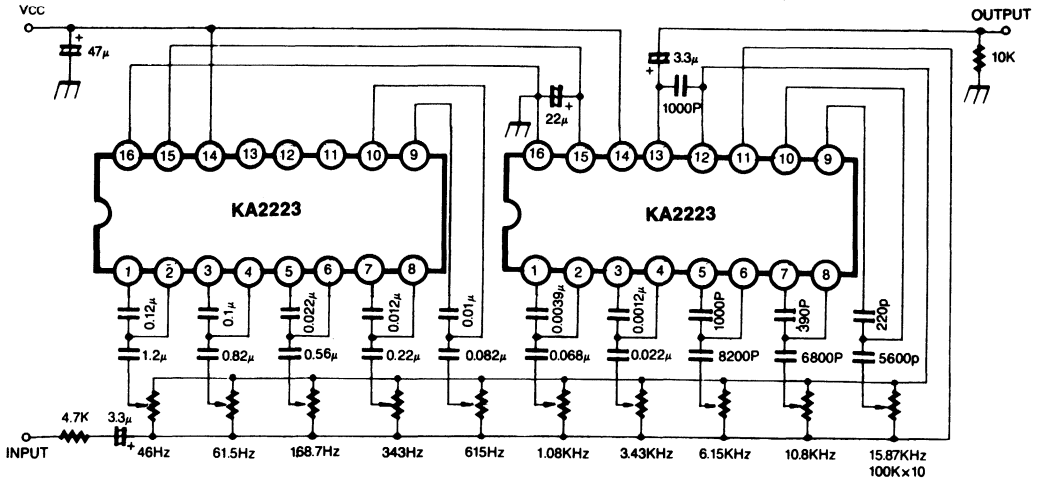
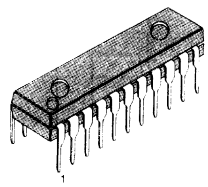


Fig. 4

3-BAND DUAL GRAPHIC EQUALIZER AMPLIFIER

The KA22233 is a monolithic integrated circuit consisting of an operational amplifier, three resonant circuits with an active filter, and it is suitable for radio cassette recorders, car stereos or music centers and audio systems.

22 DIP



FEATURES

- **Tone control with independent adjustment of each band through an external capacitor.**
- **Gain control through an external variable resistor.**
- **Increasing the bands by adding resonant circuit or using two KA22233 in series.**
- **Low noise (V_{NO}=7μV Typ, at Flat).**
- **Low distortion (THD=0.02% Typ, at f=1KHz, Flat).**
- **Large allowable input (V_i=2.3V Typ, at V_{CC}=9V, f=1KHz, Flat).**
- **Wide operating supply voltage range: V_{CC}=5V ~ 15V**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA22233	22 DIP	−20 ~ +70°C

SCHEMATIC DIAGRAM

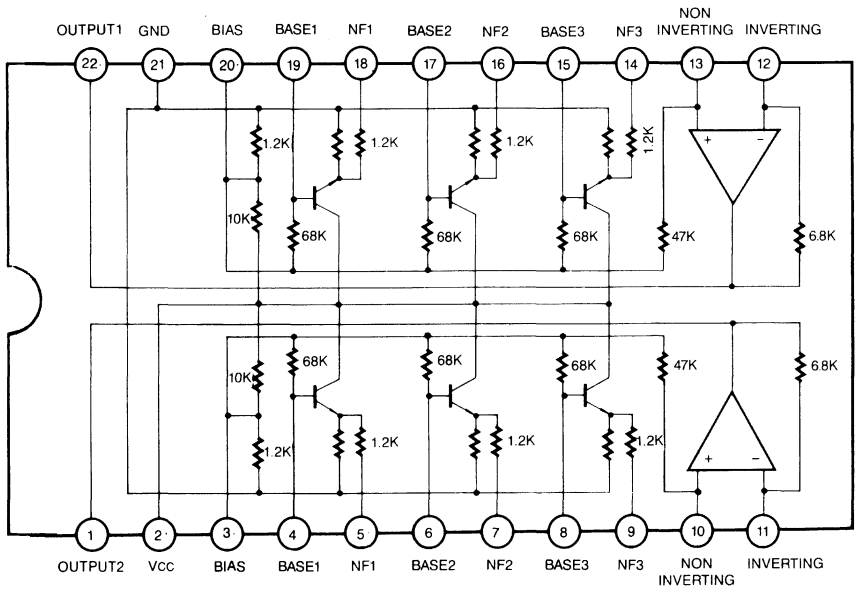


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	20	V
Power Dissipation	P_D	700	mW
Operating Temperature	T_{OPR}	−20 ~ +70	°C
Storage Temperature	T_{STG}	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 9V, R_G = 600Ω, R_L = 10KΩ, unless otherwise specified)

Characteristic		Symbol	Test f (Hz)	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current		I_{CCQ}		V_I = 0	5.0	7.2	10.0	mA
Voltage Gain	Flat	G_V (Flat)	1K	V_I = −10dBm	−2.5	−0.5	+1.5	dB
	Boost	G_V (Boost)	108					
			1.08K	V_I = −10dBm	10.5	12.5	14.5	dB
			10.8K					
	Cut	G_V (Cut)	108					
			1.08K	V_I = −10dBm	−14.5	−12.5	−10.5	dB
			10.8K					
Total Harmonic Distortion		THD	1K	V_I = 1V		0.02	0.1	%
Output Noise Voltage		V_{NO}	Flat, Input Short BW(−3dB) = 10Hz ~ 30KHz			7.0	30	μV
Channel Balance		CB	1K	V_I = 1V	−2.0	0	+2.0	dB
Cross Talk		CT	1K	V_I = 1V		70		dB

TEST CIRCUIT

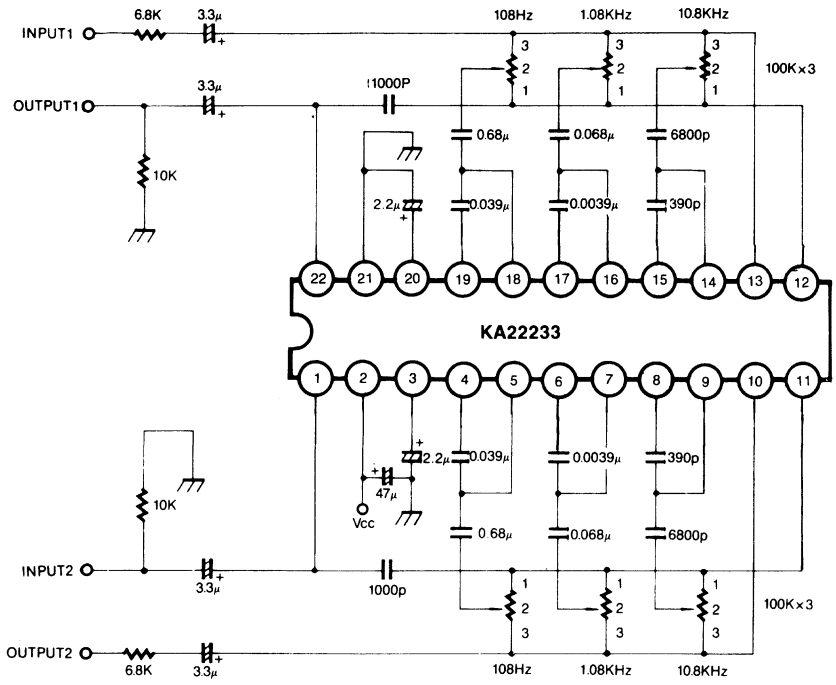
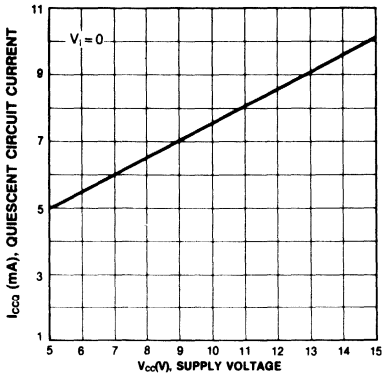


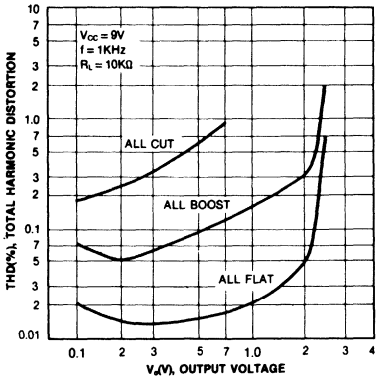
Fig. 2

Note: Volume Function
Position 1: Boost
Position 2: Flat
Position 3: Cut

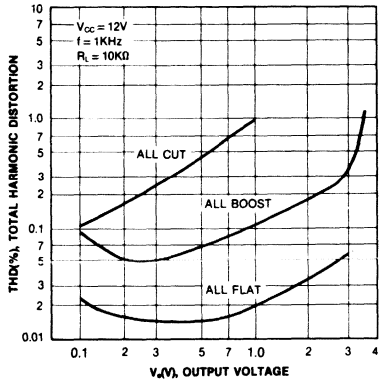
QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE



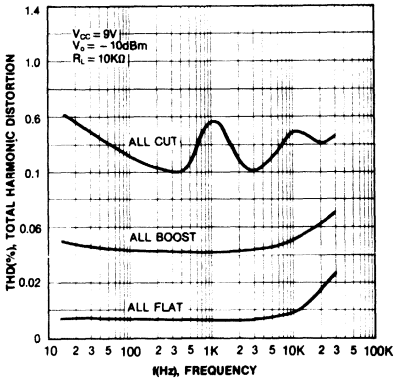
TOTAL HARMONIC DISTORTION-OUTPUT VOLTAGE



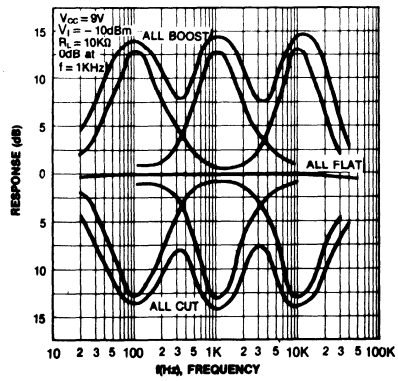
TOTAL HARMONIC DISTORTION-OUTPUT VOLTAGE



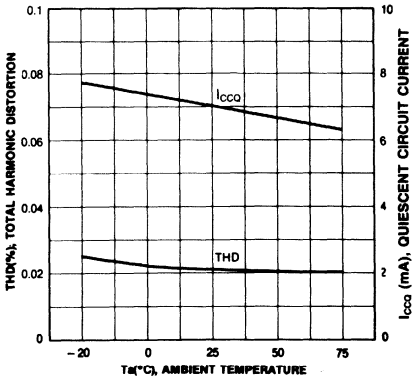
TOTAL HARMONIC DISTORTION-FREQUENCY



FREQUENCY RESPONSE



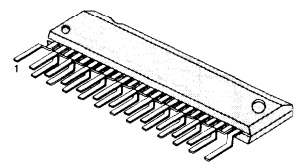
TOTAL HARMONIC DISTORTION, QUIESCENT CIRCUIT CURRENT-AMBIENT TEMPERATURE



5-BAND DUAL GRAPHIC EQUALIZER AMPLIFIER

The KA22234 is a monolithic integrated circuit developed for the stereo 5 band graphic equalizer amplifier. It is consisting of an operational amplifier, four resonant circuits with an active filter, and it is suitable for radio cassettes, car stereos or music centers.

24 ZSIP



FEATURES

- **Tone control with independent adjustment of each band through an external capacitor**
- **Gain control through an external variable resistor (Gain = ± 11dB)**
- **Excellent cross talk characteristic (CT = 70dB Typ, at $R_G = 0$)**
- **Wide operating supply voltage range: $V_{CC} = 3.5V \sim 14V$**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA22234	24 ZSIP	−20°C ~ +70°C

BLOCK DIAGRAM

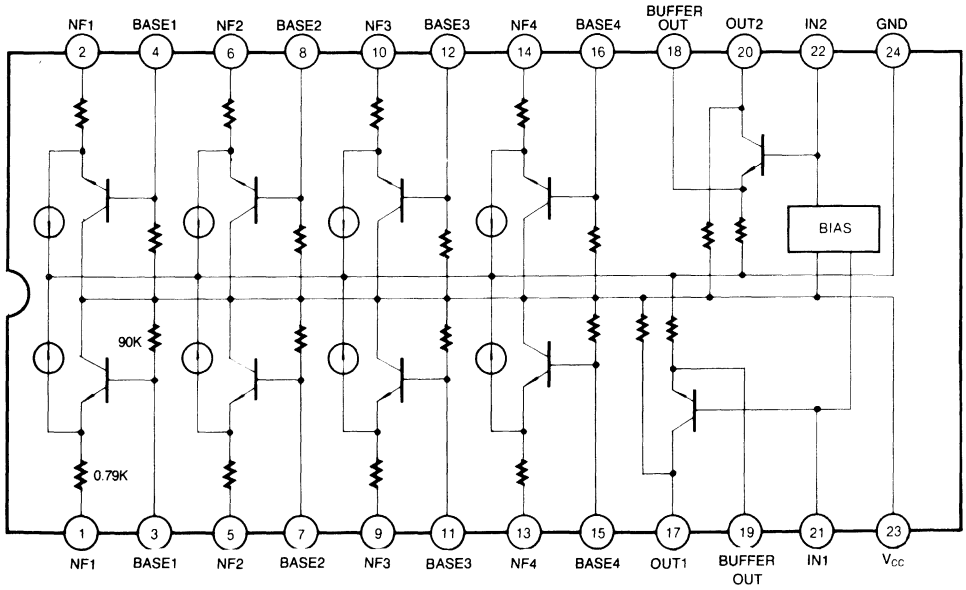


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	15	V
Power Dissipation	P_D	500	mW
Operating Temperature	T_{OPR}	−20 ~ +70	°C
Storage Temperature	T_{STG}	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 8V, R_L = 20KΩ, Flat Mode, unless otherwise specified)

Characteristic		Symbol	Test Conditions		Min	Typ	Max	Unit
			f(Hz)	Condition				
Quiescent Circuit Current		I_{CCQ}		V_I = 0	4.0	7.0	10.0	mA
Output Voltage		V_O	1K	THD = 1%	500	600		mV
Total Harmonic Distortion		THD	1K			0.1	0.3	%
Channel Balance		CB	1K		−1.0	0	1.0	dB
Cross Talk		CT	1K		50	70		dB
Output Noise Voltage		V_{NO}	Flat, R_G = 2.2KΩ BW(−3dB) = 10Hz ~ 30KHz			10	20	μV
Voltage Gain	Flat	G_V (Flat)	1K	V_I = 100mV	−2.0	−1.5	1.0	dB
	Boost	G_V (Boost)	100	V_I = 100mV	9.0	11.0	14.0	dB
			300					
			1K					
			3K					
			10K					
	Cut	G_V (Cut)	100	V_I = 100mV	−14.0	−11.0	−9.0	dB
			300					
			1K					
			3K					
			10K					

TEST CIRCUIT

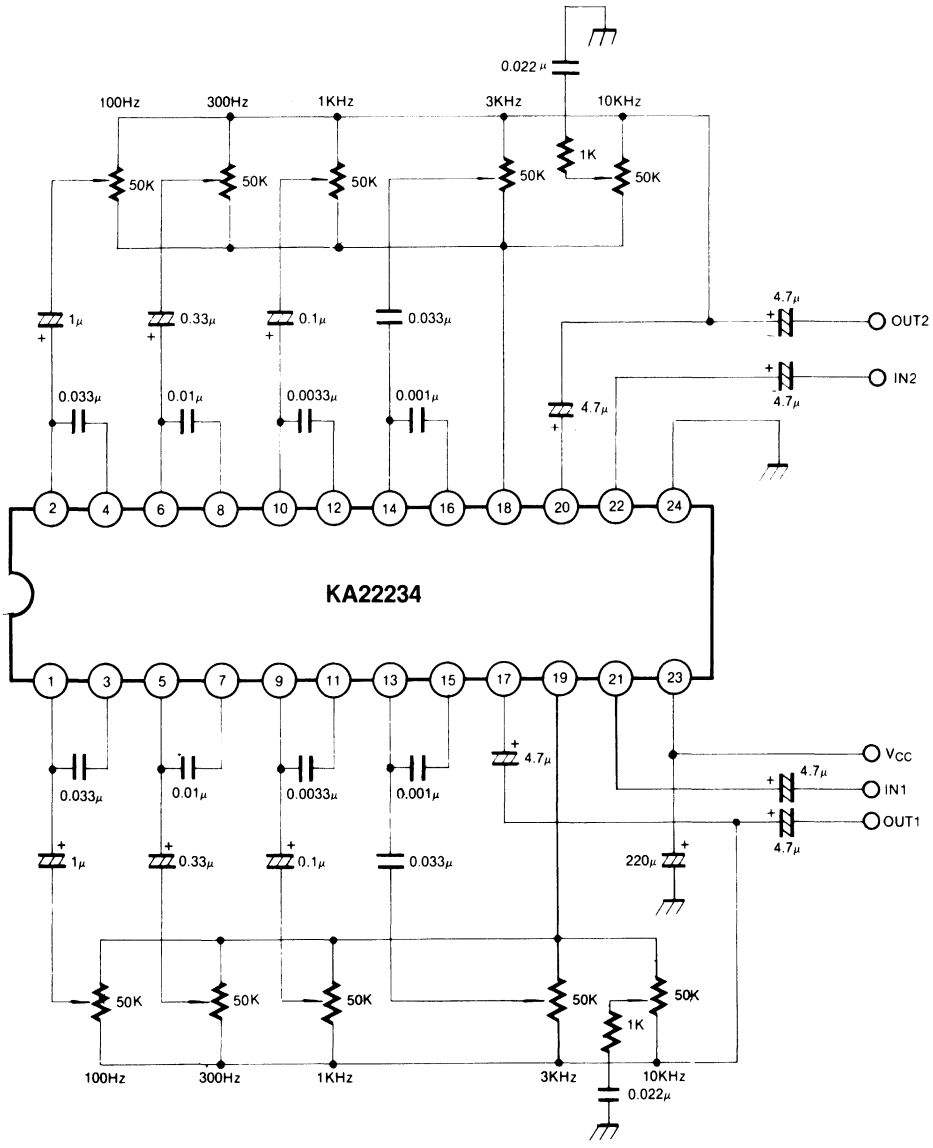
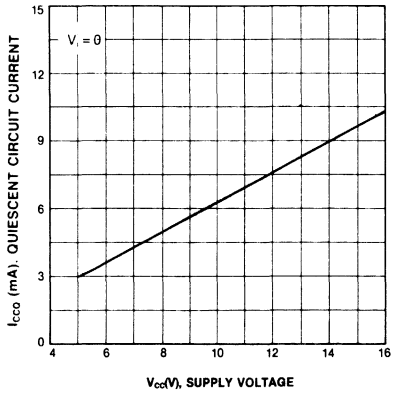
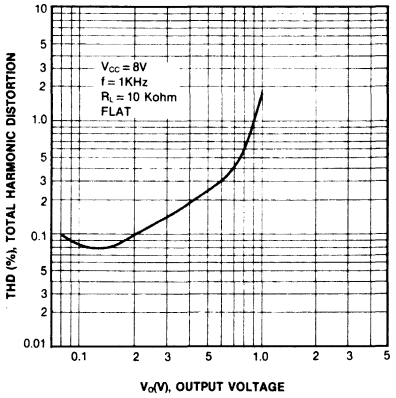


Fig. 2

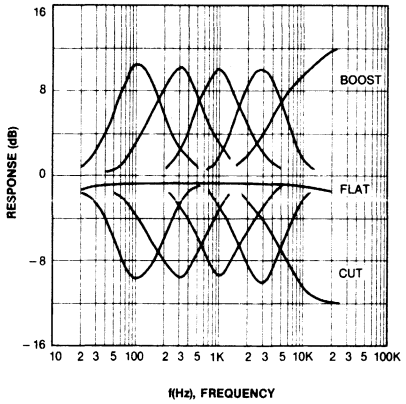
QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE



TOTAL HARMONIC DISTORTION-OUTPUT VOLTAGE



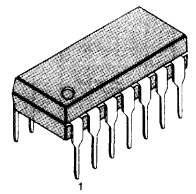
FREQUENCY RESPONSE



DUAL EQUALIZER AMPLIFIER WITH ALC

The KA?224 is a monolithic integrated circuit consisting of a dual equalizer amplifier with ALC, and it is suitable for stereo radio cassettes.

14 DIP



FEATURES

- Dual equalizer amplifier with a built-in ALC circuit.
- **Recording amp available because of high gain characteristic (Variable monitor possible).**
- **Good channel separation (CS = 50dB Typ).**
- **Quick stabilization after power on.**
- **Capable of direct meter driving and ALC transistor.**
- **Good ALC response balance between channels.**
- **Wide operating supply voltage range: V_{CC} = 4V ~ 13V**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2224	14 DIP	−20°C ~ +70°C

BLOCK DIAGRAM

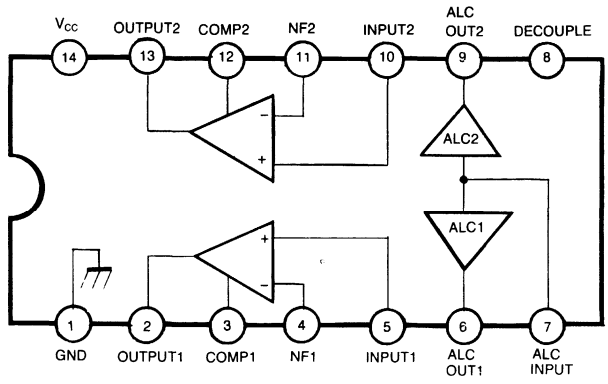


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	14	V
Power Dissipation	P_D	600	mW
Operating Temperature	T_{OPR}	−20 ~ +70	°C
Storage Temperature	T_{STG}	−40 ~ +125	°C
ALC TR Maximum Current		3.5	mA

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 5V, R_L = 10KΩ, f = 1KHz: play, R_L = 680Ω: Recording)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CCQ}	V_I = 0		4.5	10	mA
Open Loop Voltage Gain	G_{VO}			85		dB
Closed Loop Voltage Gain	G_{VC1}	Play		40		dB
	G_{VC2}	Record		58		dB
Output Voltage	V_O	THD=1%, Play	0.9	1.2		V
Total Harmonic Distortion	THD	V_O =0.5V, Play		0.1	1.0	%
Input Resistance	R_I		21	30		KΩ
Equivalent Input Noise Voltage	V_{NI}	BW (−3dB) =20Hz ~ 20KHz		1.0	2.0	μV
Cross Talk	CT	R_G = 2.2KΩ	40	50		dB
ALC Range	ΔV_{ALC}	V_I = −60dBm, Record	35	45		dB
ALC Balance	CB_{ALC}	V_I = −20dBm, Record		0	2.0	dB
ALC Distortion	THD_{ALC}	V_I = −20dBm, Record		0.5	2.0	%

TEST CIRCUIT

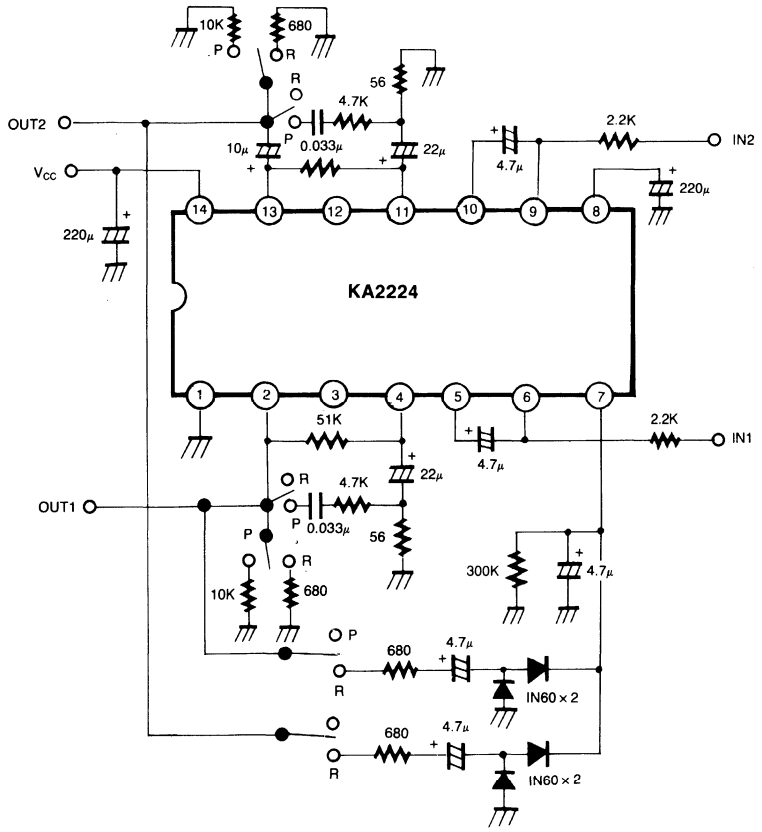
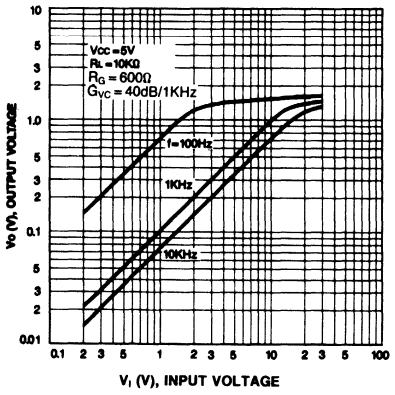
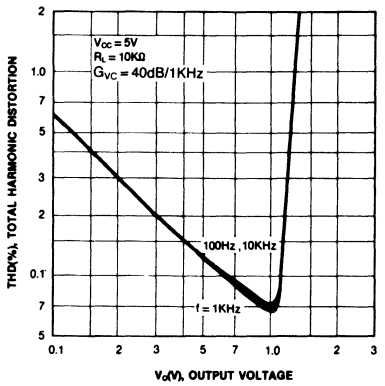


Fig. 2

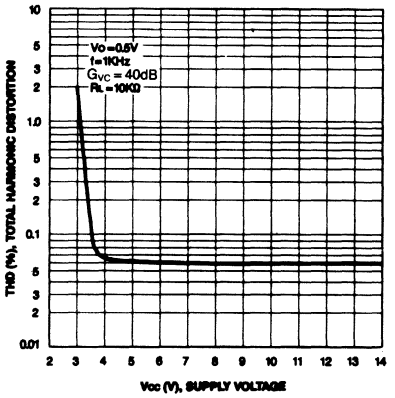
OUTPUT VOLTAGE-INPUT VOLTAGE



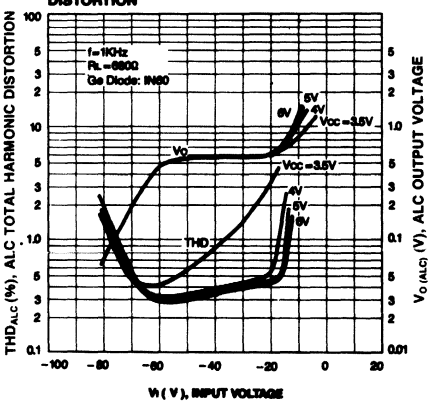
TOTAL HARMONIC DISTORTION-OUTPUT VOLTAGE



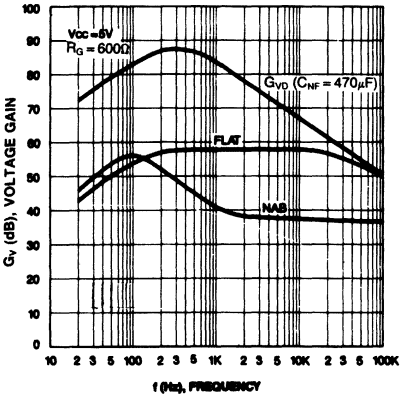
TOTAL HARMONIC DISTORTION-SUPPLY VOLTAGE



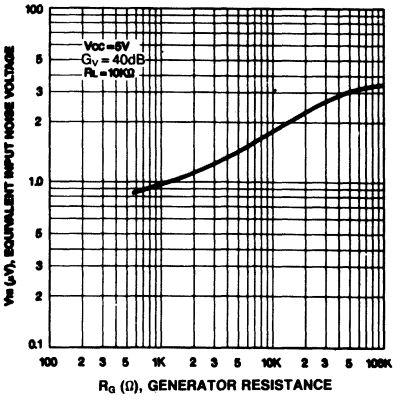
ALC OUTPUT VOLTAGE
ALC TOTAL HARMONIC DISTORTION — INPUT VOLTAGE



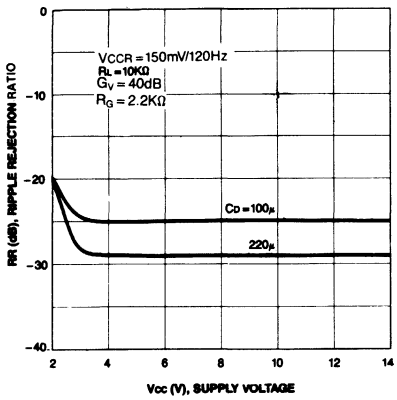
VOLTAGE GAIN-FREQUENCY



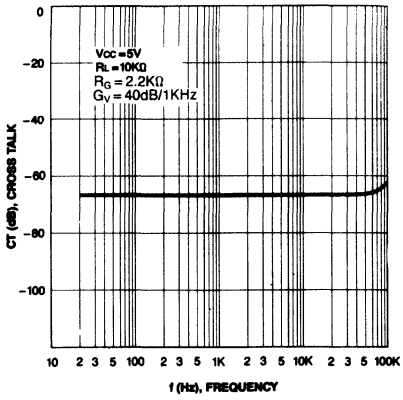
EQUIVALENT INPUT NOISE VOLTAGE -GENERATOR RESISTANCE



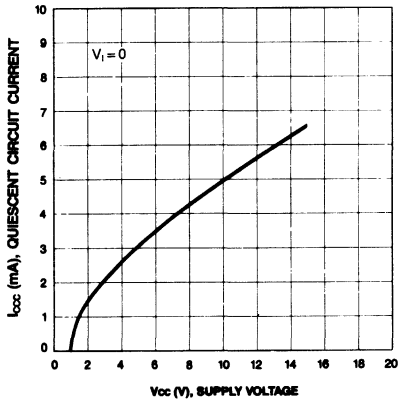
RIPPLE REJECTION RATIO-SUPPLY VOLTAGE



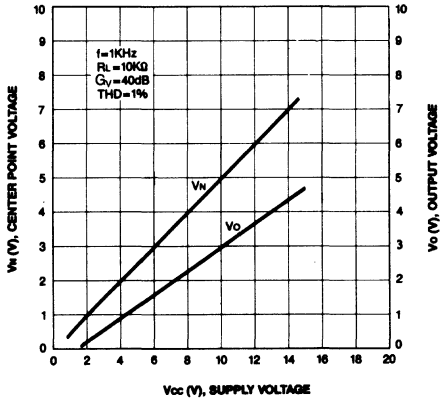
CROSS TALK-FREQUENCY



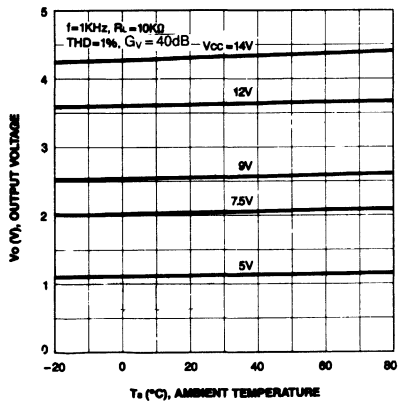
QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE



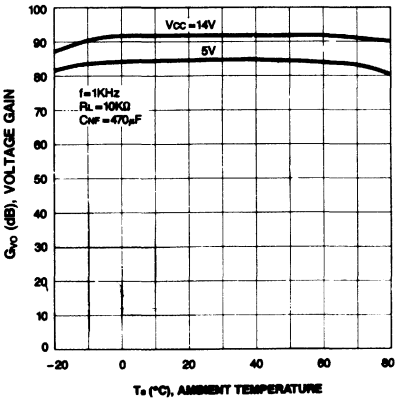
CENTER POINT VOLTAGE, OUTPUT VOLTAGE -SUPPLY VOLTAGE



OUTPUT VOLTAGE-AMBIENT TEMPERATURE



VOLTAGE GAIN-AMBIENT TEMPERATURE



APPLICATION INFORMATION

1. Closed Loop Voltage Gain

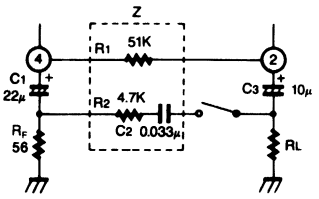


Fig. 4

SW on: play
off: record

A. Playback amplifier

$$G_V = 20 \log \frac{Z}{R_F} \text{ (dB) at f = 1KHz, } G_V = 42\text{dB (Typ)} \quad Z = R_1 // (R_2 + \frac{1}{2\pi f \cdot C_2})$$

B. Recording amplifier

$$G_V = 20 \log \frac{R_1}{R_F} \text{ (dB) at f = 1KHz, } G_V = 58\text{dB (Typ)}$$

2. ALC Circuit

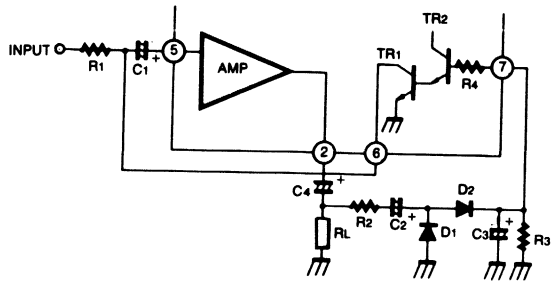
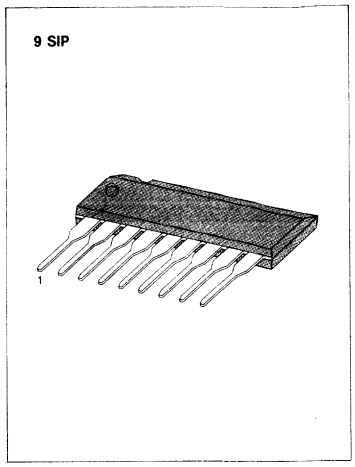


Fig. 5

The ALC circuit is consist of TR_1, TR_2 and some external components. The output level of the amplifier is rectified by external circuits. Since this DC level is applied to the ALC input terminal (Pin 7), the impedance between the collector and emitter of TR1 can change its value, therefore the pre-amplifier input level can be controlled.

DUAL EQUALIZER AMPLIFIER WITH ALC

The KA2224 is a monolithic integrated circuit consisting of a dual equalizer amplifier with ALC, and it is suitable for stereo radio cassette tape recorders.



FEATURES

- **Dual equalizer amplifier with built-in ALC circuit**
- **Low noise; V_{NI} = 1.0μV (Typ)**
- **High open loop voltage gain; 80 dB (Typ)**
- **Wide operating supply voltage range; V_{CC} = 4.5V ~ 14V**
- **Good ALC response balance between channels**
- **Not necessary the input coupling capacitor**
- **Not necessary diode or transistor for ALC**
- **Built in power supply muting circuit**
- **Minimum number of external parts required**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA22241	9 SIP	- 20°C ~ + 75°C

BLOCK DIAGRAM

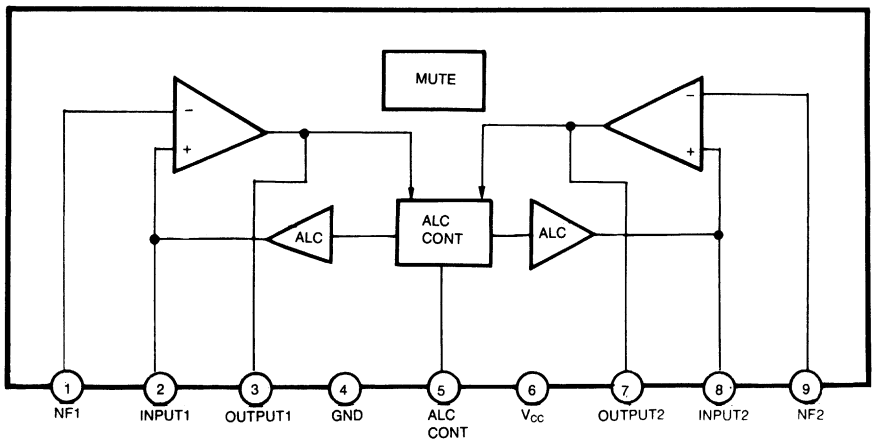


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Power Dissipation	P_D	*550	mW
Operating Temperature	T_{OPR}	−20 ~ +75	°C
Storage Temperature	T_{STG}	−40 ~ +125	°C

* : Derated avobe Ta = 25°C in the propotion of 5.5mW/°C

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 7V, f = 1KHz, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CCQ}	V_I = 0	1.5	3.5	4.5	mA
Open Loop Voltage Gain	G_{VO}	V_o = 0.3V	70	80		dB
Closed Loop Voltage Gain	G_{VC}	V_o = 0.3V	45	48	50	dB
Output Voltage	V_o	THD = 1%	0.6	1.2		V
Total Harmonic Distortion	THD	V_o = 0.3V		0.1	0.3	%
Equivalent Input Noise Voltage	V_{NI}	R_G = 2.2KΩ, BW (−3dB) = 20Hz ~ 20KHz		1.0	2.0	μV
Input Resistance	R_I		15	25	45	KΩ
ALC Range	ΔV_{ALC}	R_G = 3.9K, THD = 10%	40	45		dB
ALC Balance	CB_{ALC}	V_I = 1mV		0	2.5	dB

TEST CIRCUIT

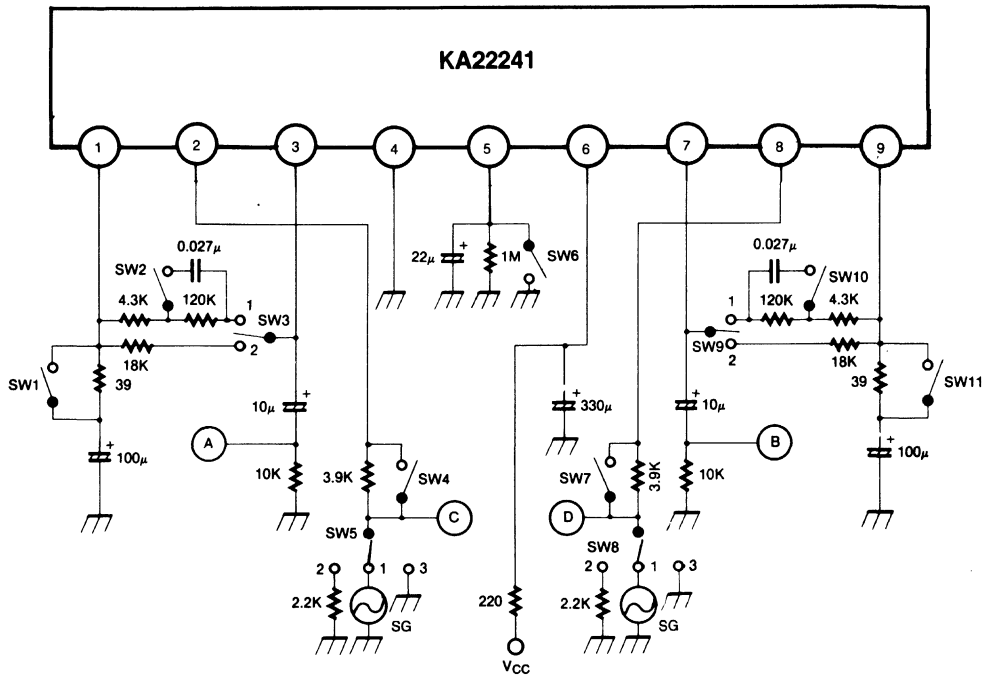


Fig. 2

TEST METHOD

Symbol		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11
I_{CCQ}		ON	OFF	1	ON	3	ON	ON	3	1	OFF	ON
G_{VO}		ON	OFF	1	ON	1	ON	ON	3	1	OFF	ON
G_{VC}	CH-1	OFF	ON	1	ON	1	ON	ON	3	1	OFF	ON
THD	CH-1	OFF	ON	1	ON	1	ON	ON	3	1	OFF	ON
V_o	CH-1	OFF	ON	1	ON	1	ON	ON	3	1	OFF	ON
V_{NI}	CH-1	OFF	ON	1	ON	2	ON	ON	3	1	OFF	ON
	CH-2	ON	OFF	1	ON	3	ON	ON	2	1	ON	OFF
ΔV_{ALC}	CH-1	OFF	OFF	2	OFF	1	OFF	ON	3	1	OFF	ON
CB_{ALC}		OFF	OFF	2	OFF	1	OFF	OFF	1	2	OFF	OFF

APPLICATION CIRCUIT

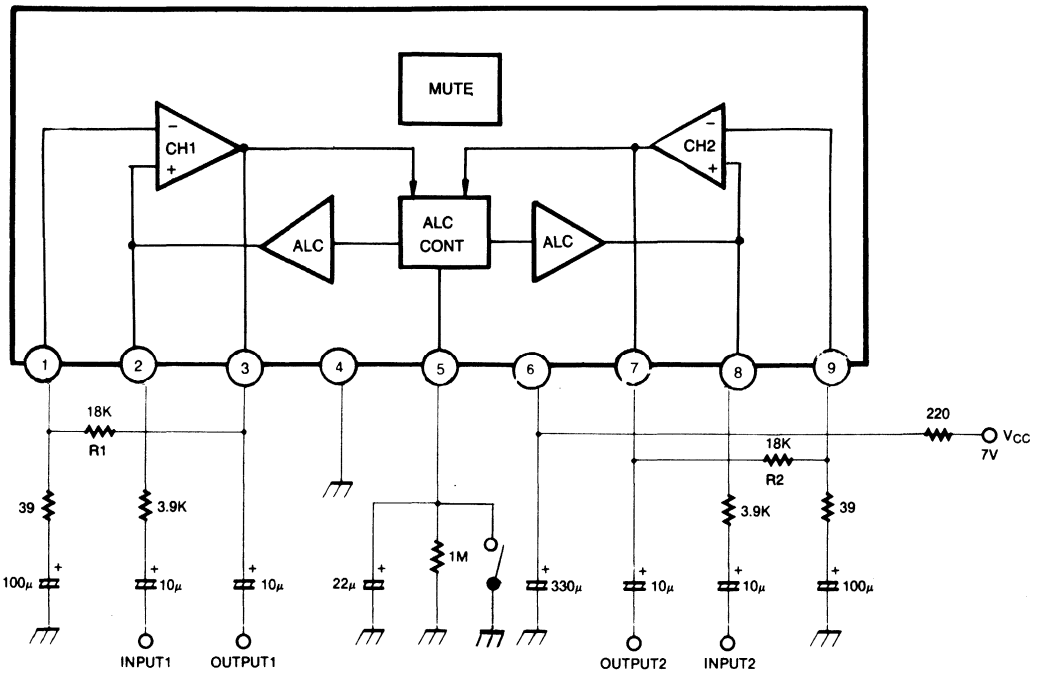
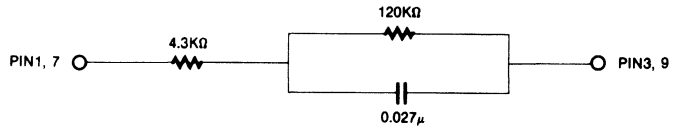


Fig. 3

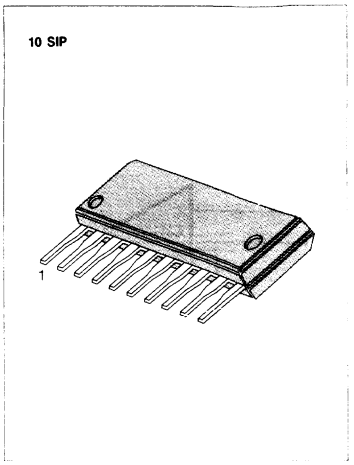
NOTE

ON recording, connect the time constant circuit as shown below, instead of R1, R2 of Pins 1-3, 7-9, which are used in the NAB.



DUAL EQUALIZER PRE-AMPLIFIER WITH ALC

The KA22242 is a monolithic integrated circuit consisting of a dual equalizer amplifier with ALC and Mute function, and it is suitable for stereo radio cassette tape recorders.



FEATURES

- **Dual equalizer amplifier with ALC circuit**
- **Direct coupling system of input circuit**
- **High open loop voltage gain (G_{VO} = 85dB at f = 1KHz)**
- **Wide operating supply voltage range (V_{CC} = 4V ~ 12V)**
- **Low noise (V_{NI} = 1.0μV at R_G = 2.2KΩ)**
- **Ripple rejection filter**
- **High input impedance (R_i = 62KΩ)**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA22242	10 SIP	−20°C ~ +75°C

BLOCK DIAGRAM

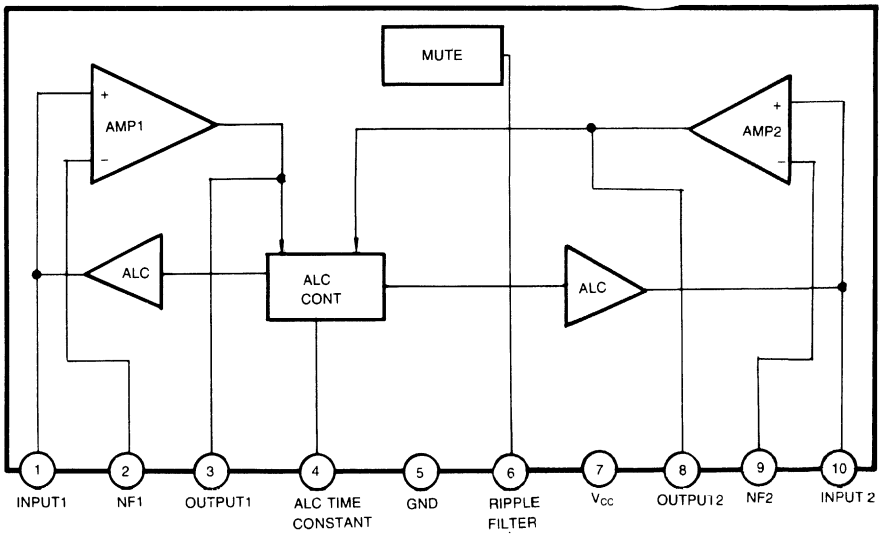


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	14	V
Power Dissipation	P_D	550	mW
Operating Temperature	T_{OPR}	−20 ~ +75	°C
Storage Temperature	T_{STG}	−55 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 8V, f = 1KHz, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CCQ}		2.5	3.3	4.0	mA
Open-loop Voltage Gain	G_{VO}	V_O = 1V	75	85		dB
Total Harmonic Distortion	THD	V_O = 0.3V		0.5	1.0	%
Output Voltage	V_O	THD = 1%	1.9	2.2		V
Equivalent Input Noise Voltage	V_{NI}	R_G = 2.2KΩ		1.0	2.5	μV
Input Resistance	R_I			62		KΩ
Cross Talk	CT	R_G = 2.2KΩ, V_O = 1V	45	55		dB
ALC Range	ΔV_{ALC}	V_I = −52dBm, 3dB up	40	45		dB
ALC Balance	CB_{ALC}	V_I = −45dB		0	2.0	dB
ALC Distortion	THD_{ALC}	V_I = −45dB		0.2	0.6	%
ALC Output Voltage	$V_{O(ALC)}$	V_I = −45dB	0.6	0.7	0.85	V

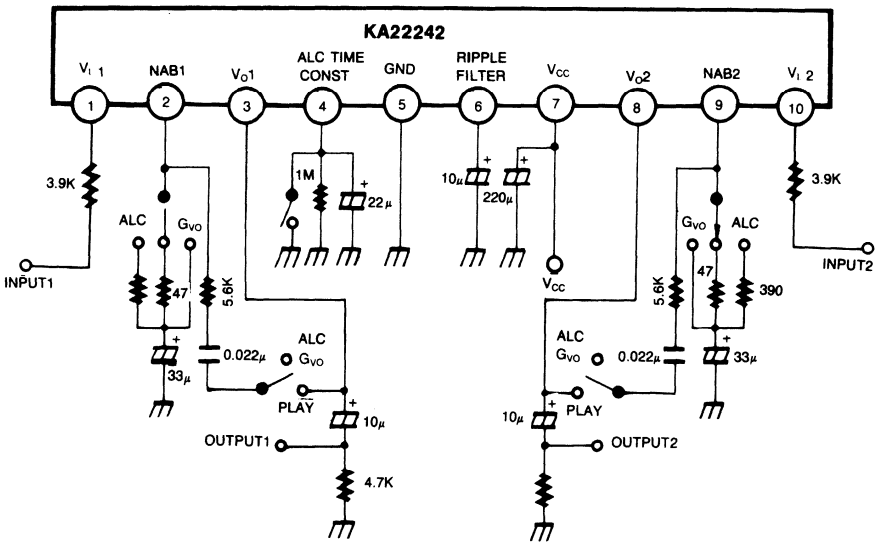
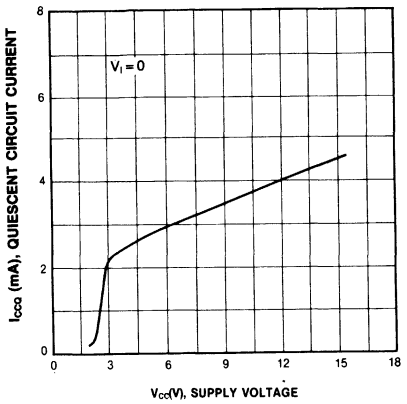
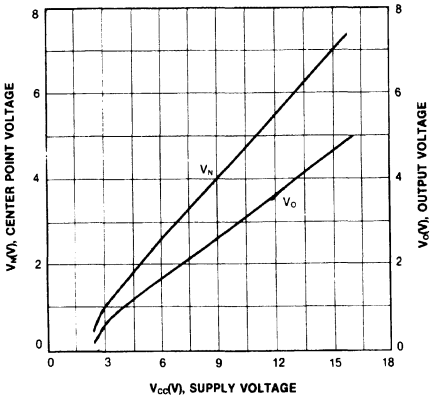


Fig. 2.

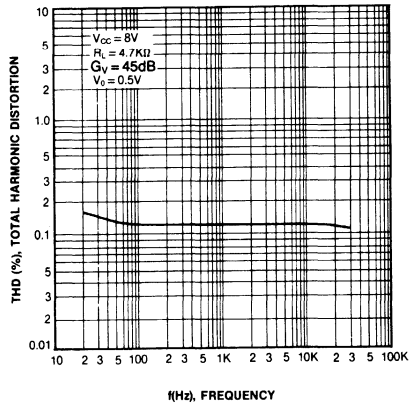
QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE



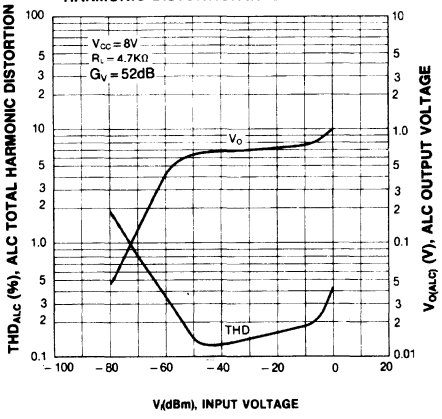
CENTER POINT VOLTAGE
OUTPUT VOLTAGE-SUPPLY VOLTAGE



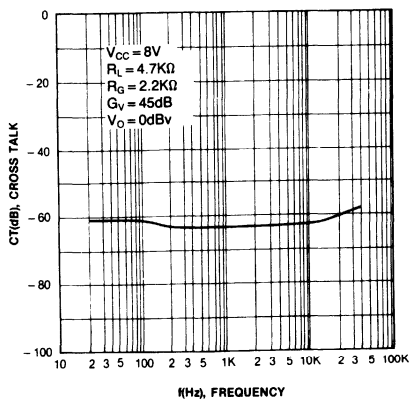
TOTAL HARMONIC DISTORTION-FREQUENCY



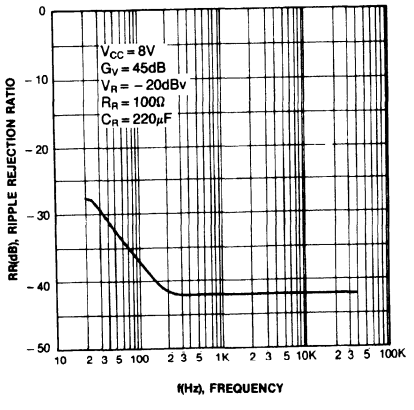
ALC OUTPUT VOLTAGE ALC TOTAL
HARMONIC DISTORTION-INPUT VOLTAGE



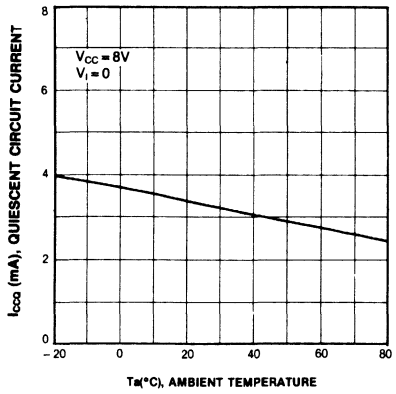
CROSS TALK-FREQUENCY



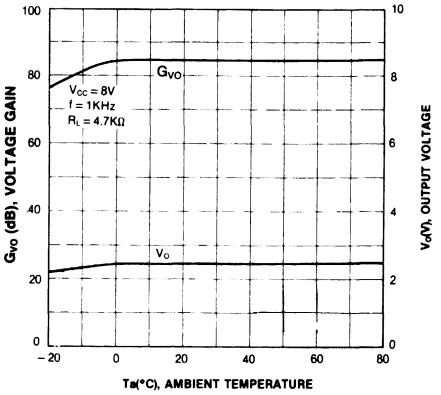
RIPPLE REJECTION RATIO-FREQUENCY



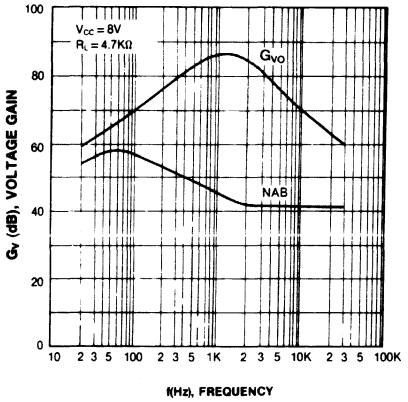
QUIESCENT CIRCUIT CURRENT-AMBIENT TEMPERATURE



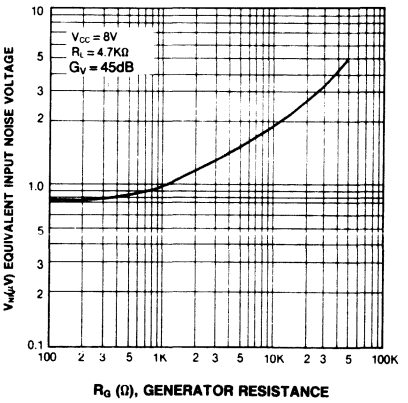
VOLTAGE GAIN OUTPUT VOLTAGE-AMBIENT TEMPERATURE



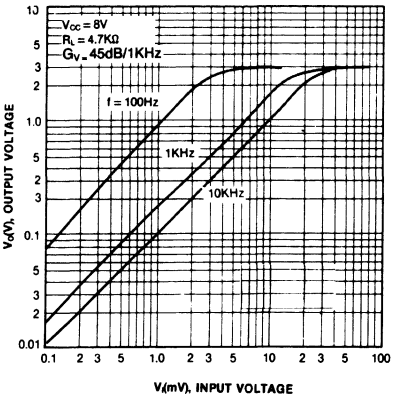
VOLTAGE GAIN-FREQUENCY



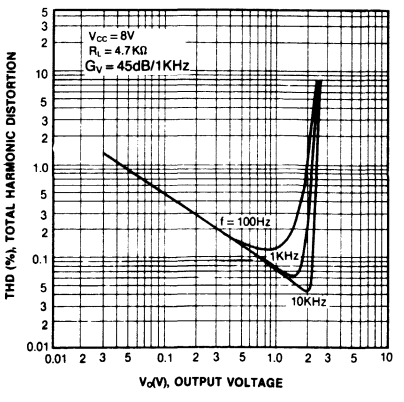
EQUIVALENT INPUT NOISE VOLTAGE-GENERATOR RESISTANCE



OUTPUT VOLTAGE-INPUT VOLTAGE



TOTAL HARMONIC DISTORTION-OUTPUT VOLTAGE



APPLICATION INFORMATION
DESCRIPTION OF KA22242

The KA22242 has a simple package, 10-pin and built-in ALC detector, mute circuit and ripple rejection filter developed for cassette tape recorders. To provide a stereo function, it has been developed into a 2-channel pre-amplifier for recording and playback. Also to provide high speed dubbing and recording gain, its gain is high (f = 1KHz, G_{VO} = 85dB) and the total harmonic distortion is low (f = 1KHz, THD = 0.5%). An input circuit is used as a direct coupling system to eliminate the input coupling capacitor and prevent tape head magnetization and pop noise. A built-in ripple circuit (ripple rejection transistor) improves the ripple rejection ratio. And the ALC circuit can achieve a wide dynamic range by simply attaching a time-constant circuit.

1. Playback Amplifier

To use the playback mode, the KA22242 can be applied for an NAB equalizer amplifier. The NAB characteristic is obtained by installing a NAB circuit in the Negative Feedback section (between Pins 2 and 3). In this case, Pin 4 is connected with the GND to eliminate the ALC effect.

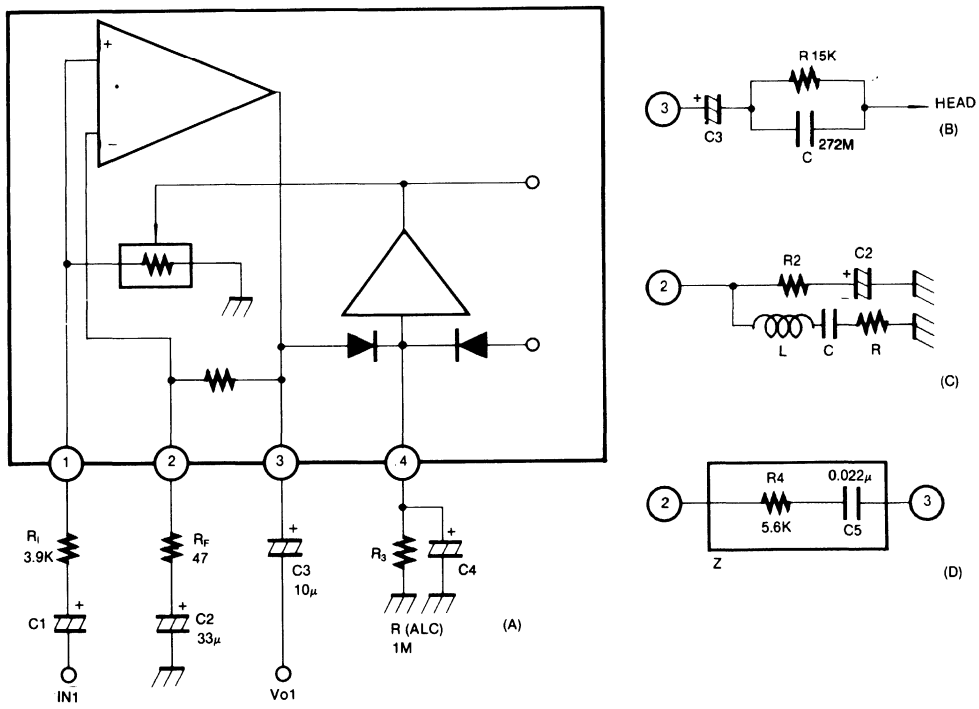


Fig. 3

2. Recording Amplifier (Figure 3 (A))

The recording amplifier's voltage gain is determined by the ratio of the internal 150KΩ to R2

$G_V = 150K\Omega/R2$

The recording amplifier requires a compensation circuit to correct loss at high frequencies. The compensation circuit may be either CR or LC resonance. The frequency response of the resonance circuit is fixed at 1~4KHz. An example using a CR is shown in Figure 3 (B), and one using LC resonance is shown in Figure 3 (C).

3. ALC Circuit

For the dynamic range, the ALC circuit uses the simple time-constant circuit. ALC operation of the KA22242 is accomplished with a signal rectifier and electronic volume control. The signal rectifier uses the comparator circuit and the comparator circuit compares the DC voltage of the output signal with the reference voltage. If the output voltage is higher than the reference voltage, the comparator turns on to charge smoothing capacitor C4.
For the dynamic range, a turn-off level ($0.7V_{rms}$) + 6dB is ensured at $V_{CC} = 6V$. When the peak voltage of the output signal is $0.7V_{rms}$, the comparator comes on and the electronic volume control is connected between the input line and GND. The input signal is attenuated by the ratio of the external resistance R_I to the electronic volume control resistance and ALC circuit is operated. The ALC range can be varied by changing R_I. If R_I is too large, the S/N ratio may degrade, so several Kohm is proper. The ALC attack time and recovery time are set at Pin 4 by C4 and R3. Note that the greater the time constant (C4, R3), the longer the recovery time, and the greater C4, the shorter the attack time.

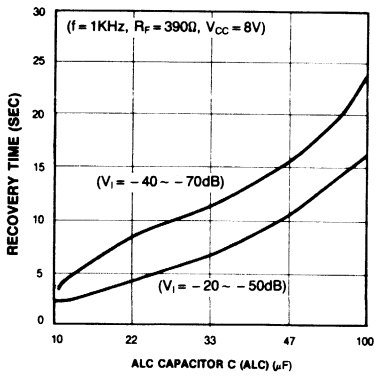
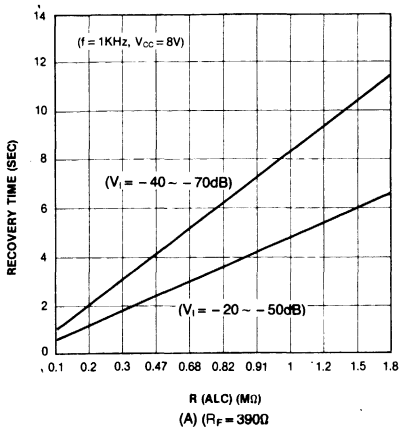


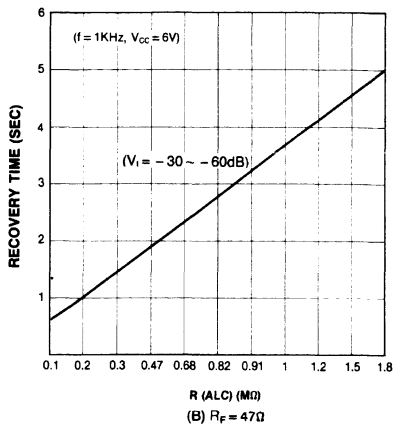
Fig. 4

Figure 4 is a ALC Time graph of the KA22242 at $R_F = 390ohm$.
At $R_F = 390ohm$, $V_I = -40dB$,
ALC recovery time is about 8 seconds and when the ALC capacitor is increased, it is increased also. And it is can be adjusted to fix the design point. But as the recovery time varies by the input level, the value of this capacitor must be considered when the set is designed.



(A) (R_F = 390Ω

Fig. 5



(B) R_F = 47Ω

Fig. 6

As the Figure 3, because the R_F range is 47 ≃ 100 ohm normally at the set application, the matching between R3 and C4 occurs.

4. Mute Function

The KA22242 has a mute function to mute at the power switch on/off. To prevent a malfunction of the ALC circuit, the KA22242 is muted at this time. If the ALC is not muted, the supply voltage charges the ALC capacitor and generates error-operations. The muting time is varied by the time-constant of the ripple filter.
C3*R internal (15K)
If C3 is too large, the rise time gets too slow and pop noises occur when other IC begins to operate faster than the KA22242 in some application circuit. In this case, if the combination with resistance is about 1Kohm, the DC voltage (V_{ODC}) at the output terminal is nearly constant.

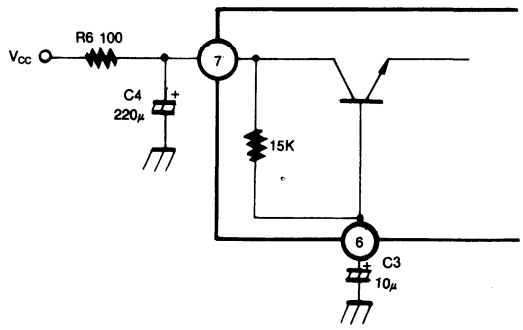


Fig. 7

APPLICATION CIRCUIT

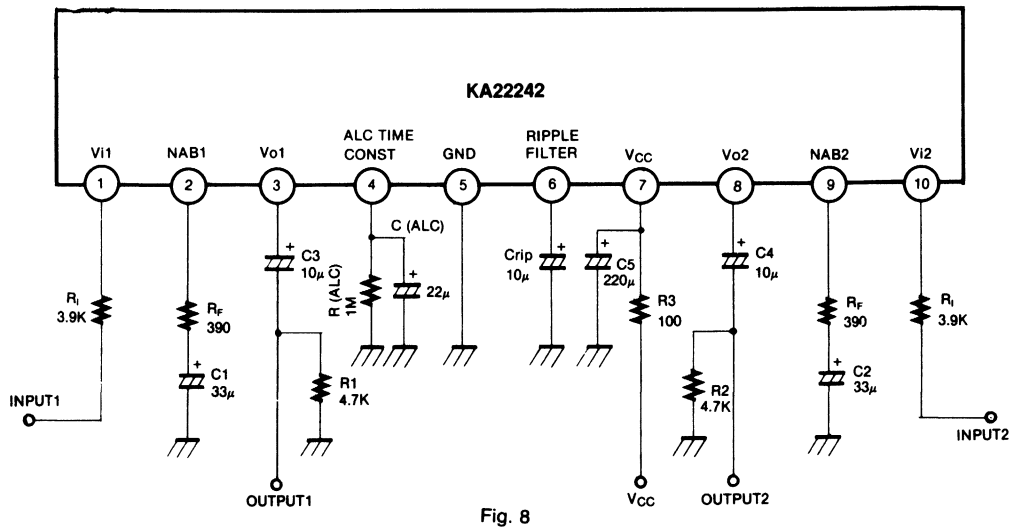
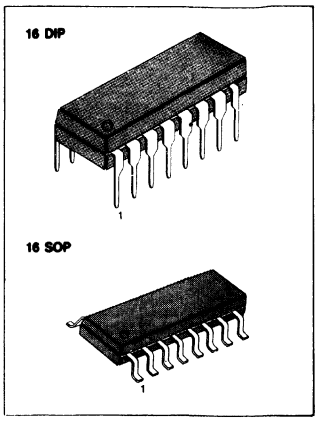


Fig. 8

DUAL PREAMPLIFIER FOR 3V USING

The KA2225 is a monolithic integrated circuit consisting of a dual equalizer amplifier, and it is suitable for 3V stereo radio cassettes.



FEATURES

- **High open loop gain: 85dB (Typ) (V_{CC} = 3V, f = 1kHz).**
- **Not necessary the input coupling capacitors.**
- **Operating supply voltage range: V_{CC} = 1.6V ~ 5V.**
- **Good channel separation: 60dB (Typ).**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2225	16 DIP	-20°C ~ +70°C
KA2225D	16 SOP	

BLOCK DIAGRAM

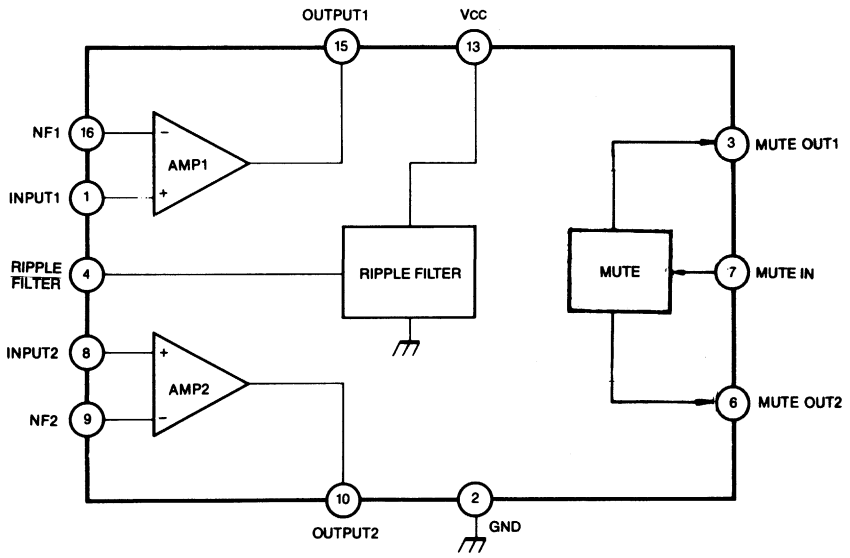


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic		Symbol	Value	Unit
Supply Voltage		V_{CC}	7	V
Power Dissipation	KA2225	P_D	750	mW
	KA2225D		350	
Operating Temperature		T_{OPR}	−20 ~ +70	°C
Storage Temperature		T_{STG}	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(T_a = 25°C, V_{CC} = 3V, f = 1KHz, unless otherwise specified)

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current		I_{CCQ}	V_I = 0		2	3.4	mA
Voltage Gain	Open Loop	G_{VO}		70	85		dB
	Closed Loop	G_{VC}			40		dB
Output Voltage		V_O	THD = 1%	0.5	0.8		V
Total Harmonic Distortion		THD	V_O = 0.1V,		0.07	0.5	%
Output Noise Voltage		V_{NO}	R_G = 2.2KΩ, G_V = 40dB BW(−3dB) = 50Hz ~ 20KHz		0.14	0.22	mV
Cross Talk		CT	R_G = 600Ω, V_O = −10dBv		60		dB
Muting Attenuation		ATT_{MUTE}	V_{MUTE} = 1V		43		dB
Input Resistance		R_I		20	30		KΩ

TEST CIRCUIT

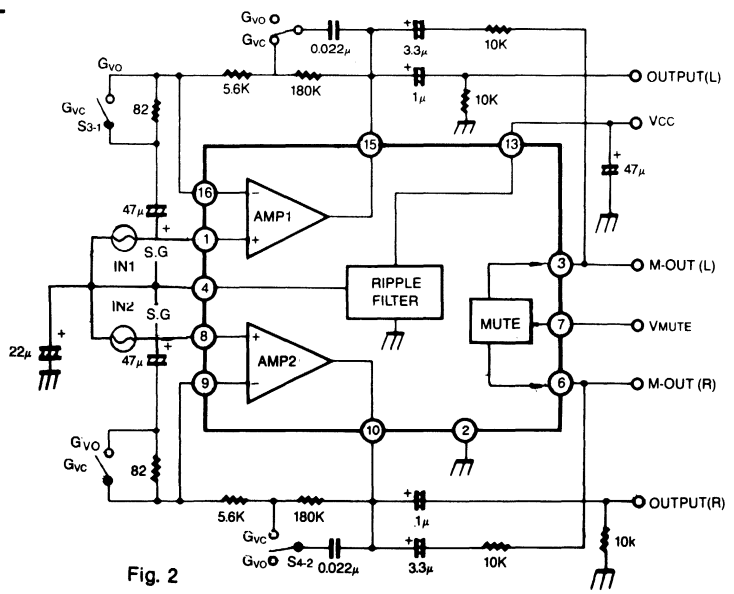


Fig. 2

APPLICATION CIRCUIT

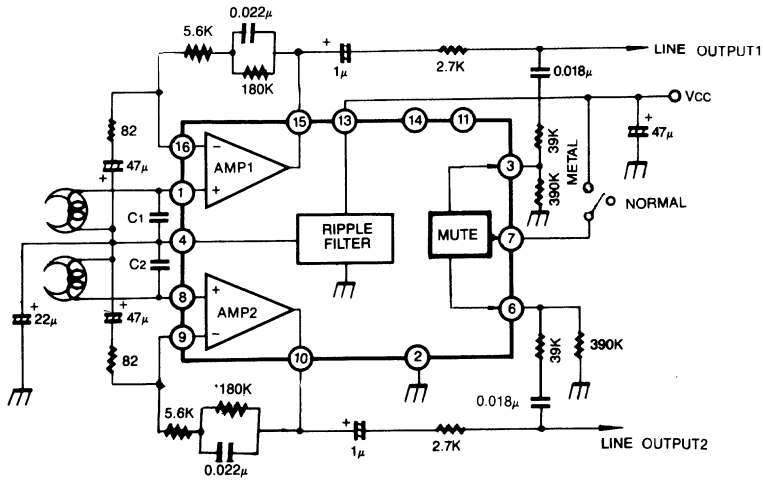


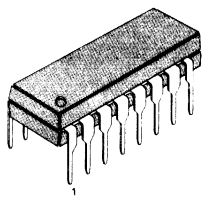
Fig. 3

- Capacitor C_1 and C_2 may be required to prevent instability caused by the pattern layout or interference of external high frequency signals.

DUAL EQUALIZER AMPLIFIER WITH REC AMP

The KA22261 is a monolithic integrated circuit consisting of a dual equalizer amplifier with REC AMP, and it is suitable for stereo radio cassettes.

16 DIP



FEATURES

- **Dual equalizer amplifier with ALC circuit.**
- **High open loop voltage gain: 78dB (Typ).**
- **Recording amplifier available because of high open loop voltage gain.**
- **Not necessary diode or transistor for ALC.**
- **Good channel separation: 60dB (Typ).**
- **Good ALC response balance between channels.**
- **Wide operating supply voltage range: V_{CC} = 6V ~ 15V.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA22261	16 DIP	−20 ~ +70°C

BLOCK DIAGRAM

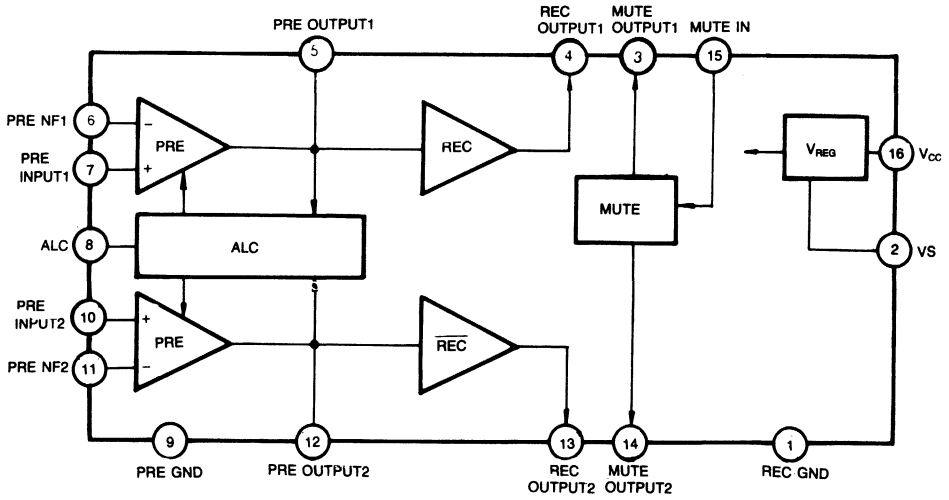


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Power Dissipation	P_D	750	mW
Operating Temperature	T_{OPR}	−20 ~ +70	°C
Storage Temperature	T_{STG}	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(T_a = 25°C, V_{CC} = 9V, f = 1KHz, unless otherwise specified)

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current		I_{CCQ}	V_I = 0		8.5	10.5	mA
PRE AMP	Open Loop Voltage Gain	G_{VO}	V_I = −80dBm	65	78		dB
	Output Voltage	Vo_1	THD = 1%	0.5	0.8		V
	Total Harmonic Distortion	THD_1	V_O = 0.2V		0.15	0.5	%
	Output Noise Voltage	V_{NO}	R_G = 2.2KΩ, NAB BW(−3dB) = 30Hz ~ 20KHz		0.26	0.6	mV
	Cross Talk	CT	R_G = 2.2KΩ	47	60		dB
REC AMP	Closed Loop Voltage Gain	G_{VC}	R_L = 10KΩ	12.7	14.7	16.7	dB
	Output Voltage	Vo_2	THD = 1%	2.0	2.5		V
	Total Harmonic Distortion	THD_2	V_O = 1.5V		0.3	1.0	%
	ALC Range (Note 1)	ΔV_{ALC}	V_I = −60dB, R_G = 2.2KΩ		45		dB
	ALC Distortion	THD_{ALC}	V_I = −20dBm, R_G = 2.2KΩ		0.3	1.0	%
	ALC Voltage	$V_{O(ALC)}$	V_I = −20dBm, R_G = 2.2KΩ	0.9	1.1	1.42	V
Muting Attenuation		ATT_{MUTE}		45	55		dB
ALC Balance		CB_{ALC}	V_I = −20dBm		0	2	dB

Note 1: Input voltage range from V_i = −60dB to output voltage V_O = 3dB up.

TEST CIRCUIT

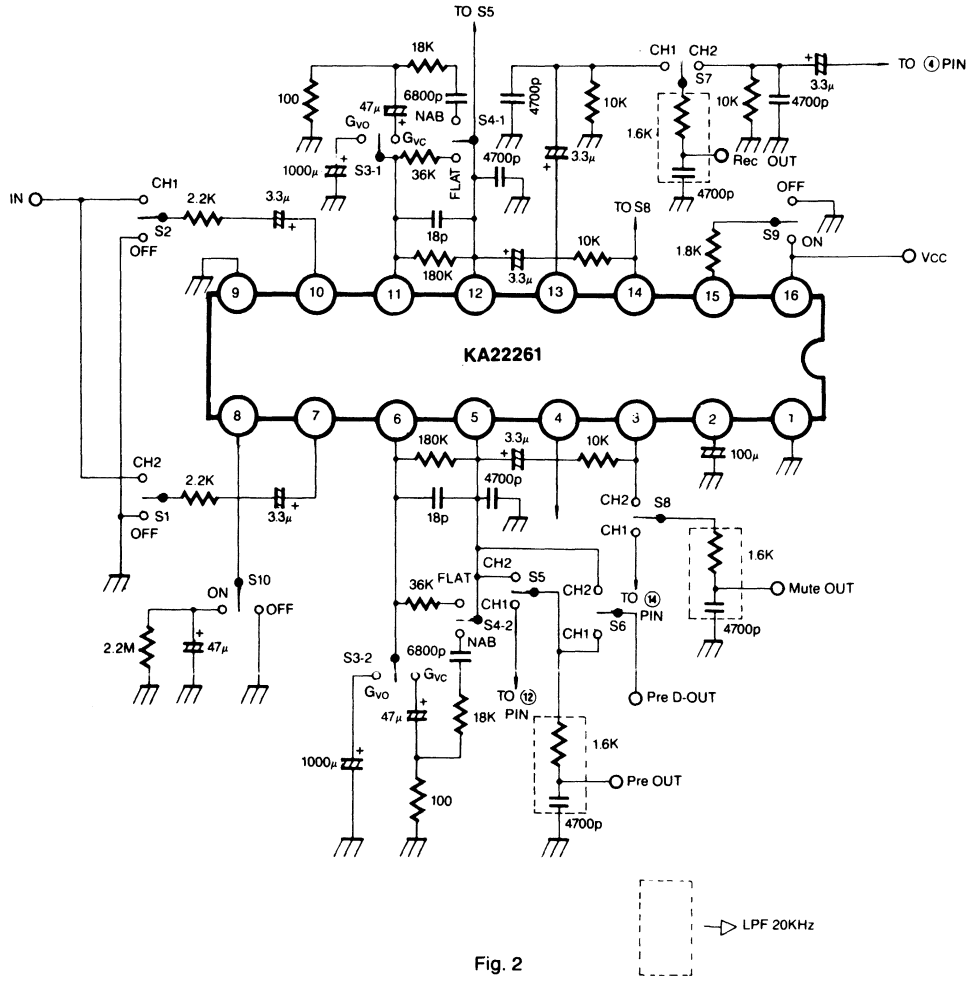


Fig. 2

APPLICATION CIRCUIT

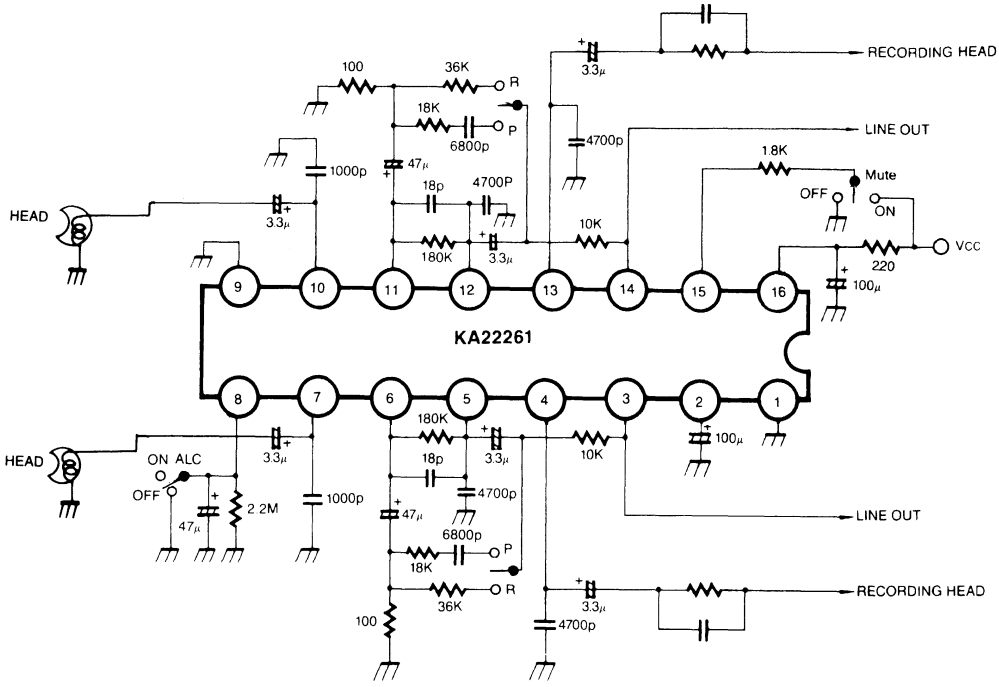
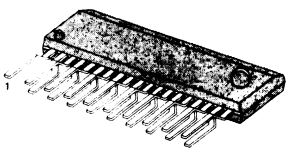


Fig. 3

DUAL EQUALIZER AMPLIFIER SYSTEM

The KA2228 is a monolithic integrated circuit consisting of play back AMP, REC AMP with ALC, mic AMP with ALC and monitor AMP. It is dual EQ AMP system built-in switch for selecting REC/PLAY mode, tape or radio (Aux) modes. It is used for radio cassette players and can be applicated easily by getting rid of the conventional mechanism REC/PLAY switch.

21 ZSIP



FEATURES

- **Following 4 modes can be operated by a combination of external switches: radio (Aux), radio (Aux) recording, mic recording and tape play back**
- **Built-in switch for selecting REC/PLAY mode.**
- **Built-in switch for selecting radio (Aux) or tape input.**
- **Few external parts.**
- **Small package: 21 shrink ZSIP type.**
- **Operating supply voltage range: V_{CC} = 3.5 ~ 7.0V**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2228	21 ZSIP	-25°C ~ +75°C

BLOCK DIAGRAM

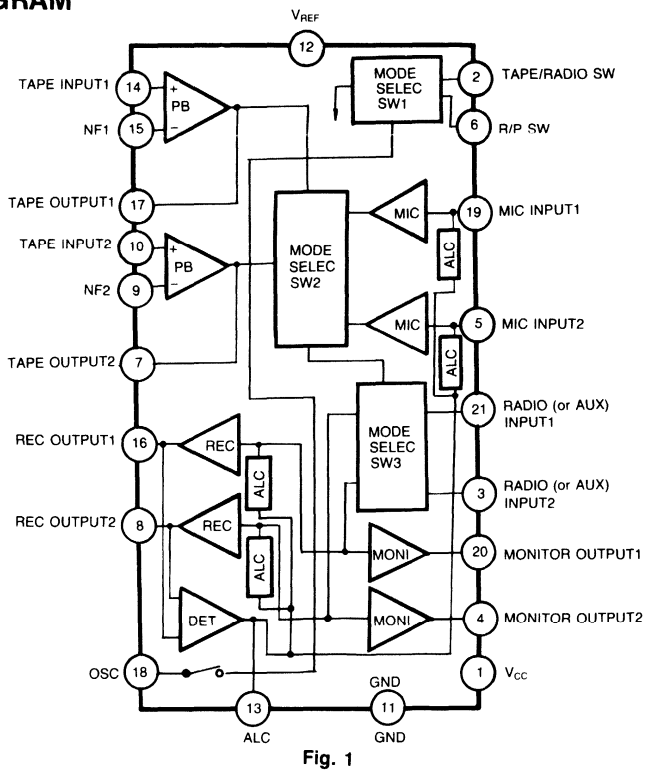


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	8	V
Power Dissipation	P_D	750	mW
Operating Temperature	T_{OPR}	−25 ~ +75	°C
Storage Temperature	T_{STG}	−55 ~ +155	°C

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 5V, f = 1KHz, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CCQ1}	Radio, V_i = 0	7	10	14	mA
	I_{CCQ2}	Radio REC, V_i = 0	10	13	16	mA
	I_{CCQ3}	Tape PB, V_i = 0	7	10	14	mA
	I_{CCQ4}	Mic REC, V_i = 0	6	9	12	mA
Reference Voltage	V_{REF}		1.8	2.0	2.3	V
MONITOR AMP						
Voltage Gain	G_{V1}	V_i = −50dBv	14	16	18	dB
Output Voltage	V_{O1}	THD = 1%	1.0	1.3		V
Total Harmonic Distortion	THD_1	V_O = −10dBv		0.06	0.2	%
Output Noise Voltage	V_{NO1}	Audio Band		14	30	μV
Cross Talk	CT_1	V_O = 0dBv	45	60		dB
Ripple Rejection Ratio	RR_1	V_R = −20dBv, f = 120Hz		50		dB
PLAY BACK AMP						
Closed Loop Voltage Gain	G_{VC}	V_i = −50dBv	35	38	41	dB
Output Voltage	G_{VO}	V_i = −90dBv	70	78		dB
Maximum Output Voltage	V_{O2}	THD = 1%	1.0	1.3		V
Total Harmonic Distortion	THD_2	V_O = −10dBv		0.02		%
Output Noise Voltage	V_{NO2}	Audio Band		80	150	μV
Cross Talk	CT_2	V_O = 0dBv	55	65		dB
Ripple Rejection Ratio	RR_2	V_R = −20dBv f = 120Hz	−34	−42		dB

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
RECORDING AMP						
Voltage Gain	G_{V2}	$V_I = -50dBv$	24	27	30	dB
Total Harmonic Distortion	THD_3	$V_O = -10dBv$		0.04		%
Output Noise Voltage	V_{NO3}	Audio Band		120	250	μV
Cross Talk	CT_3	$V_O = -10dBv$, Audio Band	55	65		dB
Ripple Rejection Ratio	RR_3	$V_R = -20dBv$, f = 120Hz	-34	-42		dB
ALC Voltage	$V_{O\,(ALC)\,1}$	$V_I = -20dBv$	-4.4	-2.7	0	dBv
ALC Voltage	$V_{O\,(ALC)\,2}$	$V_I = -15dBv$	-4.2	-2.5	0.2	dBv
ALC Voltage	$V_{O\,(ALC)\,3}$	$V_I = -5dBv$	-4.0	-2.2	0.5	dBv
MIC + REC AMP						
Voltage Gain	G_{V3}	$V_I = -80dBv$	60	63	66	dB
Total Harmonic Distortion	THD_4	$V_O = -10dBv$		0.7	2.0	%
Output Noise Voltage	V_{NO4}	Audio Band		3.5	7.0	mV
Cross Talk	CT_4	$V_O = -10dBv$	30	43		dB
Ripple Rejection Ratio	RR_4	$V_R = -20dBv$, f = 120Hz	13	20		dB
ALC Voltage	$V_{O\,(ALC)\,4}$	$V_I = -60dBv$	-4.0	-2.0	0.5	dBv
ALC Voltage	$V_{O\,(ALC)\,5}$	$V_I = -40dBv$	-4.0	-2.0	0.5	dBv
ALC Voltage	$V_{O\,(ALC)\,6}$	$V_I = -10dBv$	-4.0	-2.0	0.5	dBv

TEST CIRCUIT

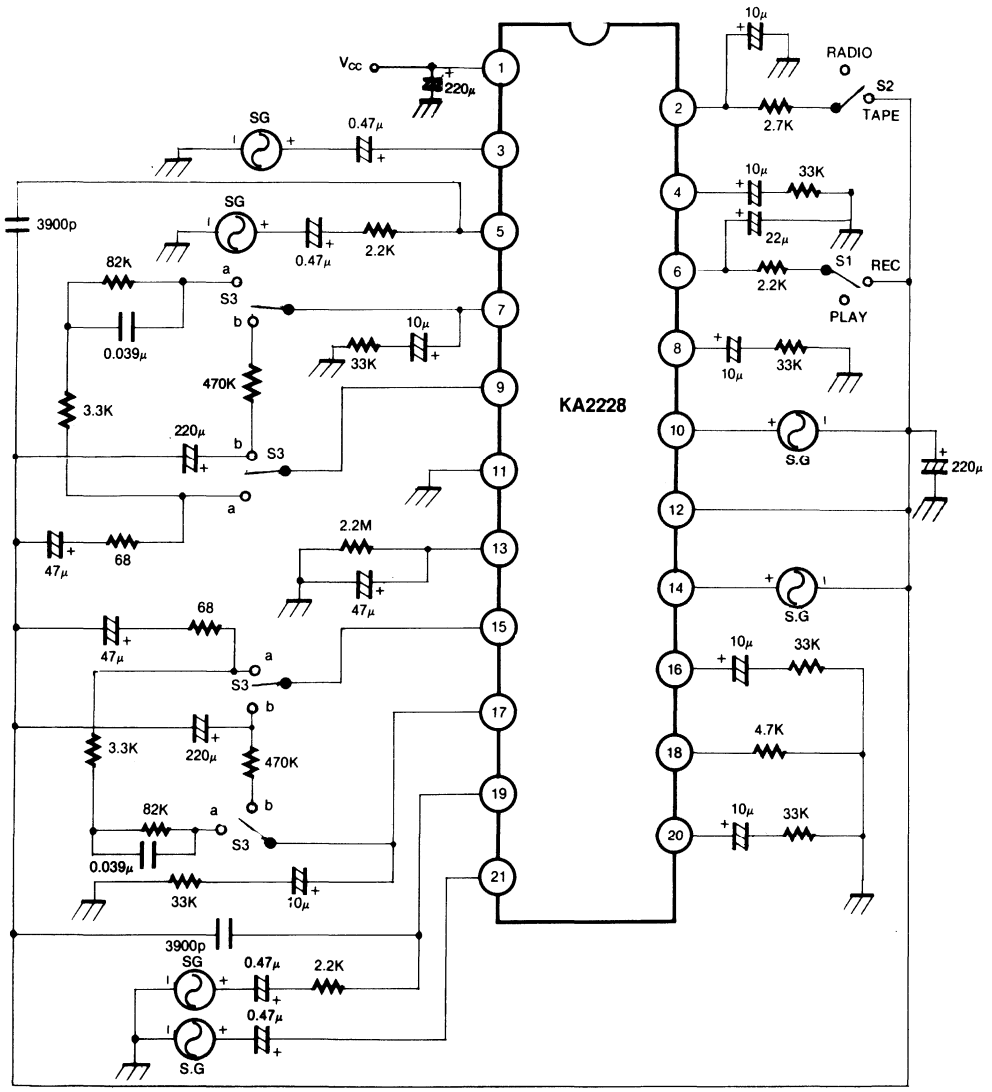
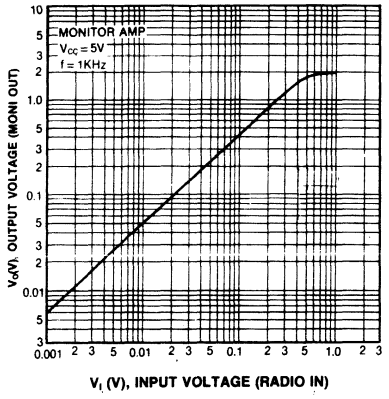


Fig. 2

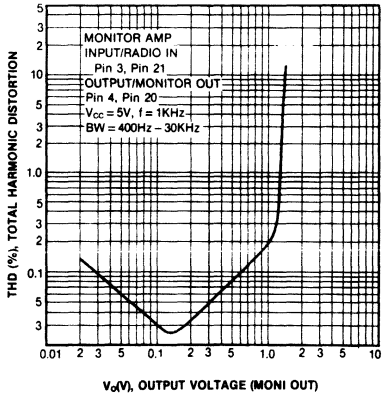
OPERATION MODE BY EXTERNAL SWITCHES (S1, S2) COMBINATION

CIRCUIT BLOCK / S1 / S2	S1 = REC		S1 = PLAY	
	S2 = RADIO	S2 = TAPE	S2 = RADIO	S2 = TAPE
MIC AMP	ON	ON	OFF	OFF
PB AMP	OFF	OFF	ON	ON
REC AMP	ON	ON	OFF	OFF
MONITOR AMP	ON	OFF	ON	ON
SMP	M	M	P	P
STR	R	T	R	T
SRE	ON	ON	OFF	OFF
OPERATION MODE	RADIO REC	MIC REC	RADIO PLAY	TAPE PLAY BACK

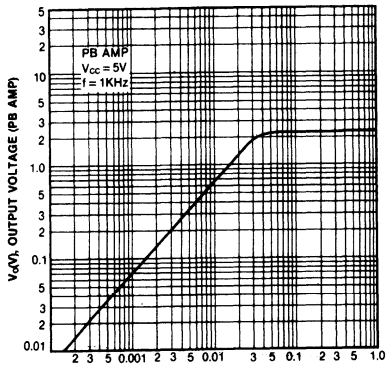
OUTPUT VOLTAGE-INPUT VOLTAGE



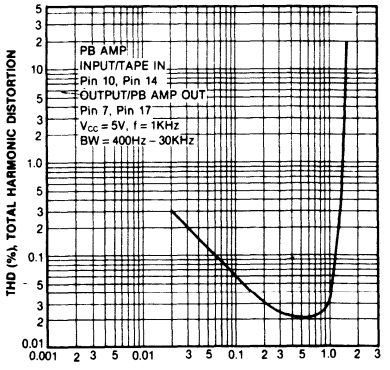
TOTAL HARMONIC DISTORTION-OUTPUT VOLTAGE



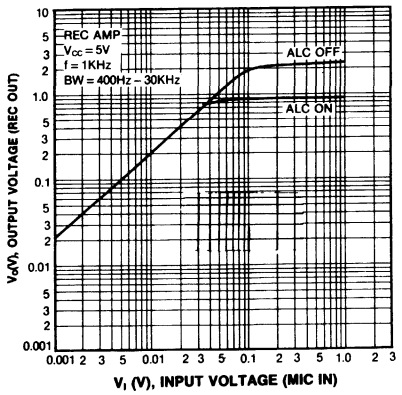
OUTPUT VOLTAGE-INPUT VOLTAGE



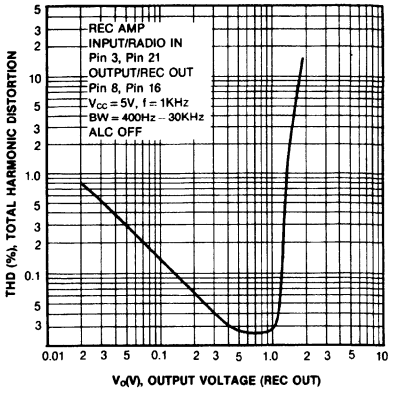
TOTAL HARMONIC DISTORTION-OUTPUT VOLTAGE



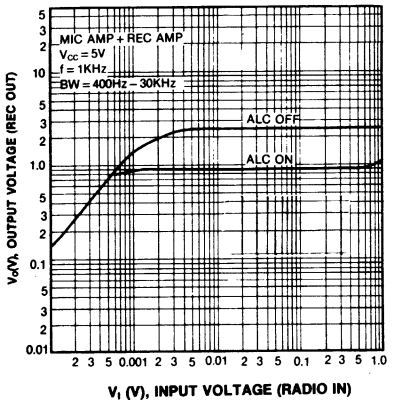
OUTPUT VOLTAGE-INPUT VOLTAGE



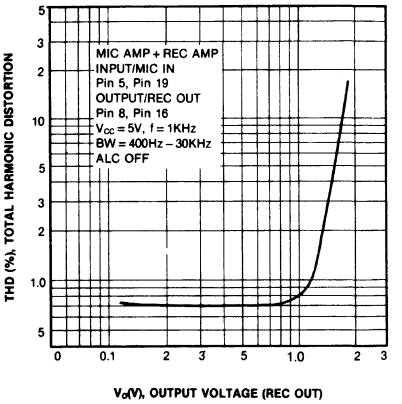
TOTAL HARMONIC DISTORTION-OUTPUT VOLTAGE



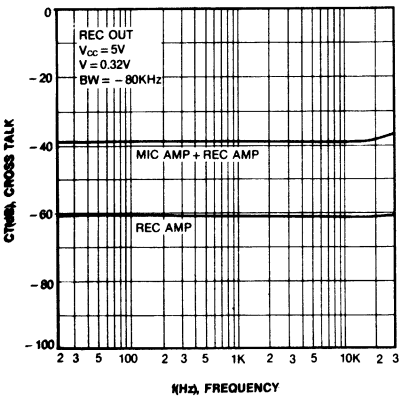
OUTPUT VOLTAGE-INPUT VOLTAGE



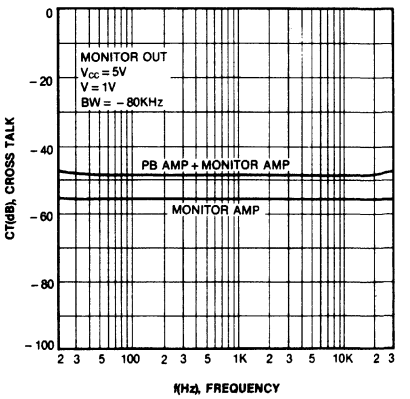
TOTAL HARMONIC DISTORTION-OUTPUT VOLTAGE



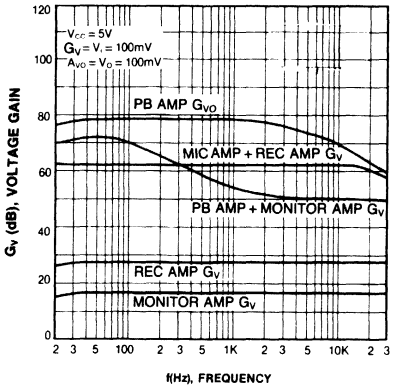
CROSS TALK-FREQUENCY



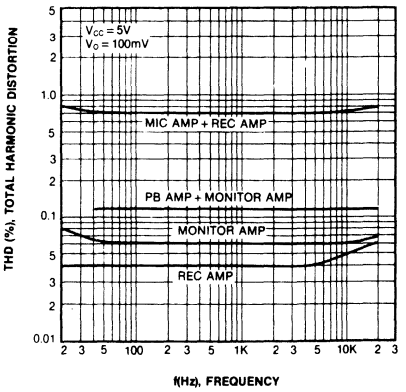
CROSS TALK-FREQUENCY



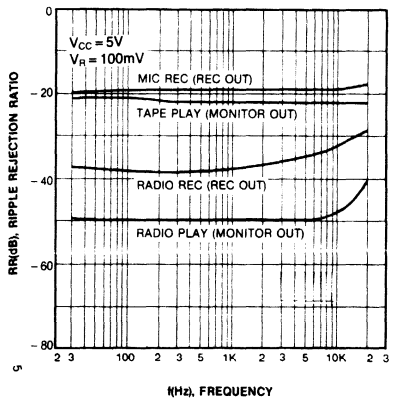
VOLTAGE GAIN-FREQUENCY



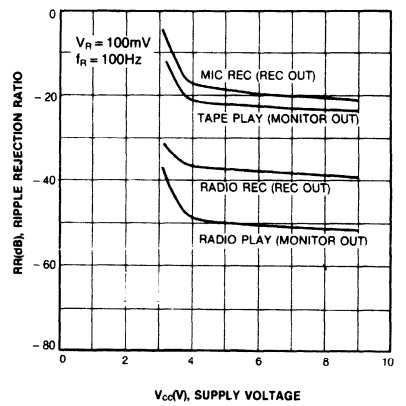
TOTAL HARMONIC DISTORTION-FREQUENCY



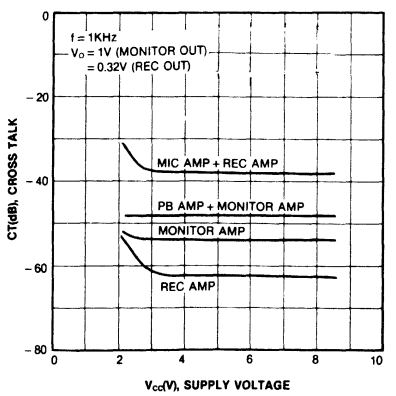
RIPPLE REJECTION RATIO-FREQUENCY



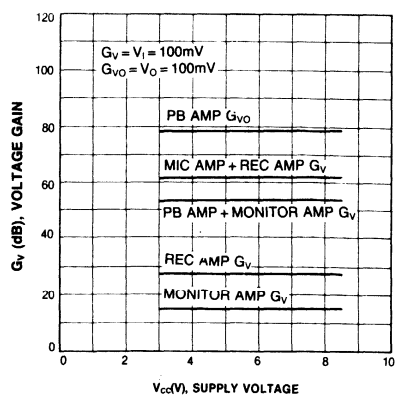
RIPPLE REJECTION RATIO-SUPPLY VOLTAGE



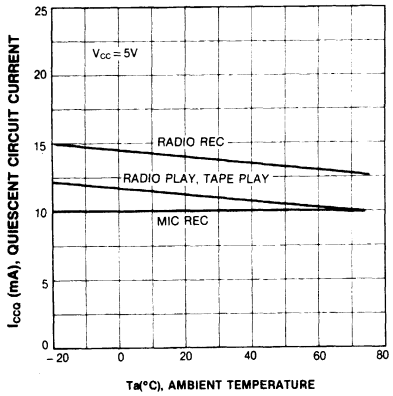
CROSS TALK-SUPPLY VOLTAGE



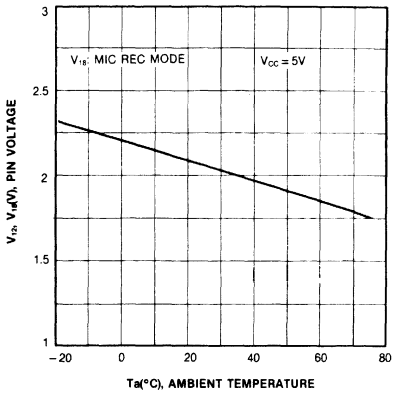
VOLTAGE GAIN SUPPLY-VOLTAGE



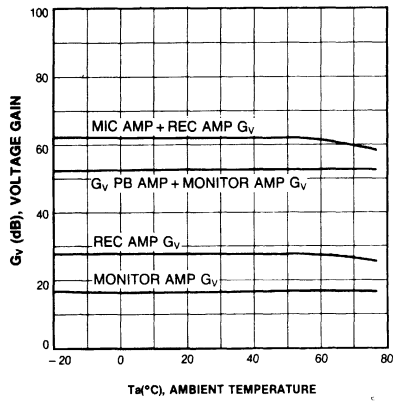
QUIESCENT CIRCUIT CURRENT
-AMBIENT TEMPERATURE



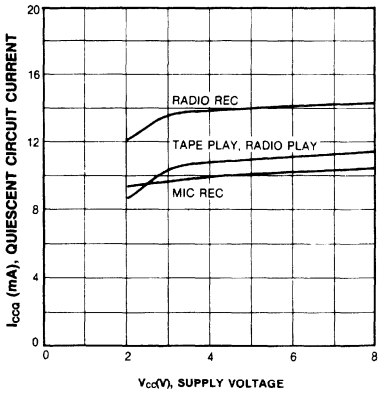
PIN 12, 18 VOLTAGE-AMBIENT TEMPERATURE



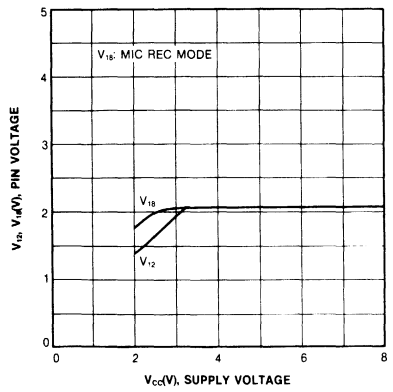
VOLTAGE GAIN AMBIENT TEMPERATURE



QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE



PIN VOLTAGE-SUPPLY VOLTAGE



APPLICATION INFORMATION

CONTROL SWITCH TERMINAL (2 , 6-PIN) THRESHOLD VOLTAGE

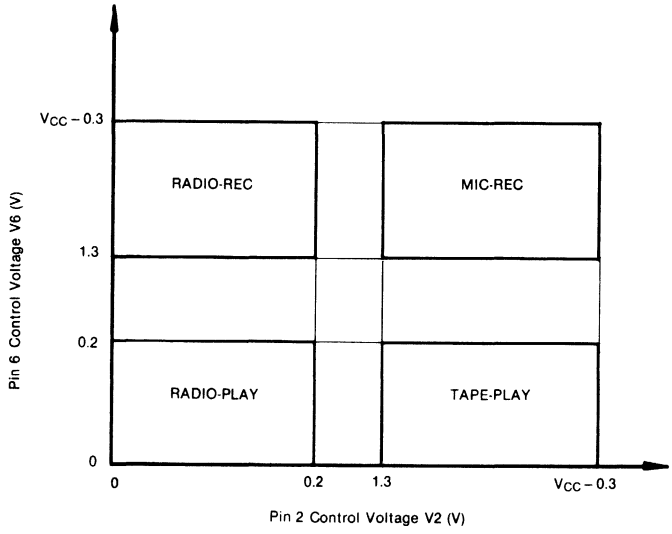


Fig. 3

APPLICATION CIRCUIT

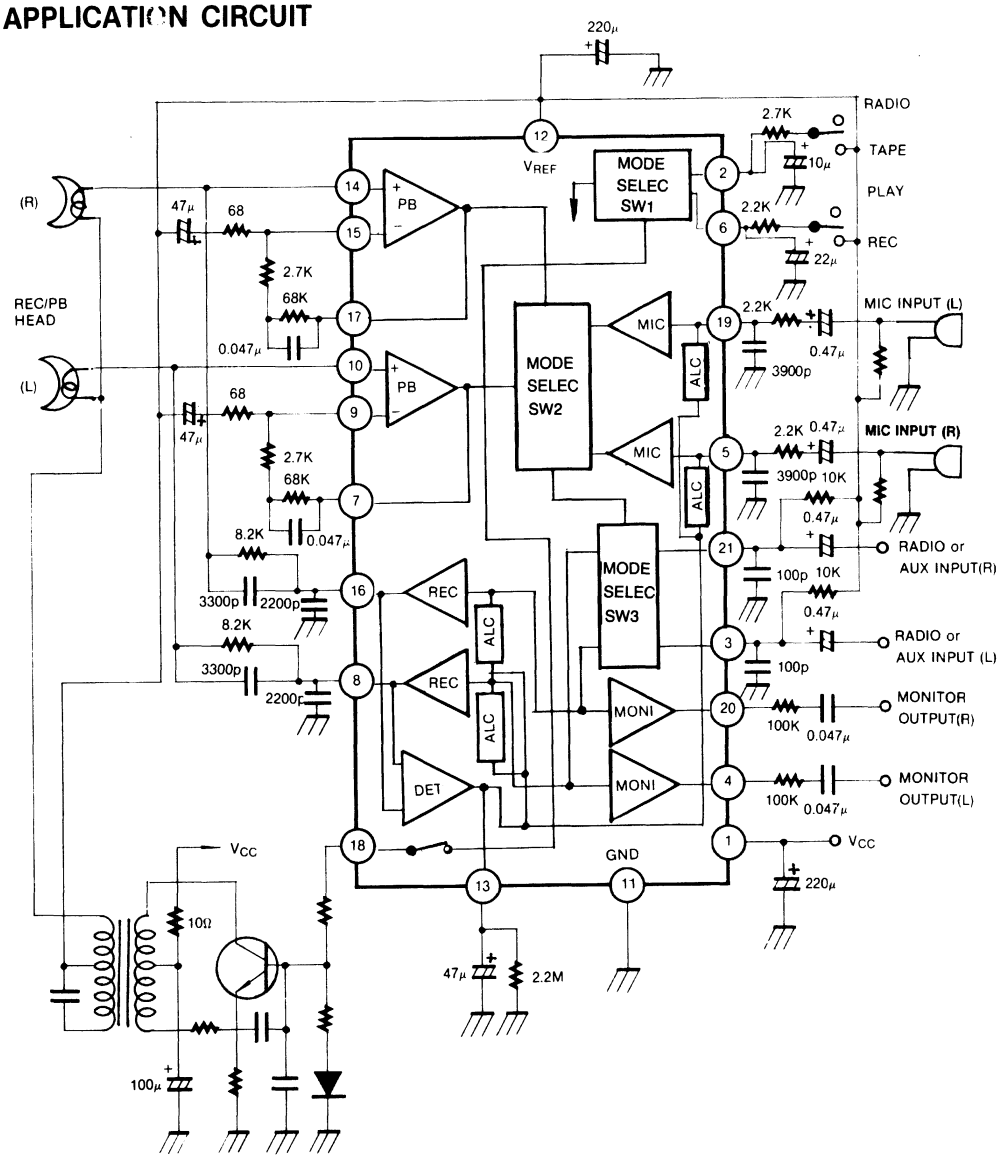
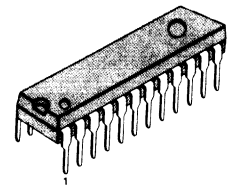


Fig. 4

PLAYBACK/RECORD PRE AMPLIFIER FOR DOUBLE DECK

The KA22291 is a monolithic integrated circuit consisting of a dual input playback amplifier, a channel for double or auto-reverse operation and a two-channel record amplifier.
It is suitable for 6V-9V double deck or auto-reverse cassette applications.

24 SDIP



FEATURES

- **Dual input two-channel playback amplifier**
- **Two-channel record amplifier**
- **Built in ALC and Muting circuit**
- **PB/REC and playback input select switch included**
- **Power ON ALC discharge circuit included**
- **Operating supply voltage: V_{CC} = 4V ~ 12V**
- **REC/PB power on quick start circuit**
- **Few external part required.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA22291	24 SDIP	-25°C ~ +75°C

BLOCK DIAGRAM

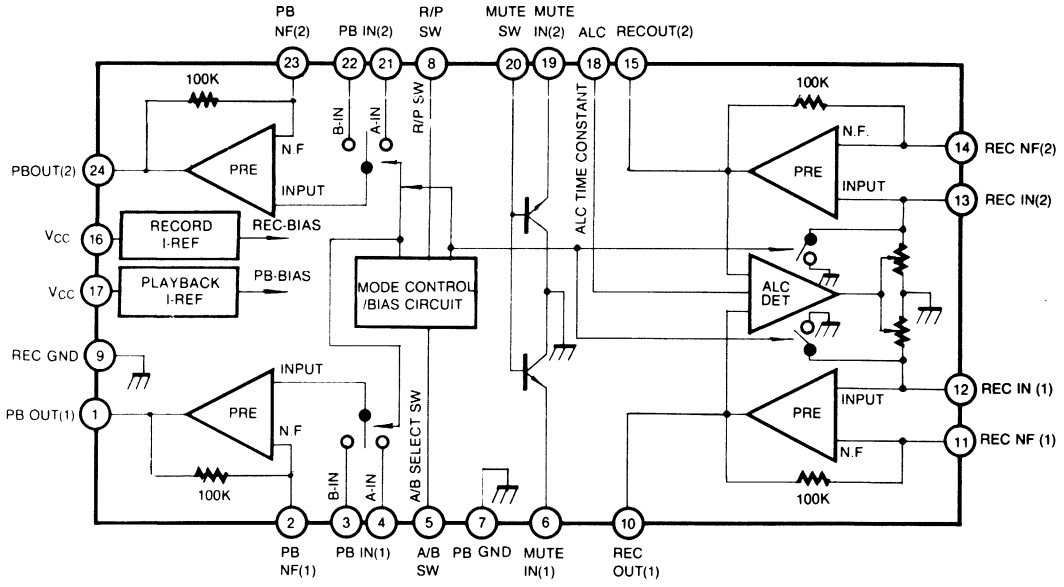


Fig. 1

* These specifications are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	12	V
Power Dissipation	P_D	1000	mW
Operating Temperature	T_{OPR}	−25 ~ +75	°C
Storage Temperature	T_{STG}	−55 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(T_a = 25°C, V_{CC} = 9V, f = 1KHz, unless otherwise specified)

	Characteristic		Symbol	Test Condition	Min	Typ	Max	Unit
	Circuit Current		I_{CCQ}	V_I = 0, REC MODE	10	18	26	mA
PLAYBACK	Open Loop Voltage Gain		G_{VO}	V_I = −80dBm	60	90		dB
PLAYBACK	Output Voltage		V_{O1}	THD = 1%, NAB	0.75	1.2		V
PLAYBACK	Total Harmonic Distortion		THD_1	V_O = 0.2V, NAB		0.05	0.3	%
PLAYBACK	Cross Talk	Ch to Ch	CT_1	V_O = 0.5V, NAB		−55	−45	dB
PLAYBACK	Cross Talk	Ain to Bin	CT_2	V_O = 0.5V, NAB		−55	−45	dB
PLAYBACK	Equivalent Input Noise Voltage		V_{NI}	Filter: 20Hz ~ 20KHz R_G = 2.2K, V_I = 0		1.2	2.2	μV
RECORD	Close Loop Voltage Gain		G_{VC}	V_I = 68dBm, ALC off	58	60	62	dB
RECORD	Output Voltage		V_{O2}	THD = 1%, ALC off	1.2	1.6		V
RECORD	Total Harmonic Distortion		THD_2	V_I = 68dBm, ALC off		0.2	1	%
RECORD	ALC Output Voltage		$V_{O(ALC)}$	V_I = −20dBm	0.75	0.95	1.35	V
RECORD	ALC THD		THD_{ALC}	V_I = −20dBm		0.2	1.0	%
RECORD	ALC Range		ΔV_{ALC}	V_I = −60dBm, +3dB UP	40	50		dB
RECORD	Cross Talk (ALC)		CT_3	V_I = −50dBm		−55	−40	dB
	RECORD TO PLAYBACK Cross Talk		CT_4	REC input = 0 PLAY output = 0.5V		−55	−40	dB
	Muting Range		MR	V_I = −20dBm		−55	−40	dB

*These specification are subject to change without notice.

TEST CIRCUIT

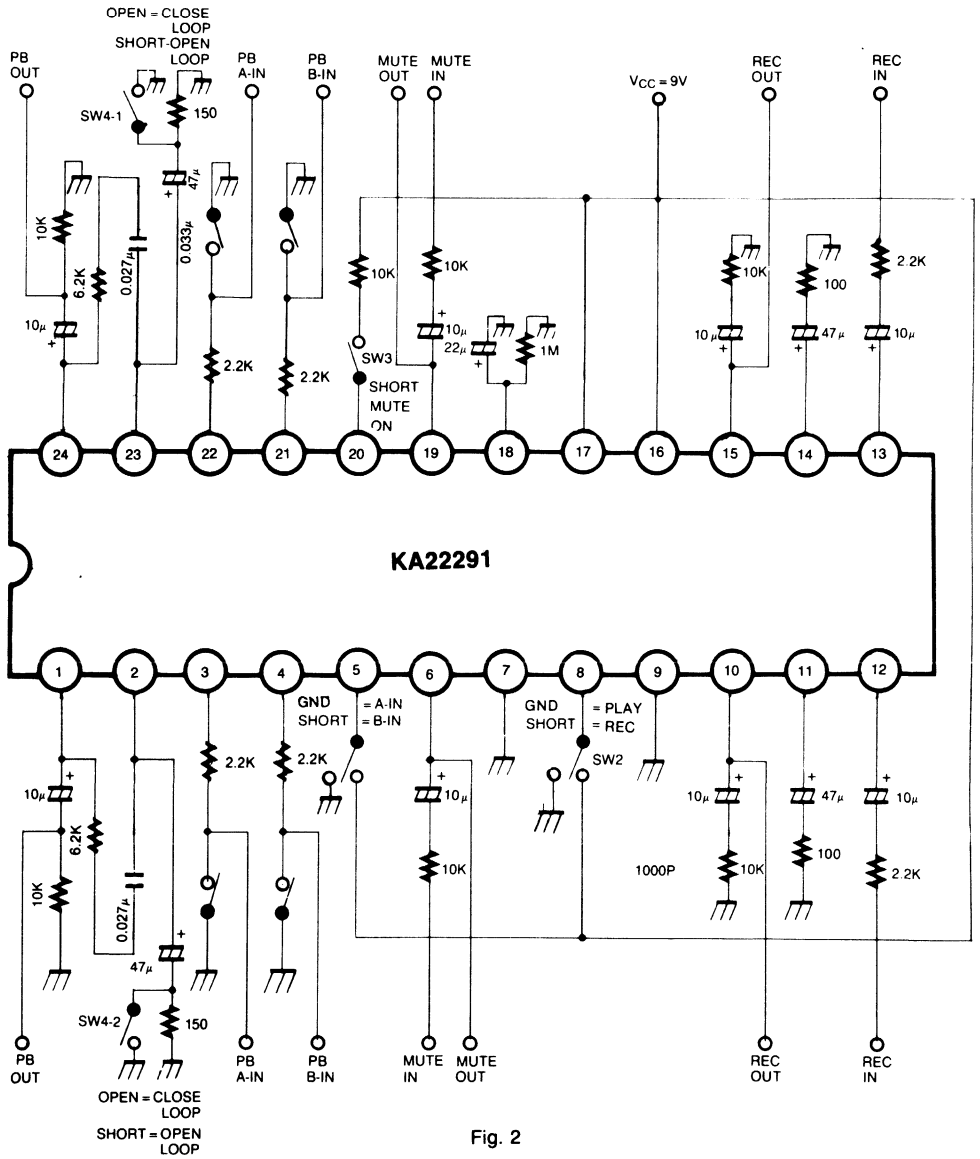


Fig. 2

* These specifications are subject to change without notice.

APPLICATION INFORMATION

1. R/P SWITCH

Apply R/P input voltage at PIN 8.
PLAY: 0V (GND)
REC: 4.5V ~ 12V (Don't apply 13V above).
Only valid A/B input select in playback mode.
In record mode, the playback A-input was available and the ALC was turned on by record bias.

A. RECORD MODE SCHEMATIC

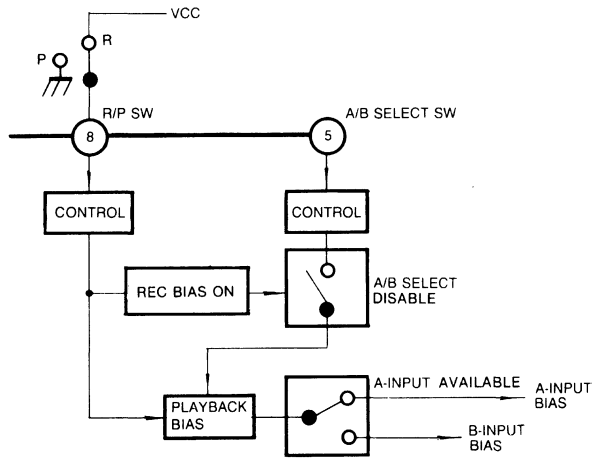


Fig. 3

B. PLAYBACK MODE SCHEMATIC

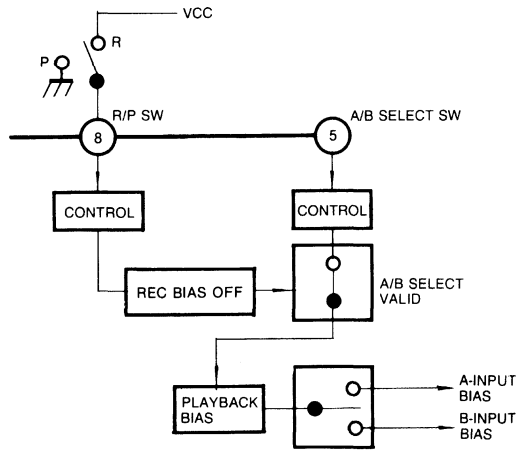


Fig. 4

* These specifications are subject to change without notice.

2. PLAYBACK A/B INPUT SELECT SWITCH (only playback mode)

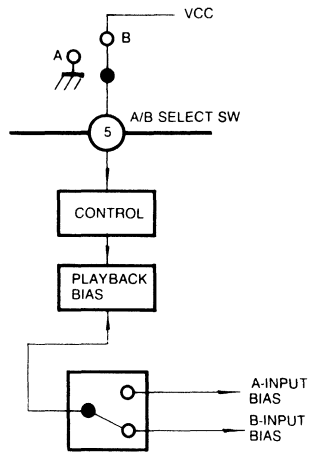
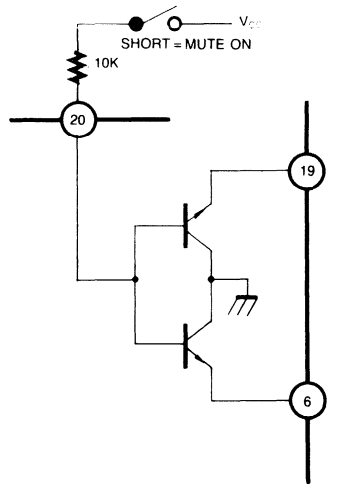


Fig. 5

3. MUTE SWITCH



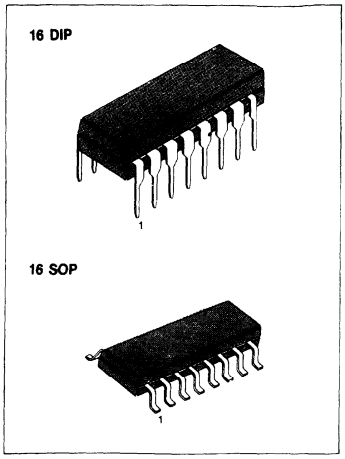
*THIS CIRCUIT IS OPERATED ON REVERSE SATURATION MODE

Fig. 6

*These specification are subject to change without notice.

AM 1-CHIP RADIO

The KA22421 is a monolithic integrated circuit designed for the portable AM radio.



FUNCTIONS

- Converter
- IF Amp
- AM DET
- Power Amp

FEATURES

- **Portable AM 1-chip radio.**
- **Low quiescent current: I_{CCQ} = 1.6mA (Typ) at V_{CC} = 3V.**
- **Operating supply voltage range: V_{CC} = 2V ~ 5V.**
- **High power efficiency**
- **Power output: P_O = 100mW (Typ) at THD = 10%.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA22421	16 DIP	-20°C ~ +70°C
KA22421D	16 SOP	

BLOCK DIAGRAM

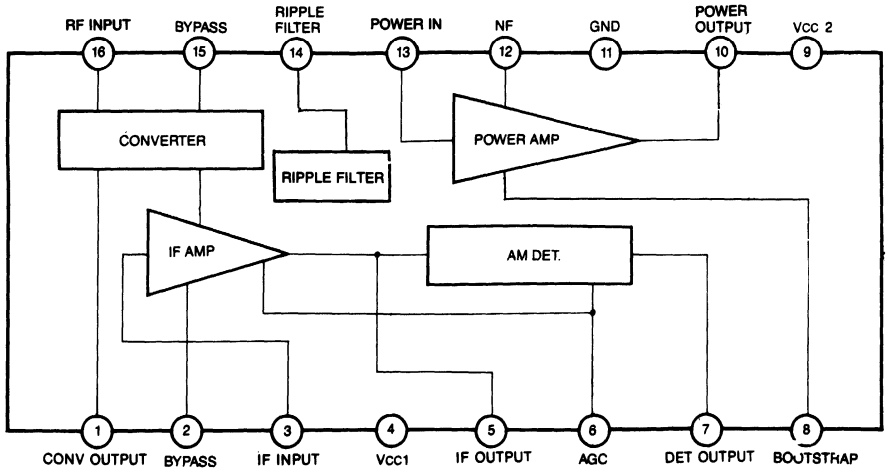


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Characteristic		Symbol	Value	Unit
Supply Voltage		V_{CC}	6	V
Power Dissipation	KA22421	P_D	750	mW
	KA22421D		350	
Output Peak Current		I_{PK}	0.2	A
Operating Temperature		T_{OPR}	−20 ~ +70	°C
Storage Temperature		T_{STG}	−55 ~ +150	°C

Note: Derated above T_a = 25°C in the proportion of 6mW/°C (KA22421D: 2.8mW/°C)

ELECTRICAL CHARACTERISTICS

(V_{CC} = 3V, f = 1MHz, f_m = 1KHz, 30% Mod, R_g = 50Ω, R_L = 8Ω, T_a = 25°C)

Characteristic	Symbol	Test Circuit	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CCQ}	1	V_I = 0	0.7	1.6	3.0	mA
Maximum Sensitivity	S_{MAX}	1	V_I = 20dBμ, VR = Max	200			mV
Output Power	P_O	1	V_I = 42dBμ, VR = Max	80	100		mW
Total Harmonic Distortion	THD	1	V_I = 42dBμ		2	6	%
Signal to Noise Ratio	S/N	1	V_O = 200mV		44		dB
Output Noise Voltage	V_{NO}	1	V_I = 0, VR = Max		3.5		mV

APPLICATION CIRCUIT

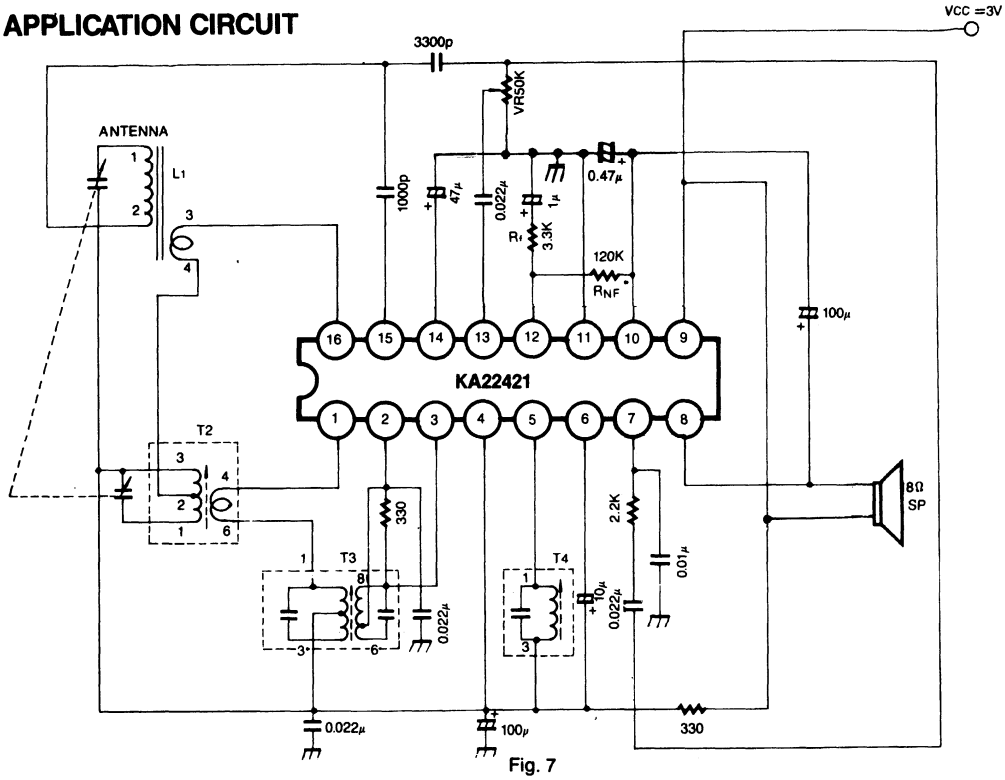


Fig. 7

TEST CIRCUIT 1

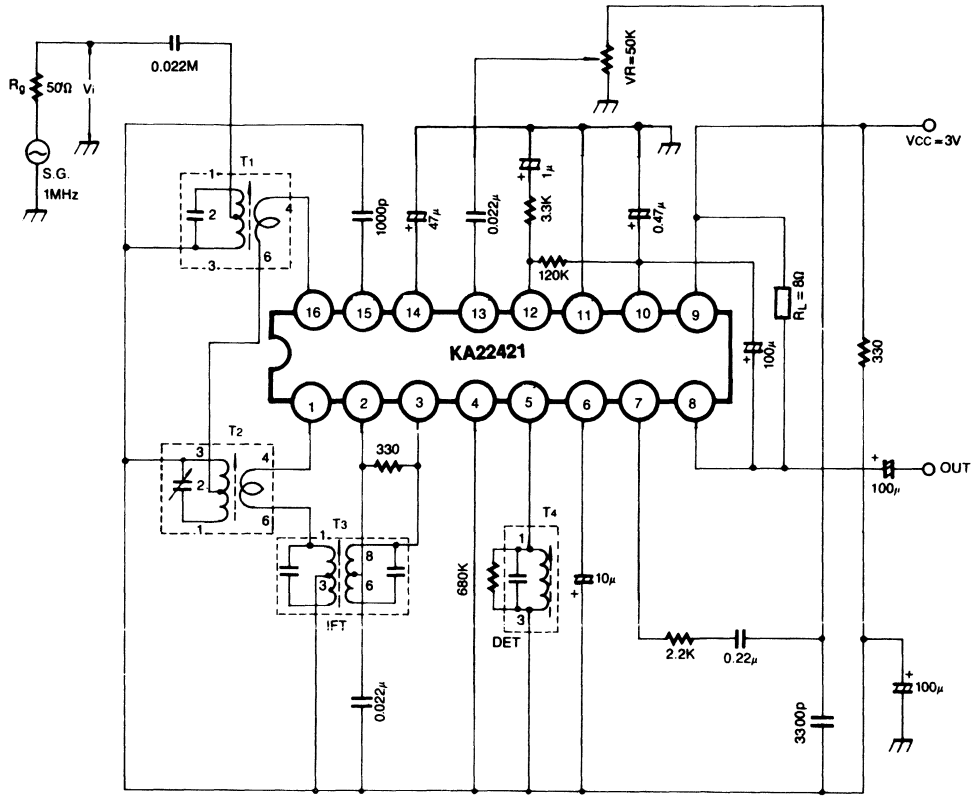
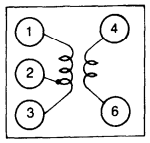


Fig. 2

COIL SPECIFICATIONS

T1 Antenna Coil



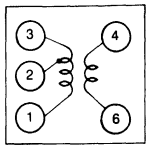
(Bottom View)

f (kHz)	L (μH)	Q_O	TURNS		
	1-3	1-3	1-2	2-3	4-6
300	600	115	2	130	8

KOREA TOKO

Wire: 0.07mmϕUEW

T2 OSC Coil



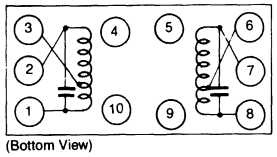
(Bottom View)

f (kHz)	L (μH)	Q_O	TURNS		
	1-3	1-3	1-2	2-3	4-6
796	360	125	92½	8	10½

KOREA TOKO

Wire: 0.08mmϕUEW

T3 AM IFT



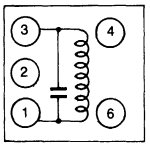
(Bottom View)

C_O (pF)		f (kHz)	Q_O	TURNS			
1-2	7-8		1-2	1-3	2-3	6-7	6-8
			7-8				
150	150	455	65	80	148	196	32

KOREA TOKO

Wire: 0.08mmϕUEW

T4 Detector Coil



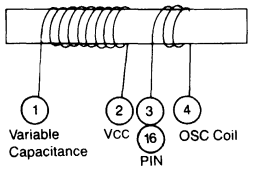
(Bottom View)

C_O (pF)	f (kHz)	Q_O	TURNS
1-3		1-3	1-3
180	455	65	142

KOREA TOKO

Wire: 0.08mmϕUEW

L1 Bar Antenna Coil

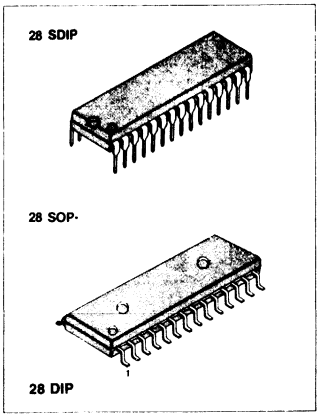


f (kHz)	L (μF)	Q_O	TURNS	
	1-2	1-2	1-2	3-4
796	625	200 Min	105	20

Core: 12mmϕ x 52mmϕ
Wire: USTC-0.1mmϕ

AM/FM ONE-CHIP RADIO

The KA22426 is a monolithic integrated circuit designed for radio-cassette tape recorders, clock radios and headphone radios.



FUNCTIONS

- AM/FM RF AMP
- Local OSC
- AM AGC Control
- FM AFC Control
- Audio Power AMP
- Tuning Indicator
- DC Volume
- AM/FM IF AMP
- FM Quadrature DET
- AM DET

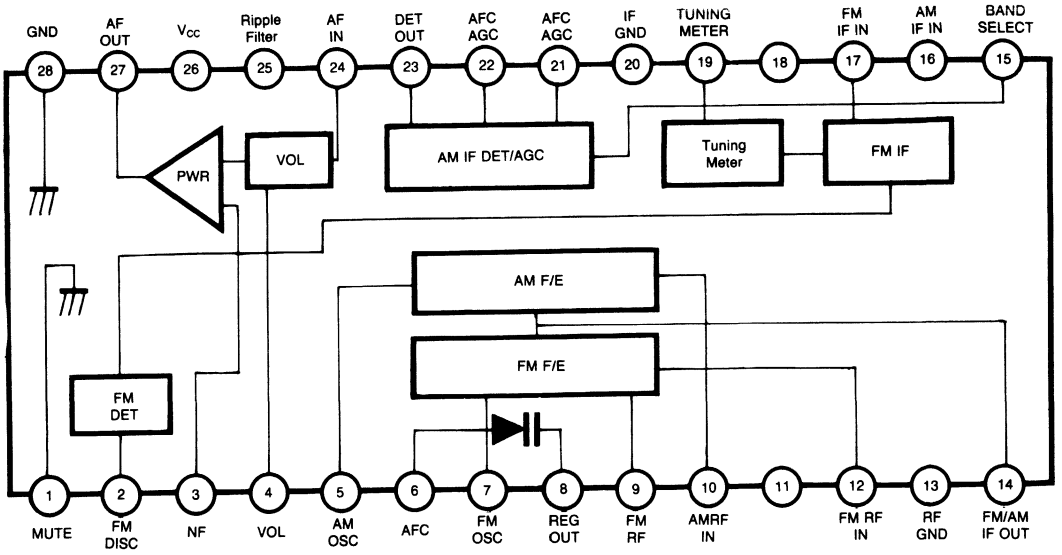
FEATURES

- **Built-in AM/FM Switching Circuit**
- **Wide operating supply voltage: V_{CC} = 2 ~ 8.5 V**
- **Low current consumption (V_{CC} = 3V)**
  FM: I_{CCQ} = 5.3mA (typ)
  AM: I_{CCQ} = 3.4mA (typ)
- **High Power Audio Amplifier: 0.5W(typ) at V_{CC} = 6V, RL = 8Ω, THD = 10%**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA22426	28 DIP	-20 ~ +70°C
KA22426D	28 SOP	
KA22426M	28 SDIP	

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	9	V
Power Dissipation	P_D	1000	mW
Operating Temperature	T_{OPR}	−20 ~ +70	°C
Storage Temperature	T_{STG}	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 6V, Ta = 25°C, FM; Δf = 22.5KHz, fm = 1KHz, AM; 30% Mod unless otherwise specified)

	Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
FM	Quiescent Circuit Current	I_{CCQ}	V_I = 0		7.0	14.0	mA
	F/E Voltage Gain	G_{V1V}	$V_I(1)$ = 40dBμ, f = 100MHz, Δf = 0	32	39	46	dB
	Detect Output Gain	$V_O(1)$	$V_I(3)$ = 90dBμ, f = 10.7 MHz	−26	−20	−14	dBm
	IF-3dB Sensitivity	$V_{I(LIM)}$	$V_O(V_I3)$ = 90dBμ − 3dB, f = 10.7 MHz		24	32	dBμ
	Total Harmonic Distortion	THD_1	$V_I(3)$ = 90dBμ, f = 10.7MHz (Δf = 75KHz)		0.3	2.0	%
	Meter Drive Current	$I_M(1)$	$V_I(3)$ = 60dBμ, f = 10.7MHz	1.8	3.5	7.0	mA
AM	Quiescent Circuit Current	$I_{CCQ}(2)$	V_I = 0		3.5	10.0	mA
	F/E Voltage Gain	$G_V(2)$	$V_I(2)$ = 60dBμ, f = 1660KHz, m = 0%	15	22	29	dB
	IF Voltage Gain	$G_V(3)$	$V_O(3)$ = −34dBm, f = 455KHz	14	20	27	dBμ
	Detect Output Voltage	$V_O(2)$	$V_I(3)$ = 85dBμ, f = 455KHz	−26	−20	−14	dBm
	Total Harmonic Distortion	THD_2	$V_I(2)$ = 95dBμ, f = 1660KHz, V_{CC} = 7.8V		0.6	2.0	%
	Meter Drive Current	$I_M(2)$	$V_I(3)$ = 85dBμ, f = 455KHz	1.3	3.0	7.0	mA
AF	Closed Loop Voltage Gain	$G_V(4)$	$V_O(4)$ = 0dBm, f = 1KHz	27	31.5	36	dB
	Total Harmonic Distortion	THD_3	P_O = 50mW, f = KHz		0.3	2.5	%
	Output Power	P_O	R_L = 8Ω, THD = 10%, f = 1KHz	0.4	0.5		W

APPLICATION CIRCUIT

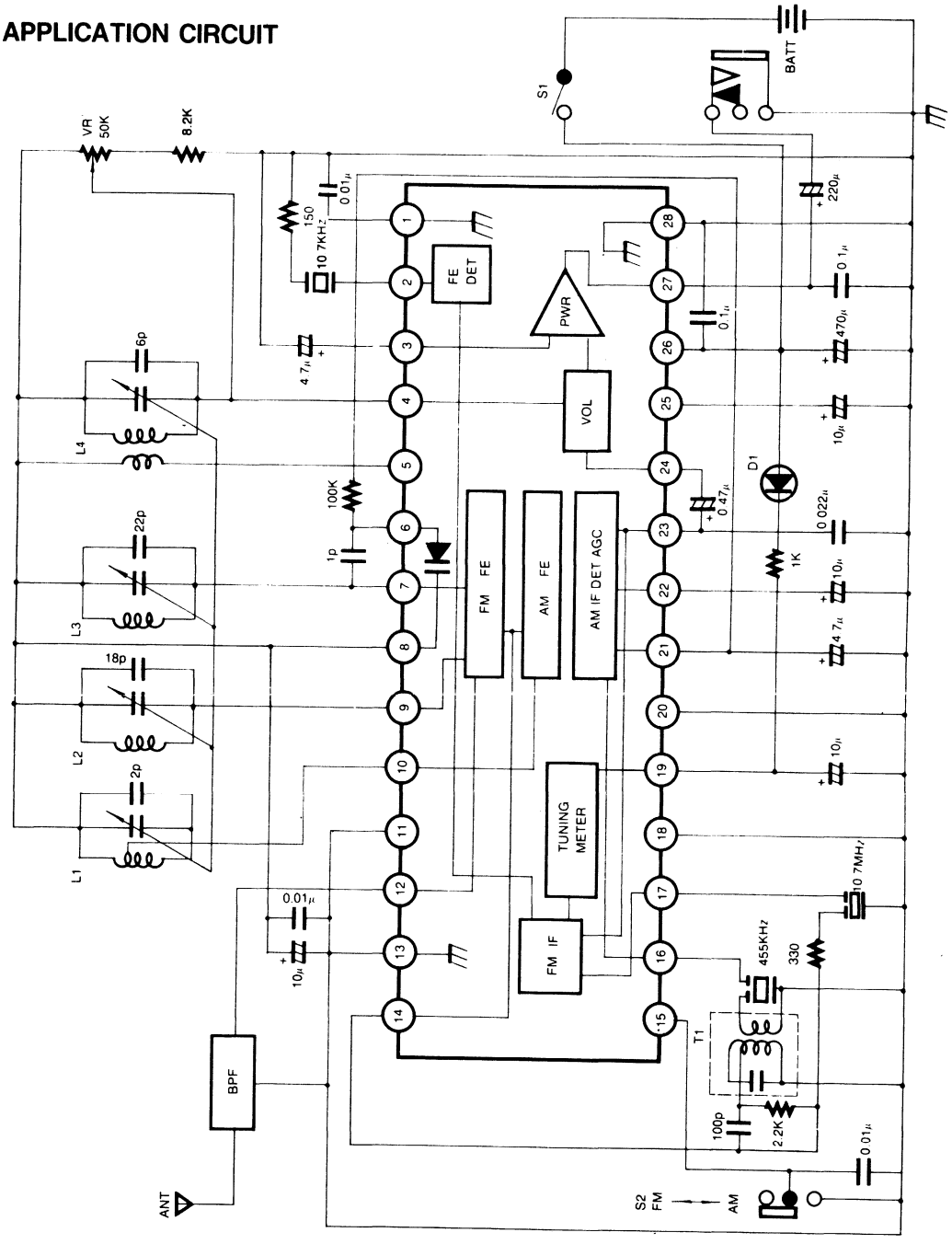
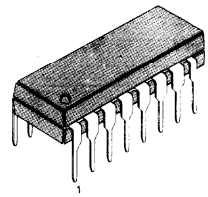


Fig. 3

AM/FM 1-CHIP RADIO

KA22427 is a monolithic integrated circuit designed for the portable AM/FM radio or AM/FM clock radios.

16 DIP



FUNCTIONS

- AM RF & MIX
- AM AGC
- AM/FM DET
- Regulator
- AM Local OSC
- AM/FM IF AMP
- Audio Power AMP
- FM AFC Control

FEATURE

- **Portable AM/FM 1-chip radio**
- **Wide operating supply voltage range: V_{CC} = 3V ~ 12V (Approximately) (Depending on the internal regulator tolerance)**
- **Recommended operating supply voltage: V_{CC} = 4.5V ~ 9V**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA22427	16 DIP	-20°C ~ +70°C

R_L \ V_{CC}	4.5V	6.0V	7.5V	9.0V	Line Operated
8Ω	O	O	O	X	X
16Ω	O	O	O	O	X
45Ω	O	O	O	O	O

- On using AC line as an internal shunt regulator mode, it is possible to use low cost application without a transformer (approximately 42mA)
- IF AMP gain is determined by DC voltage appeared at IC Pin 16.
- Power output: P_o = 0.28W (Min.) at THD = 10% (V_{CC} = 5.5V/8Ω).

BLOCK DIAGRAM

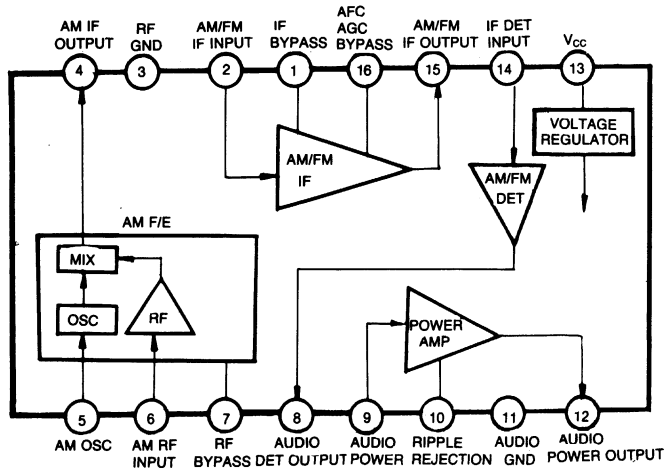


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	13	V
Power Dissipation (Note) Ta≤65°C	P_D	600	mW
Supply Current	I_{CC}	44	mA
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	100	°C/W
Operating Temperature	T_{OPR}	− 20 ~ + 70	°C
Storage Temperature	T_{STG}	− 55 ~ + 150	°C

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 5.5V, f_m = 1KHz, AM: f = 1MHz, 30% Mod, FM: f = 10.7MHz
△f = 22.5KHz, Unless otherwise specified)

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit
FM	Quiescent Circuit Current	I_{CCQ}	SW: FM, V_{CC} = 3V	10	15	20	mA
			SW: FM, V_{CC} = 9V	13	20	26	
	Pin 16 Terminal Voltage	V_{16} (FM)	SW: FM, V_{CC} = 9V, V_I = 0	2.0	2.4	3.1	V
	− 3dB Limiting Sensitivity	$V_{I\,(LIM)}$	SW: FM, − 3dB V_{16} = 2.4V, V_R Min		57		dBμ
AM	Internal Regulated Vtg.	V_{CC}	SW: AM, I_{CC} = 42mA	12	13.2	14.0	V
	Pin 16 Voltage	V_{16} (AM)	SW: AM, V_{CC} = 9V, V_I = 0	1.4		1.9	V
	Maximum Sensitivity	S_{MAX}	SW: AM, V_{CC} = 12V V_I = 37dBμ, R_L = 45Ω	1.5	3.0		V
	Signal to Noise Ratio	S/N	V_I = 37.5dBμ, R_L = 8Ω P_o = 50mW	15	20		dB
PWR AMP	Output Power	P_o	f = 1KHz, THD = 10% V_R Min, R_L = 8Ω	0.28			W
	Total Harmonic Distortion	THD	I_{CC} = 42mA, R_L = 45Ω f = 1KHz, V_o = 2V V_R Min		0.5	4.0	%
	Voltage gain	G_V	f = 1KHz, R_L = 8Ω P_o = 50mW		41		dB

TEST CIRCUIT

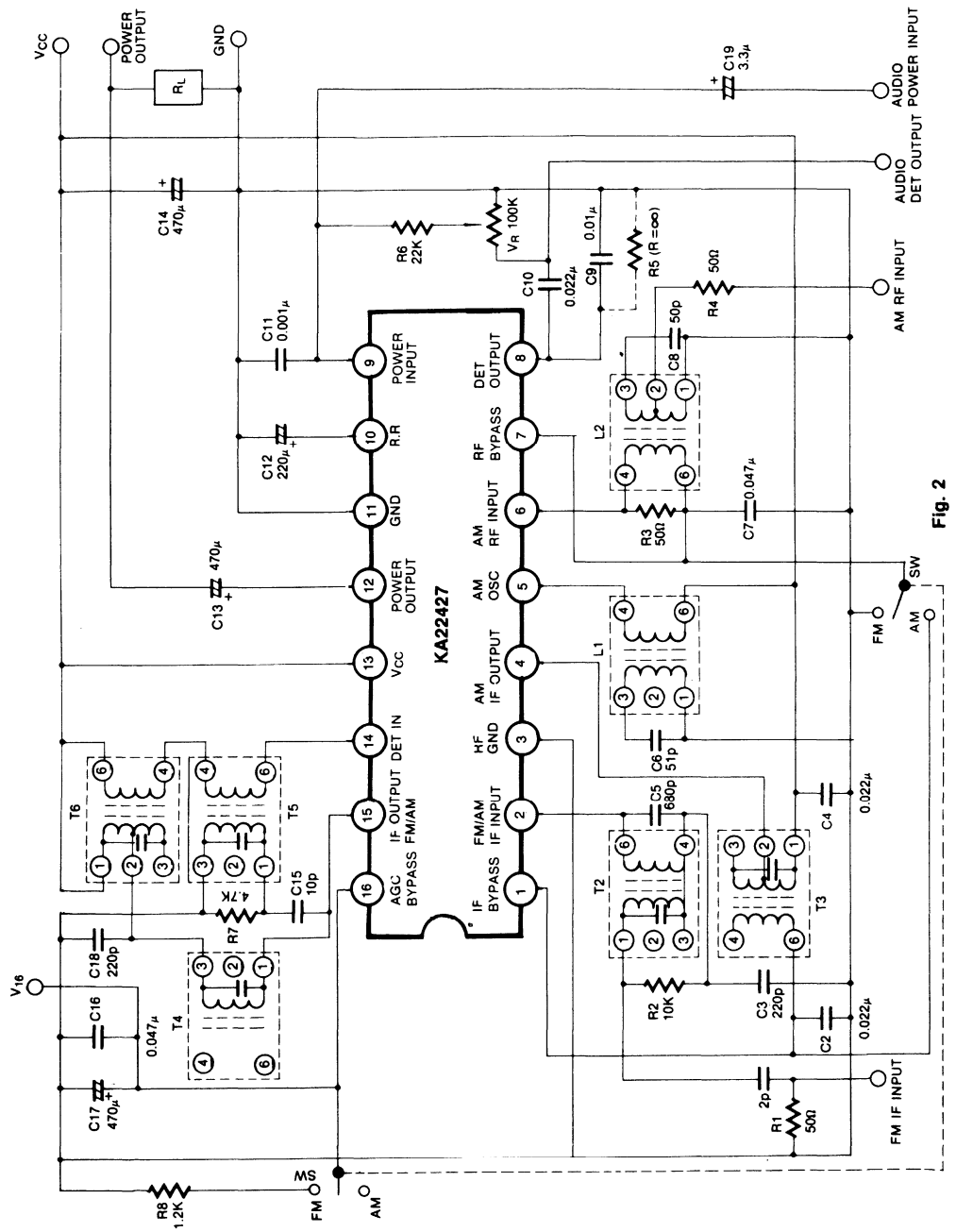


Fig. 2

APPLICATION INFORMATION

- EXTERNAL COMPONENTS

Parts Number	Purpose	Typical	Influence	
			Smaller Than Typ	Greater Than Typ
R5	AM Gain Control	47KΩ (33K~∞)	Low AM Gain	AGC Distortion Increase, High Gain
R7	FM Detector Damper	4.7KΩ	Low Detector Output, Stable IF Gain, Low FM Gain	Sharp IF AMP Curve
R8	FM Gain Adjust	470	Low FM Gain	High Gain, but Noise Increases
C2	IF Bypass	0.022μF	Should Not Be Less Than 0.005μF	High IF Gain, S/N Ratio Degrade
C4	IF Filter	0.022μF	Removal May Cause IF Oscillation	No Influence
C7	AM Bypass	0.047μF	Low Gain	Using over 1μF Will Cause FM Distortion at Small Signal
C9	Detector Filter	0.01μF	Unstable IF AMP Oscillation	Poor FM Frequency Response
C10	Audio Coupling	0.022μF	Lower Sensitivity, Poor Low Frequency Response	Bass Boost Affects De-emphasis Curve
C11	Audio Input High-Cut	0.001μF	Audio Oscillation	Poor Response
C12	Ripple Filter	220μF	Poor Frequency Response & Low Gain	Improves AC Hum
C13	Audio Output Coupling	470μF	Poor Low Frequency Response	Can Achieve Optimum Output Power
C14	Power Line Filter	470μF	Poor AC Hum	Improves AC Hum
C15	FM Detector Phase-Shift	10pF	Narrow IF Bandwidth	Wide IF Bandwidth
C16	High Freq. (IF) Bypass	0.047μF	Removal Will Cause FM Oscillation	No Influence
C17	AM AGC Time Constant and High Frequency (IF) Bypass	0.047μF	Not Recommend to Charge	

FUNCTION DESCRIPTION (Pin 16 DC Voltage)

1. IF Gain Grouping Table
   (1) Test Condition: V_{CC} = 9V (Pin 13).
   Pin 8 resistance (AM) = 47KΩ.
   Pin 16 resistance (FM) = 1.2KΩ.
   (2) Grouping Table

V16 (FM) \ V16 (AM)	1.4 – 1.7V	1.7 – 1.9V
2.6 – 3.0V	C1	C2

2. IF gain is determined by DC voltage appeared at IC Pin 16.
   The DC voltage at Pin 16 to the following values:
   AM = 1.4 ~ 1.65V (DC)
   FM = 1.9 ~ 2.10V (DC)
   AM gain can be adjusted by the loading resistor value of Pin 8 (AM) from 33KΩ to infinity.
   FM gain can be adjusted by the loading resistor vale of Pin 16 (FM) from 390Ω to 680Ω.
   Recommended resistance (Pin 8, Pin 16).
   Pin 8 (AM) = 47KΩ
   Pin 16 (FM) = 470Ω

APPLICATION CIRCUIT 1

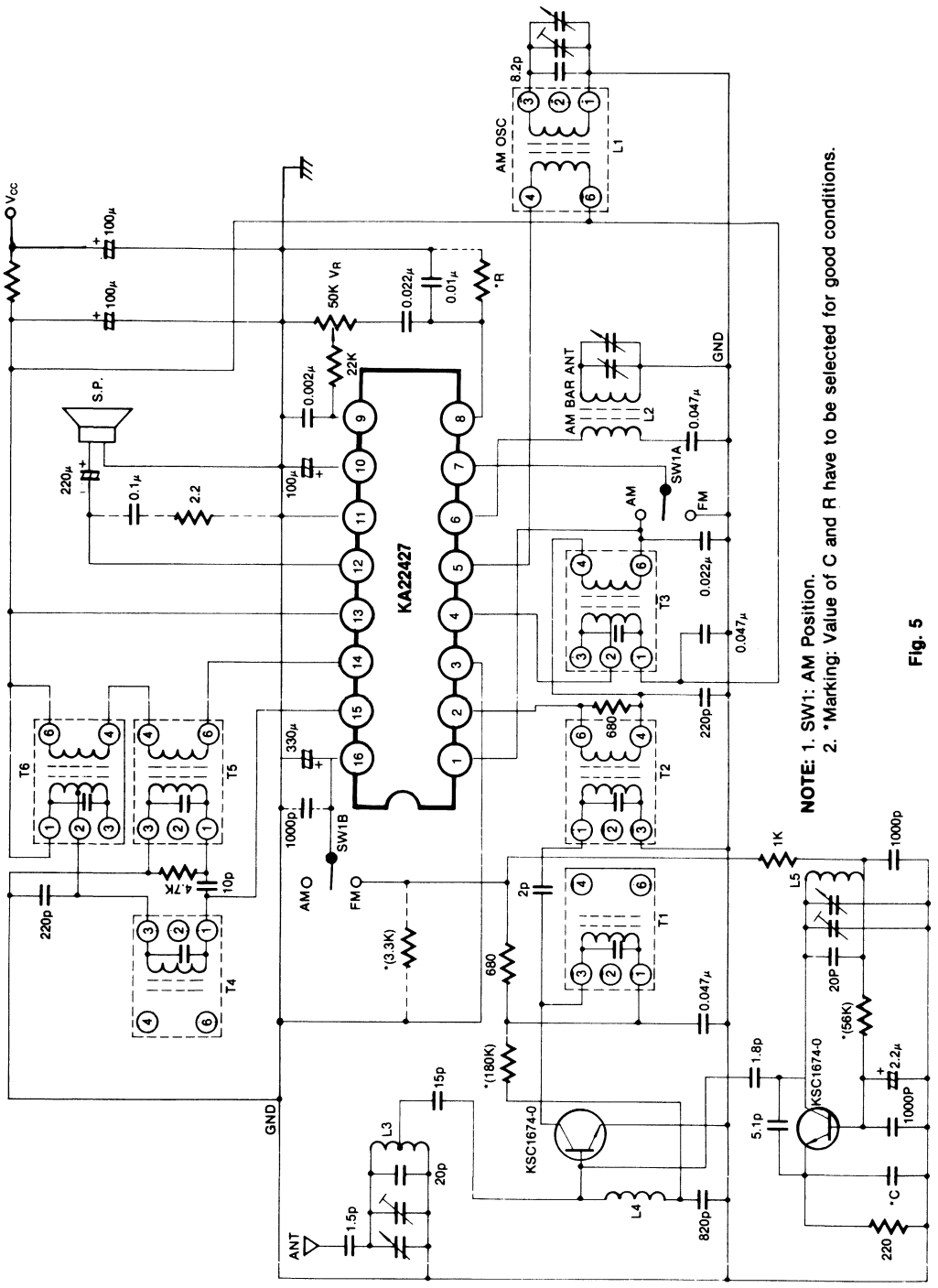
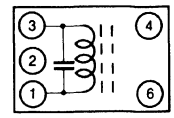
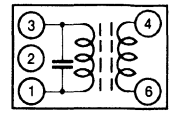
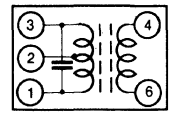
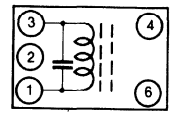
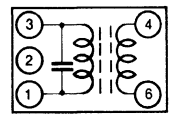
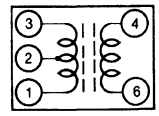
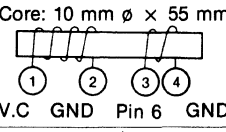
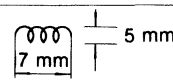
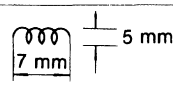
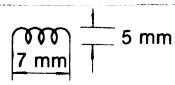
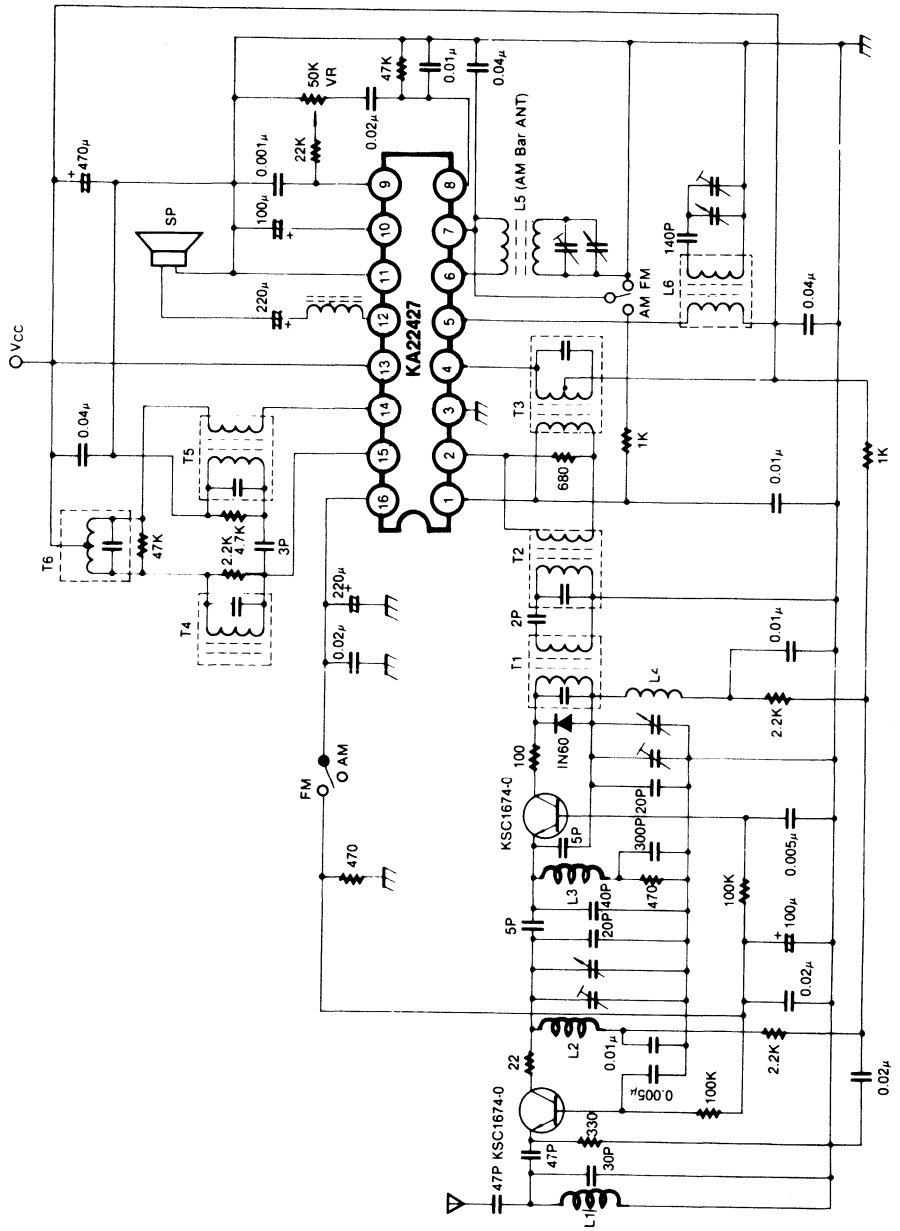


Fig. 5

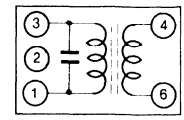
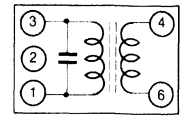
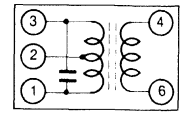
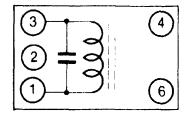
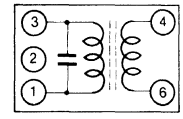
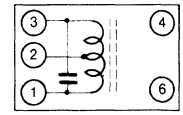
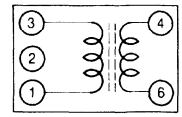
COIL SPECIFICATION 1

Coil No.	f	Q_o	Turns		C_o	Connections
T1	10.7MHz	120	1 – 3	8T	150pF	
T2	10.7MHz	70 min	1 – 3 4 – 6	11T 2T	75 ± 5pF	
T3 (T6)	455KHz	80 min	1 – 2 2 – 3 4 – 6	91T 55T 6T	180 ± 5pF	
T4	10.7MHz	45 min	1 – 3	11T	82 ± 3pF	
T5	10.7MHz	25 min	1 – 3 4 – 6	7T 7T	180pF	
L1	AM Local Oscillator	90 min	1 – 3 4 – 6	86T 7T		
L2	AM ANT	200	1 – 2 (L = 560μH) 3 – 4	138T 9T		
L3	FM ANT		0.8 mm ø UEW TAP	5T 0.5T		
L4	Trap		0.32 mm ø UEW	10T		
L5	FM Oscillator		0.8 mm ø UEW	4T	—	

APPLICATION CIRCUIT 2



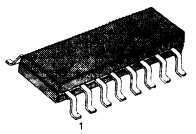
COIL SPECIFICATION 2

Coil No.	f	Q_0	Turns		C.L.	Connections
T1	10.7MHz	90	1 – 3	11	82pF	
			4 – 6	3		
T2	10.7MHz	60	1 – 3	5	390pF	
			4 – 6	2		
T3	455KHz	100	1 – 2	127	180pF	
			2 – 3	28		
			4 – 6	10		
T4	10.7MHz	45 (Min)	1 – 3	11	82pF	
T5	10.7MHz	25 (Min)	1 – 3	7	180pF	
			4 – 6	7		
T6	455KHz	100	1 – 2	50	390pF	
			2 – 3	50		
L6	796KHz	100	1 – 3	100	360μH	
			4 – 6	10		

FM ONE CHIP RADIO

The KA22429 is a monolithic integrated circuit designed for Portable FM radio.
It is consisting of a RF input stage, Mixer, IF, Mute control and Loop (earphone drive) AMP.
It is suitable a pocket-size radio.

16 SOP



FUNCTIONS

- RF input stage
- Local osc
- Mixer
- IF amp
- Mute control
- Earphone drive amp.

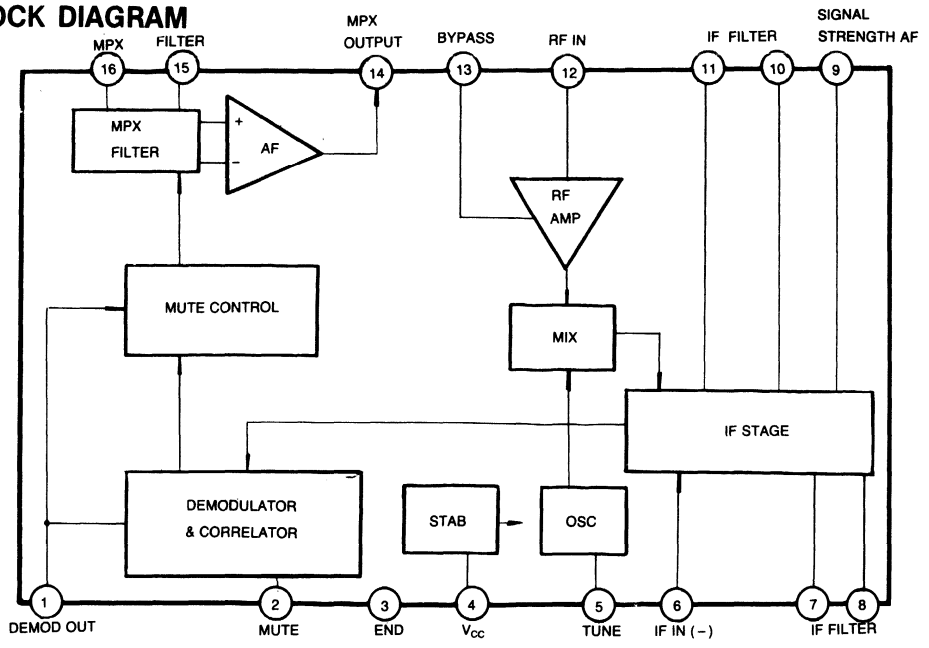
FEATURES

- **Minimum number of external parts required**
- **It is able to a single trimmer tuning**
- **No FM det coil**
- **It is FLL IF detect system (76KHz)**
- **Operating voltage: V_{CC} = 1.8V ~ 6.0V**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA22429D	16 SOP	- 10°C ~ + 70°C

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	7	V
Oscillator Voltage	V_{OSC}	−0.5 ~ +0.5	V
Operating Temperature	T_{OPR}	−10 ~ +70	°C
Storage Temperature	T_{STG}	−55 ~ +150	°C
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	300	K/W

ELECTRICAL CHARACTERISTIC

MONO CONDITION: f = 98MHz, f_m = 1KHz, Δf = ±22.5KHz, V_I = 50dBμ, Ta = 25°C, V_{CC} = 3V
STEREO CONDITION: f = 98MHz, f_m = 1KHz, Δf = ±22.5KHz, V_I = 60dBμ (Modulated with pilot Δf = ±6.75KHz)

	Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
	Quiescent Circuit Current	I_{CCQ}	V_I = 0		6.3		mA
MONO	Sensitivity	S_{VI1}	−3dB: Mute Disable		12		dBμ
		S_{VI2}	S/N = 26dB: Mute Enable		17		dBμ
	Signal to Noise Ratio	S/N_1			60		dB
	Total Harmonic Distortion	THD_1	Δf = ±22.5KHz		0.7		%
		THD_2	Δf = ±75KHz		2.3		%
	AM Rejection Ratio	AMR	AM: fm = 1KHz, m = 80% FM: fm = 1KHz, Δf = 75KHz		50		dB
	Oscillator Voltage	V_{OSC}			250		mV
	AFC Range	ΔAFC			160		KHz
	Mute Range	MR			120		KHz
	Band Width	BW	ΔV_O = 3dB Pre-Emphasis t = 5KHz		10		KHz
	AM Output Voltage	V_{O1}			90		μV
STEREO	Sensitivity	S_{VI3}	S/N = 46dB		49		dBμ
	Signal to Noise Ratio	S/N_2			53		dB
	Channel Separation	CS			20		dB
	AF Output Voltage	V_{O2}			80		mV

TEST CIRCUIT

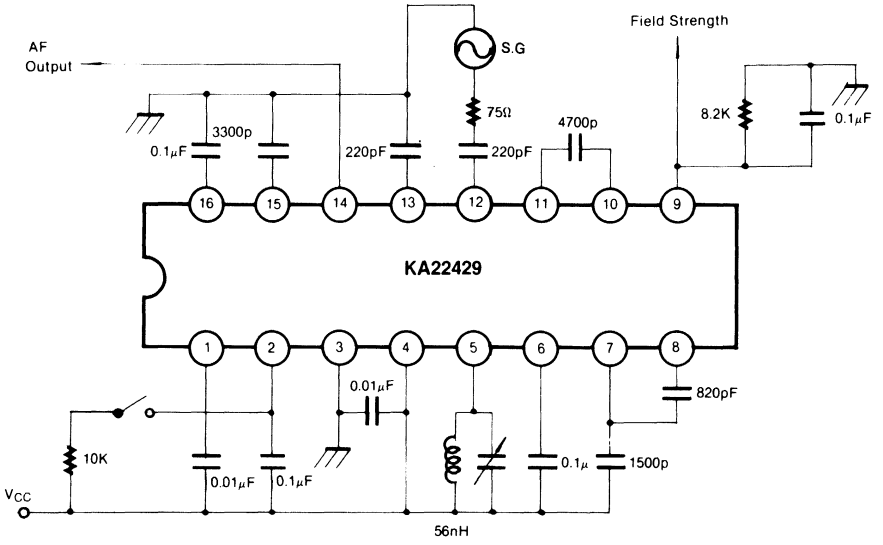


Fig. 1 Test Circuit for Mono Operation

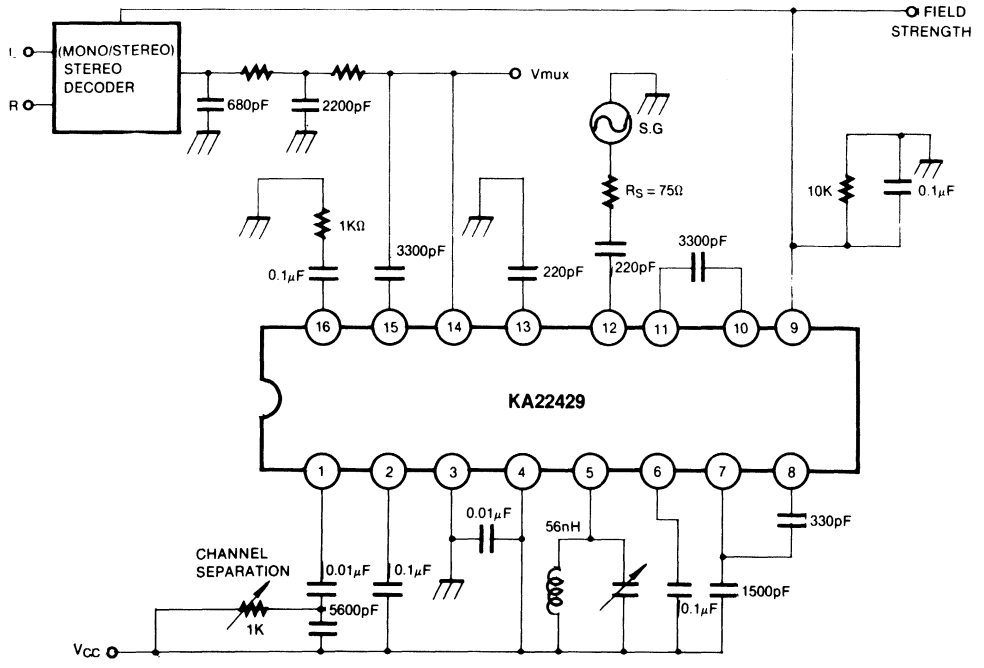
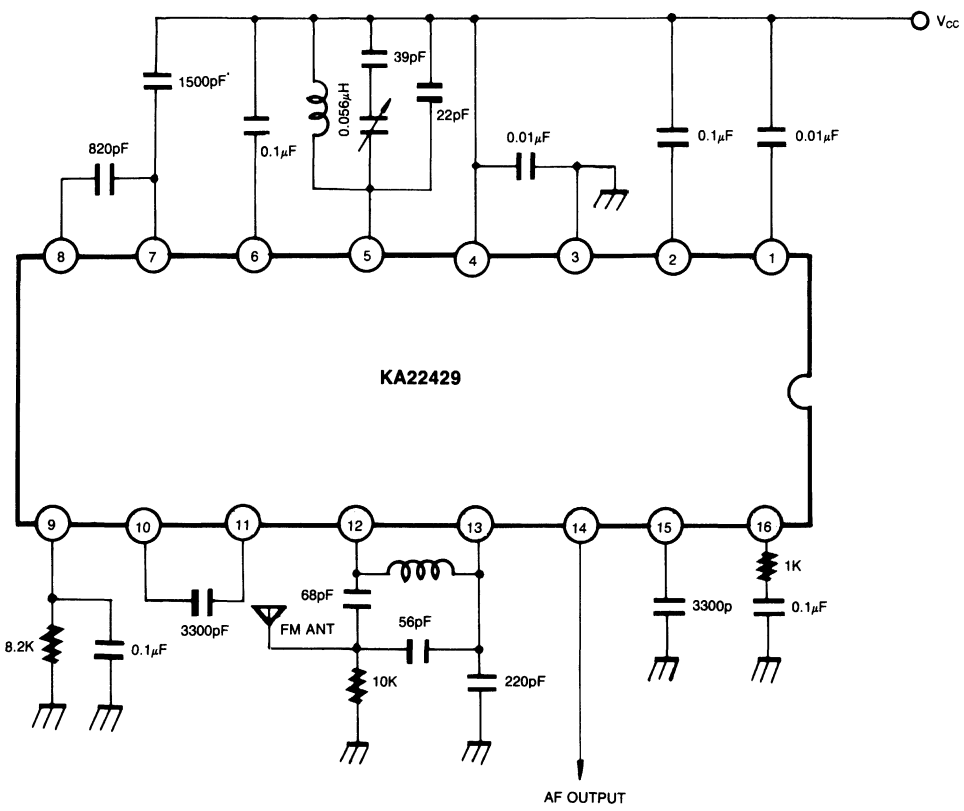


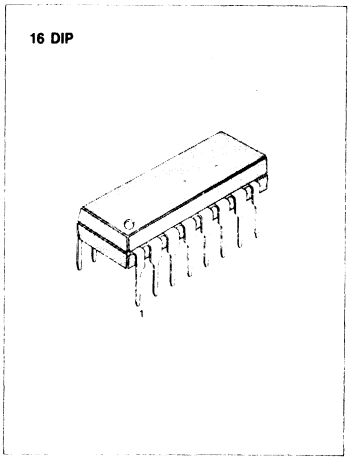
Fig. 2 Test Circuit for Stereo Operation

APPLICATION CIRCUIT



AM/FM IF SYSTEM

The KA2243 is a monolithic integrated circuit developed for radio cassette tape recorders which include AM/FM IF amplifier and detector.



FUNCTIONS

- AM Section:
  IF amplifier with AGC detector.
  Signal meter driver circuit.
  Voltage regulator for RF external circuit.
- FM Section:
  IF amplifier.
  Quadrature detector.
  Post amplifier.
  Signal meter driver circuit.

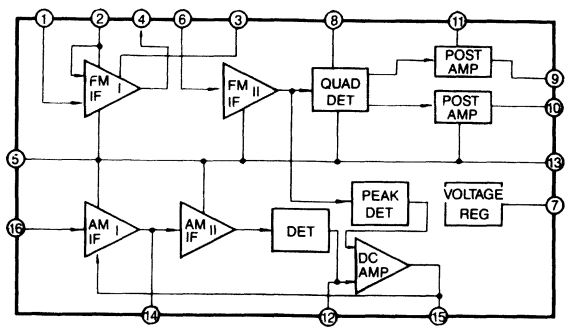
FEATURES

- **Suitable for radio cassettes and home stereos.**
- **Wide operating supply voltage range: V_{CC} = 3V ~ 14V.**
- **Low quiescent circuit current.**
- **AM section.**
  Simplified input circuit IFT (Ceramic filter type).
  RF AGC available.
- **FM section.**
  High limiting sensitivity (33dBμ, Typ).
  Low residual noise (45dB at V_i = −10dBμ).
  Small side peak of detuned output voltage.

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2243	16 DIP	−20°C ~ +70°C

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Power Dissipation	P_D	600	mW
Operating Temperature	T_{OPR}	−20 ~ +70	°C
Storage Temperature	T_{STG}	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(T_a = 25°C, V_{CC} = 5.5V, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
FM Section (f = 10.7MHz, fm = 1KHz, Δf = ± 75KHz)						
Quiescent Circuit Current	I_{CCQ}	V_I = 0	7	11	16.5	mA
−3dB Limiting Sensitivity	$V_{I\ (LIM)}$	V_O (V_I = 100dBμ)-3dB		33	38	dBμ
Detector Output Voltage	$V_{O\ (DET)}$	V_I = 100dBμ	180	245	310	mV
Total Harmonic Distortion	THD	V_I = 100dBμ		0.3	1.0	%
AM Rejection Ratio	AMR	V_I = 100dBμ	50	60		dB
Signal to Noise Ratio	S/N	V_I = 100dBμ	72	83		dB
Signal Meter Output	V_M	V_I = 100dBμ	1.05	1.5	2.05	V
Residual Noise	V_N	V_O (AF) (V_I = 100dBμ) V_O (AF) (V_I = −10dBμ)		45		dB
Muting Attenuation	ATT_{MUTE}	V_I = 37dBμ, Mute SW on		35		dB
AM Section (f=455KHz, fm=1KHz, 30% Mod)						
Quiescent Circuit Current	I_{CCQ}	V_I = 0		8		mA
Maximum Sensitivity	S_{MAX}	V_O (AF)=10mV		29		dBμ
Detector Output Voltage	V_O	V_I = 74dBμ	45	65	85	mV
Total Harmonic Distortion	THD	V_I = 74dBμ		0.3	2.0	%
		V_I = 100dBμ		0.7	3.5	%
Signal to Noise Ratio	S/N	V_I = 74dBμ	45	55		dBμ
Signal Meter Output	V_M	V_I = 100dBμ	1.2	1.4	1.6	V
Input Impedance (Pin 16)	Z_I	Pin 16 0.8−0.9V_{DC}	1.45	2.12	2.8	KΩ

TEST CIRCUIT

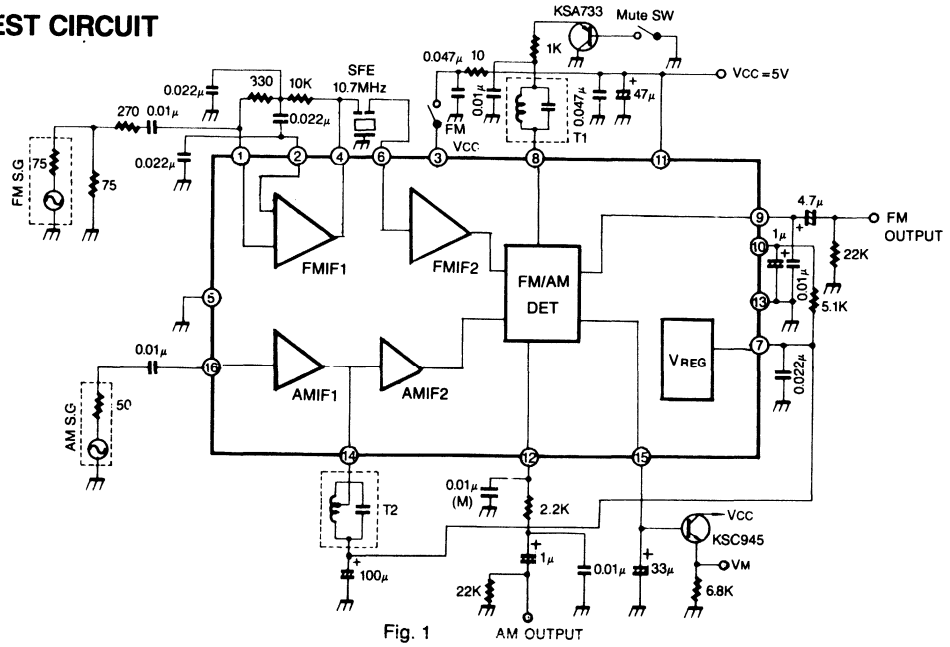
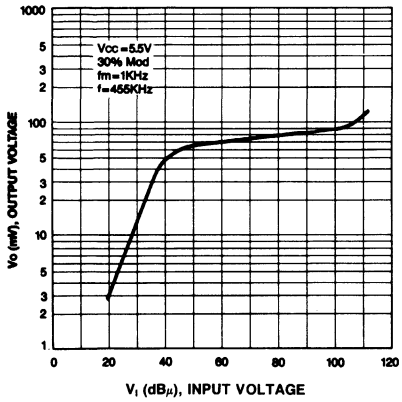


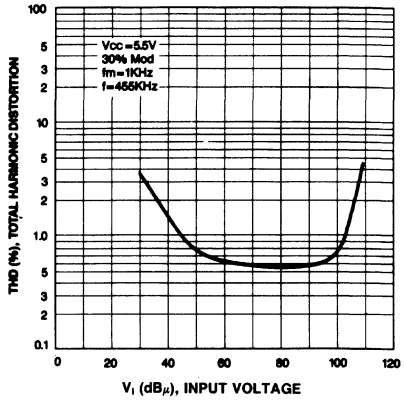
Fig. 1

(AM Section)

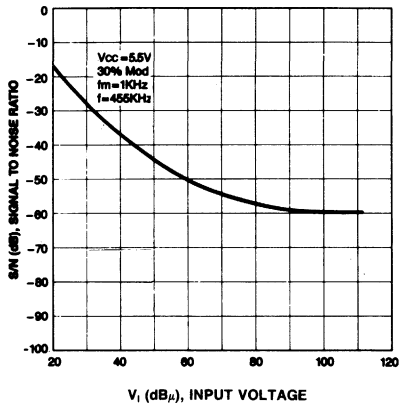
OUTPUT VOLTAGE-INPUT VOLTAGE



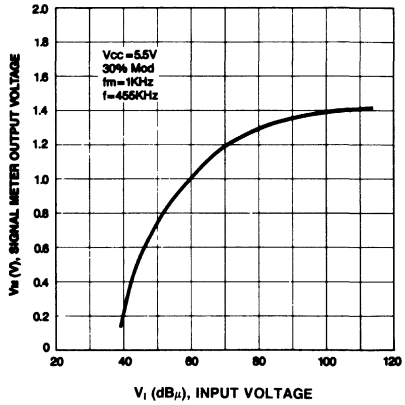
TOTAL HARMONIC DISTORTION-INPUT VOLTAGE



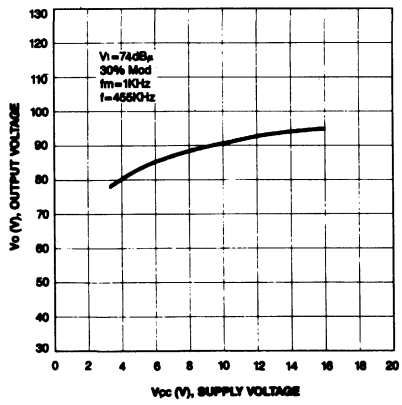
SIGNAL TO NOISE RATIO-INPUT VOLTAGE



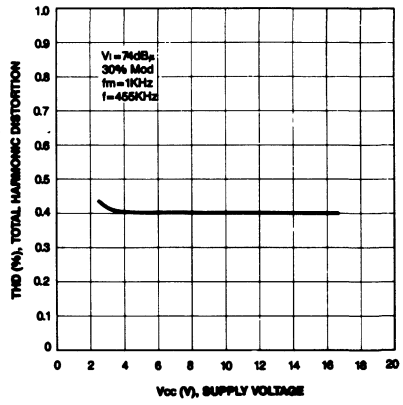
SIGNAL METER OUTPUT VOLTAGE-INPUT VOLTAGE



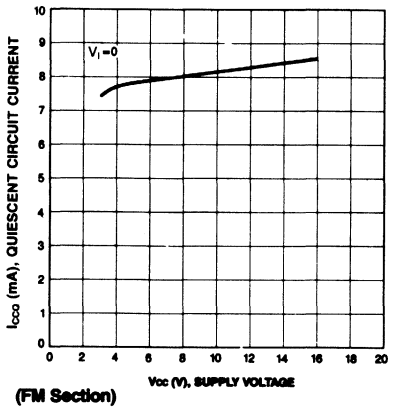
OUTPUT VOLTAGE-SUPPLY VOLTAGE



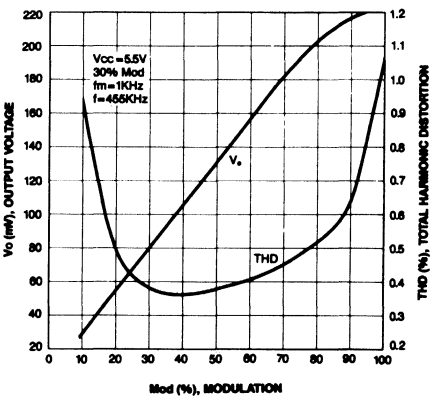
TOTAL HARMONIC DISTORTION-SUPPLY VOLTAGE



QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE

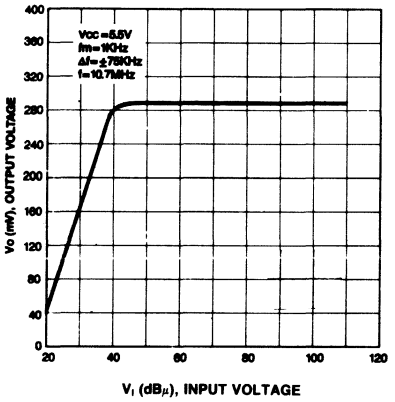


OUTPUT VOLTAGE — MODULATION
TOTAL HARMONIC DISTORTION

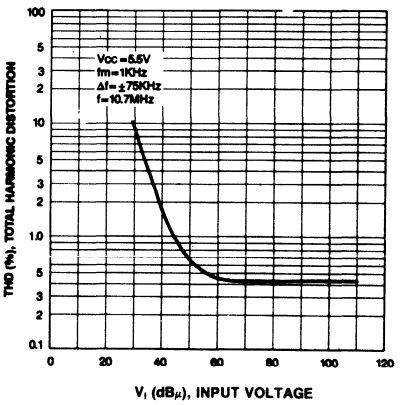


(FM Section)

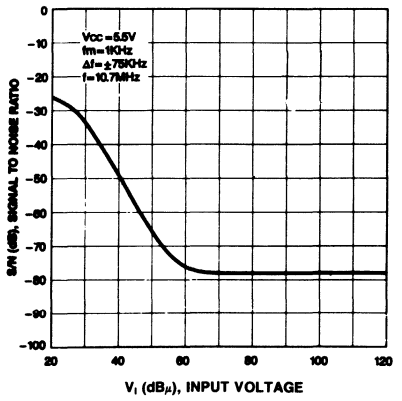
OUTPUT VOLTAGE-INPUT VOLTAGE



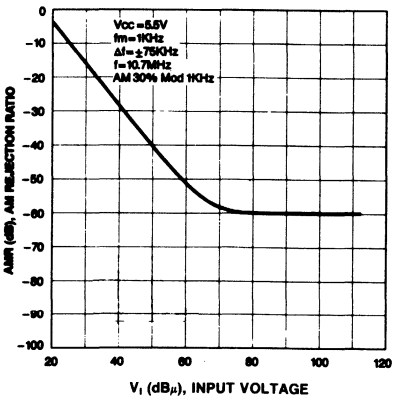
TOTAL HARMONIC DISTORTION-INPUT VOLTAGE



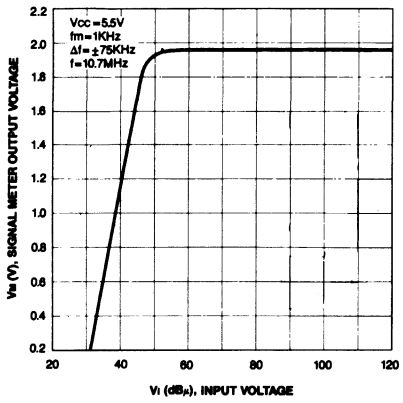
SIGNAL TO NOISE RATIO-INPUT VOLTAGE



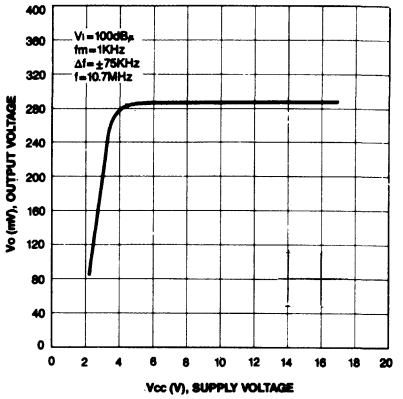
AM REJECTION RATIO-INPUT VOLTAGE



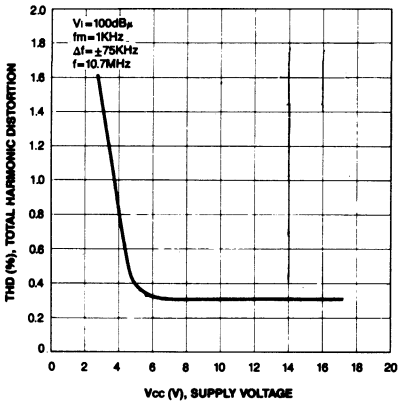
SIGNAL METER OUTPUT VOLTAGE-INPUT VOLTAGE



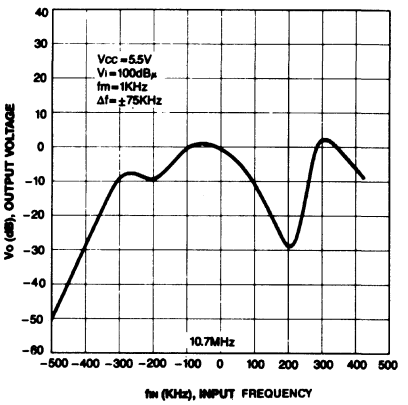
OUTPUT VOLTAGE-SUPPLY VOLTAGE



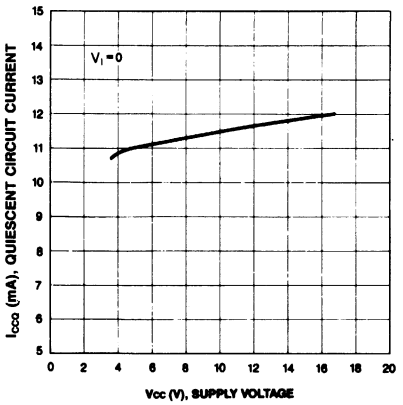
TOTAL HARMONIC DISTORTION-SUPPLY VOLTAGE



OUTPUT VOLTAGE-INPUT FREQUENCY



QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE



APPLICATION CIRCUIT

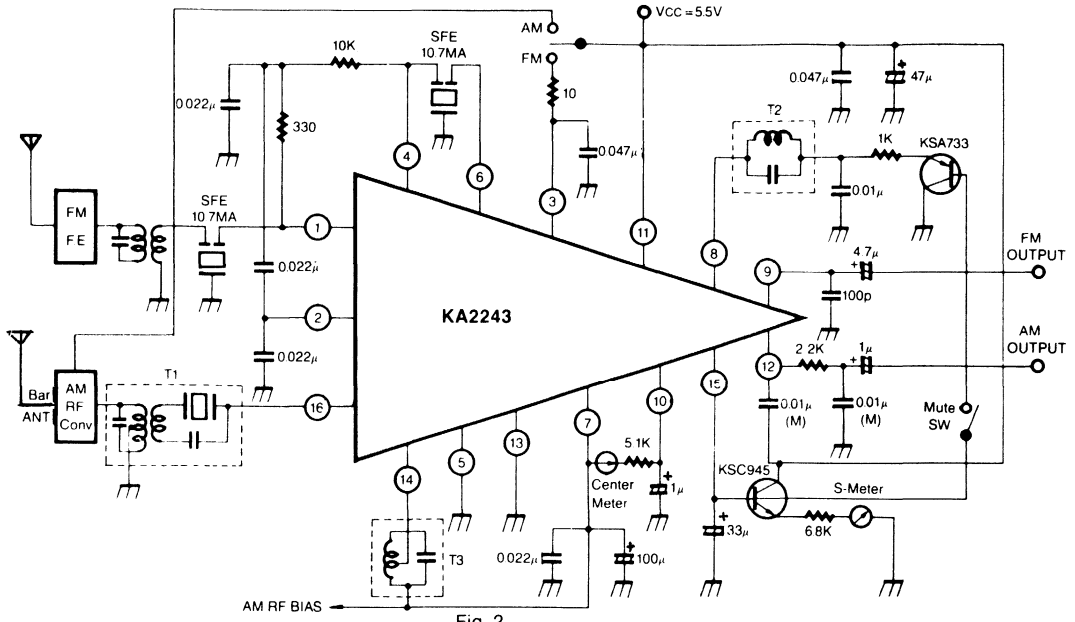
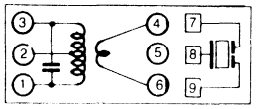


Fig. 2

COIL SPECIFICATION

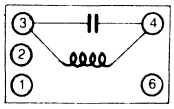
1. T1



C_O (pF)	f (KHz)	Q_O (%)	TURNS		
			4-6	3-2	2-1
180	455	105	6	93	55

Seoul Jupa
SJ-015-552
0.06mmϕ UEW

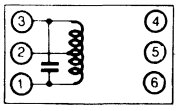
2. T2



C_O (pF)	f (MHz)	Q_O (%)	TURNS		
			3-4		
82	10.7	65	9		

Seoul Jupa
SJ-59JG-043
0.07mmϕ UEW

3. T3

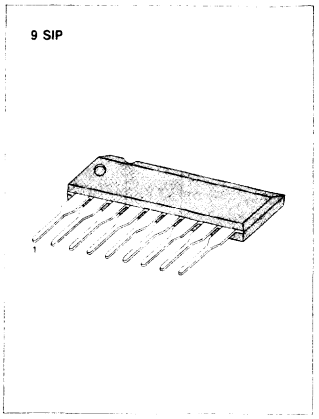


C_O (pF)	f (KHz)	Q_O (%)	TURNS		
			1-2	2-3	
180	455	120	51	92	

Seoul Jupa
SJ-015-521
0.07mmϕ UEW

FM IF SYSTEM FOR CAR RADIOS

The KA2244 is a monolithic integrated circuit consisting of FM IF amplifier, detector, muting circuit and signal meter driver. It is suitable for car radios.



FUNCTIONS

- 3-stage IF amplifiers.
- Peak detector.
- Muting circuit.
- Signal meter drive circuit.

FEATURES

- **Suitable for FM car radios.**
- **Wice operating supply voltage range: V_{CC} = 8V ~ 15V**
- **High detector output voltage (V_O = 500mV, Typ).**
- **Variable muting level.**
- **Muting off by Pin 4 open.**
- **Simplified single coil tuning.**
- **Low distortion (THD=0.1%; Typ).**
- **Minimum number of external parts required.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2244	9 SIP	-- 20°C ~ + 70°C

BLOCK DIAGRAM

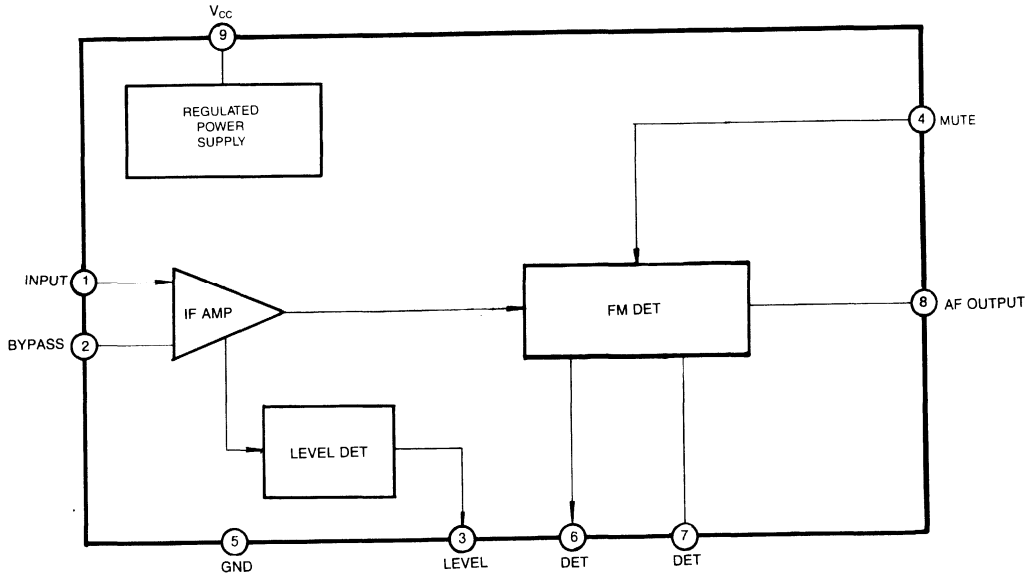


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Input Voltage	V_I	0.7	V
Power Dissipation	P_D	750	mW
Operating Temperature	T_{OPR}	−20 ~ +70	°C
Storage Temperature	T_{STG}	−40 ~ +125	°C

*: Derated above Ta = 25°C in the proportion of 4mW/°C

ELECTRICAL CHARACTERISTICS

(T_a = 25°C, V_{CC} = 12V, f = 10.7MHz, fm = 400Hz, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CCQ}	V_I = 0	10	14	18	mA
−3dB Limiting Sensitivity	$V_{I(LIM)}$	−3dB point from V_O (V_I = 80dBμ, Δf = ±75KHz)		50	55	dBμ
AM Rejection Ratio	AMR	FM: Δf = ±75KHz dev AM: 30% Mod, fm = 1KHz V_I = 80dBμ		50		dB
Detector Output Voltage	$V_{O(DET)}$	Δf = ±75KHz dev V_I = 80dBμ	300	500	700	mV
Total Harmonic Distortion	THD	Δf = ±22.5KHz dev V_I = 80dBμ		0.1		%
Signal to Noise Ratio	S/N	Δf = ±75KHz dev V_I = 80dBμ		75		dB
Muting Attenuation	ATT_{MUTE}	Δf = ±75KHz dev V_I = 80dBμ, V_4 = 0		70		dB
Meter Driver Voltage	V_M	V_I = 110dBμ		4.0		V

TEST CIRCUIT

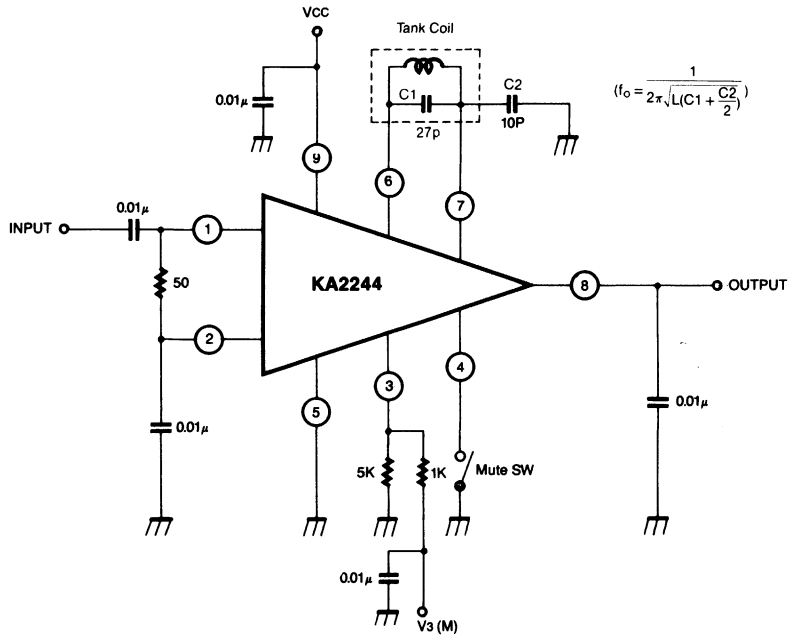
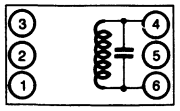


Fig. 2

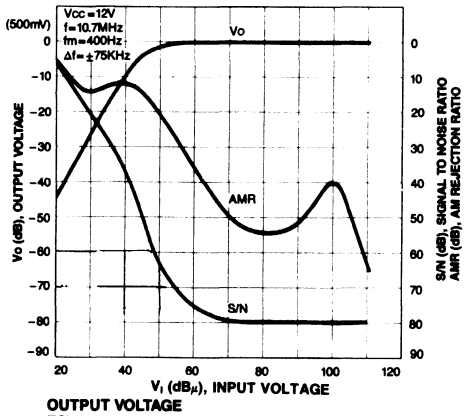
COIL SPECIFICATIONS



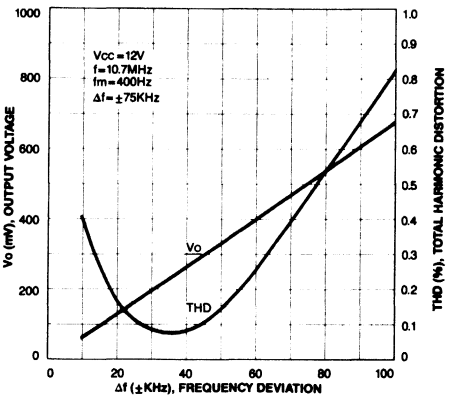
C_o (pF)	f (MHz)	Q_o (%)	TURNS		
			4-6		
27	10.7	150	18		

Seoul Jupa SJ-59JG-045 0.1mmϕ UEW

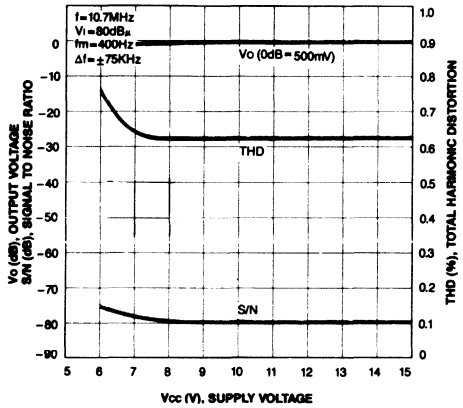
OUTPUT VOLTAGE
SIGNAL TO NOISE RATIO — INPUT VOLTAGE
AM REJECTION RATIO



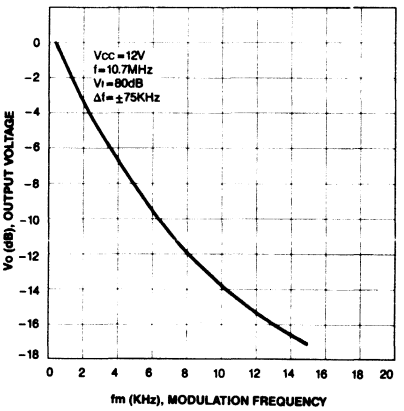
OUTPUT VOLTAGE ,
TOTAL HARMONIC DISTORTION —FREQUENCY DEVIATION



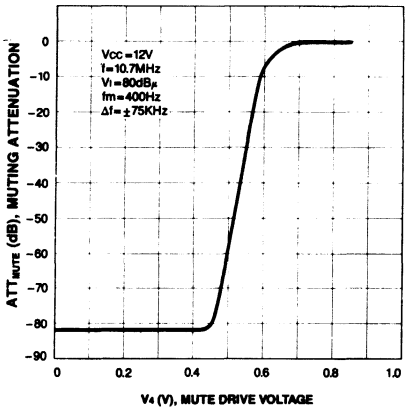
OUTPUT VOLTAGE
TOTAL HARMONIC DISTORTION —SUPPLY VOLTAGE
SIGNAL TO NOISE RATIO



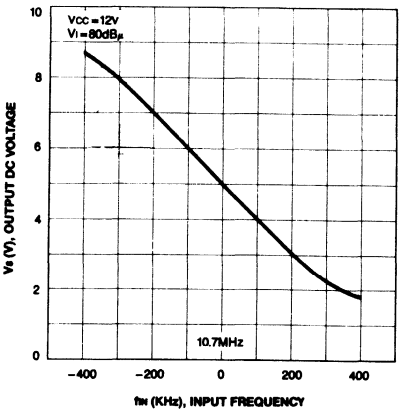
OUTPUT VOLTAGE-MODULATION FREQUENCY



MUTING ATTENUATION-MUTE DRIVE VOLTAGE



OUTPUT DC VOLTAGE-INPUT FREQUENCY

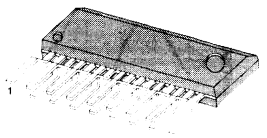


FM IF SYSTEM FOR CAR STEREO

The KA22441 is a monolithic integrated circuit consisting of FM IF system suitable for use in car stereo and music centers.

It features practically all of the functions for use a FM tuner, including AGC output, AFC output, level meter output in a single package.

16 ZSIP



FUNCTIONS

- FM IF amplifier.
- Quadrature detector.
- AFC output.
- AGC output.
- Level meter output.
- Muting for weak signal.
- Muting for detuned condition.

FEATURES

- **Soft muting function.**
- **Variable muting maximum attenuation.**
- **Variable muting attack input signal.**
- **Variable muting slope with respect to input signal level.**
- **Level meter output.**
- **AFC output.**
- **AGC output.**
- **High sensitivity ($V_{I(LIM)}$ = 25dBμ: Typ).**
- **High output level.**
- **Good S/N ratio (78dB: Typ).**
- **Low distortion (0.05%: Typ).**
- **Wide operating supply voltage range: V_{CC} = 6V ~ 14V**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA22441	16 ZSIP	−20°C ~ +70°C

BLOCK DIAGRAM

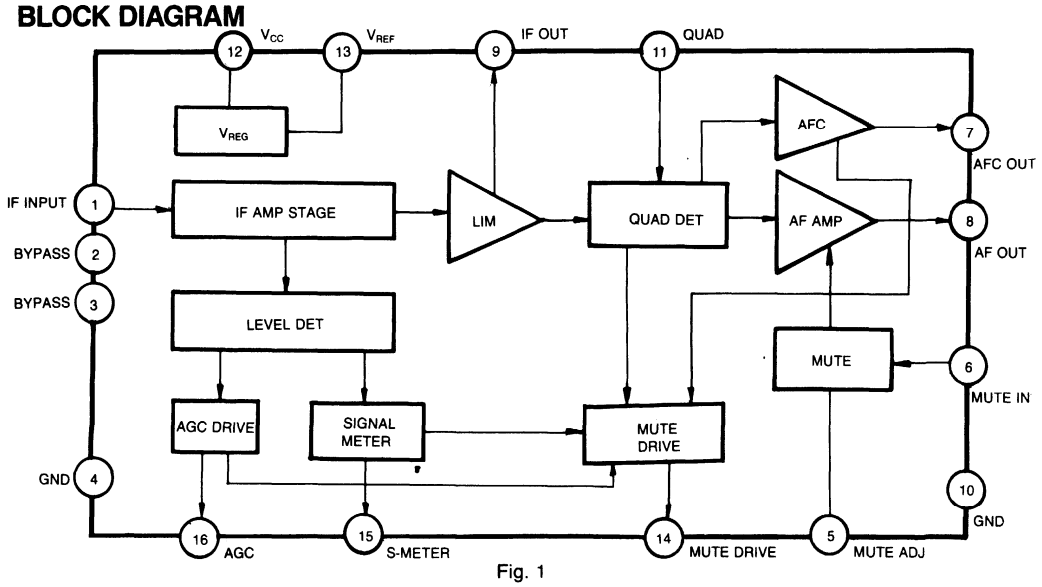


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Power Dissipation	P_D	640	mW
Operating Temperature	T_{OPR}	−20 ~ +70	°C
Storage Temperature	T_{STG}	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(T_a =25°C, V_{CC} =8V, Δf=±75KHz, V_i =100dBμ, fm=400Hz, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC}		6	8	14	V
−3dB Limiting Sensitivity	I_{CCQ}	V_I = 0	15	21	27	mA
Input Limiting Sensitivity	$V_{I\,(LIM)}$	V_O (V_O = 100dBμ) −3dB down		25	29	dBμ
Dectector Output Voltage	$V_{O\,(DET)}$		200	260	320	mV
Total Harmonic Distortion	THD			0.05	0.2	%
Signal to Noise Ratio	S/N		70	78		dB
AM Rejection Ratio	AMR	AM: fm=1KHz, 30% Mod	50	63		dB
Signal Meter Output Voltage	V_M	V_I = 0	0	0.1	0.3	V
		V_I = 100dBμ	4.5	5.3	6.0	
AGC Output Voltage	$V_{O\,(AGC)}$	V_I = 0	3.5	4.1	4.5	V
		V_I = 100dBμ	0	0.02	0.3	
Muting Sensitivity	S_{MUTE}	V_{14} = 2V	22	26	32	dBμ
Muting Attenuation	ATT_{MUTE}	V_6 = 2V	10	15	20	dB
		V_6 = 5V	24	28	32	
Muting Bandwidth	BW_{MUTE}	V_{14} = 2V	140	210	370	KHz

TEST CIRCUIT

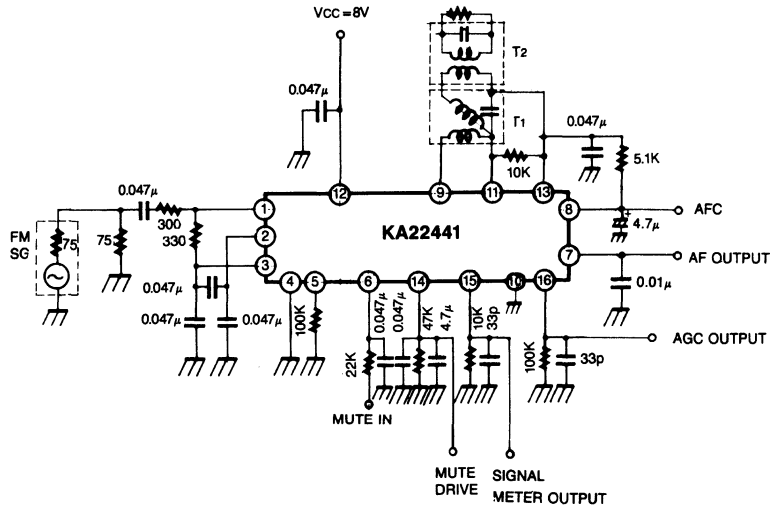


Fig. 2

APPLICATION INFORMATION

C_1, C_2, C_3: IF amplifier bypass capacitors
These capacitors bypass to the ground both the carrier signal and the high-frequency components of the amplifier output.

C_{10} : **Power supply bypass capacitor**

C_9 : **Internal regulated power supply bypass capacitor**

C_8 : **AFC output smoothing capacitor**
This capacitor bypasses to the ground the detector signal output at Pin 7.

C_7 : **De-emphasis capacitor**
The value of the C_8 determines the de-emphasis time constant.

C_6 : **Mute drive output smoothing capacitor**
This capacitor bypasses to the ground high-frequency noise components included in the muting output.

C_5 : **Signal meter output voltage smoothing capacitor**
This capacitor is used to reduce any IF carrier signal components or other high-frequency components remaining on the level meter output voltage.

C_4 : **AGC voltage smoothing capacitor**
If C_{11} is not connected, the AGC output will contain residual IF carrier frequency components.

R_1 : **IF amplifier resistor**
The IF amplifier input impedance is determined by the value of this resistance.

R_2 : **Muting maximum attenuation adjustment resistor**
The value of this resistor sets the maximum muting attenuation which is used when no signal is present or in the detuned condition. If the value of R_5 is made small, the maximum muting attenuation is decreased.

R_3 : **Mute drive current adjusting resistor**
This resistor is used to adjust the slope of the muting attenuation. If the value of this resistor is made small, the muting slope for the input signal level is increased.

R_4 : **Muting bandwidth adjustment resistor**
This resistor is capable of adjusting the muting bandwidth and AFC sensitivity. If the value of R_7 is made small, the muting bandwidth widens and the AFC sensitivity decreases.

R_5 : **Damping resistor**
If the value of R_{11} is made small, the Q of the tuned circuit decreases with an accompanying decrease in gain.

R_6 : **Damping resistor**

R_7 : **Mute drive load resistor**
If R_{14} is made large, the time required for muting to be removed will increase.

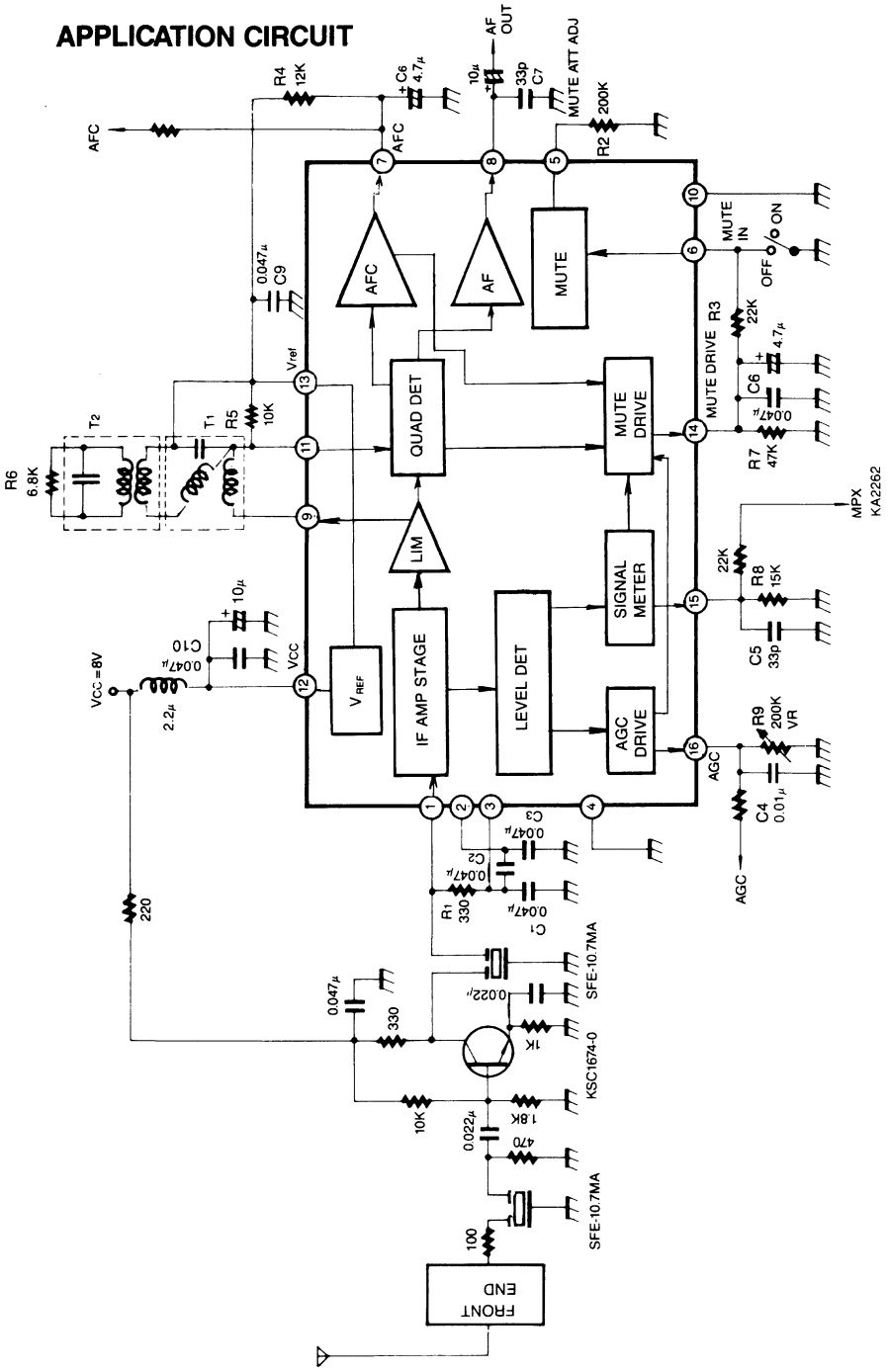
R_8 : **Signal meter output load resistor**
This resistor is used to adjust the slope of the muting attenuation. If the value of this resistor is made small, the slope of the muting attenuation is increased.

R_9 : **AGC output load resistor**
This resistor is used to set the weak-signal muting starting point. If the value of this resistor is made small, the starting point of input signal level for muting is raised.

L_1 : **Power supply chock coil**

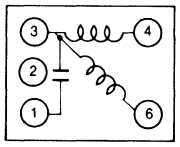
T_1, T_2 : **IF transformer**
The detector output voltage and total harmonic distortion are determined by the Q of this quadrature detector coil.

APPLICATION CIRCUIT



COIL SPECIFICATIONS

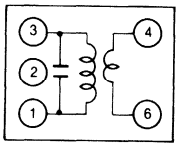
1. T1



C_o (pF)	f (MHz)	Q_o (%)	Turns	
			3 – 4	6 – 3
120	10.7	20 (Min)	89 1/2	17 1/2

KOREA TOKO 292MEA-K5018FKG-KR 0.07ø 2UEW

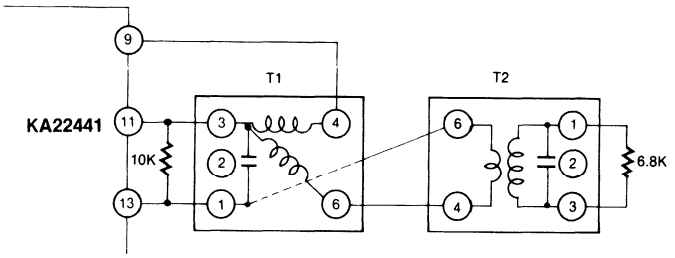
2. T2



C_o (pF)	f (MHz)	Q_o (%)	Turns	
			1 – 3	6 – 4
62	10.7	20 (Min)	24	1

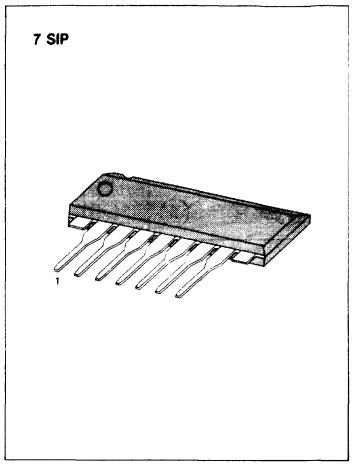
KOREA TOKO 292MEA-K5019AN-KR 0.07ø 2UEW

COIL COMBINATION



FM IF SYSTEM FOR CAR RADIOS

The KA2245 is a monolithic integrated circuit consisting of an FM IF amplifier and detector.
It is suitable for car radios.



FUNCTIONS

- 3-stage IF amplifier.
- Peak detector.

FEATURES

- **Suitable for FM car radios.**
- **Wide operating supply voltage range: V_{CC} = 8V ~ 14V.**
- **High detector output voltage (V_O = 500mV,Typ).**
- **Excellent AM rejection: AMR=50dB (Typ).**
- **High sensitivity: $V_{I\,(LIM)}$ = 50dBμV (Typ).**
- **Simplified single coil tuning.**
- **Low distortion (THD=0.1%: Typ).**
- **Minimum number of external parts required.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2245	7 SIP	-20°C ~ +70°C

BLOCK DIAGRAM

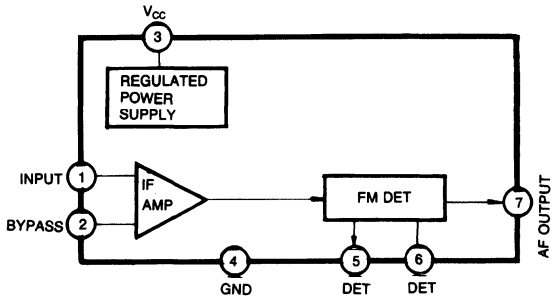


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	15	V
Input Voltage	V_I	0.7	V
Power Dissipation	P_D	400	mW
Operating Temperature	T_{OPR}	−20 ~ +70	°C
Storage Temperature	T_{STG}	−40 ~ +125	°C

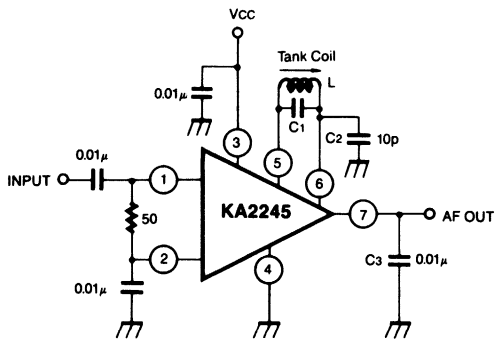
*: Derated above Ta=25°C in the proportion of 4mW/°C

ELECTRICAL CHARACTERISTICS

(T_a = 25°C, V_{CC} = 12V, f = 10.7MHz, fm = 400Hz)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CCQ}	V_I = 0	8	12	15	mA
−3dB Limiting Sensitivity	$V_{I\,(LIM)}$	−3dB point from V_O V_I = 80dBμ, Δf = ±75KHz		50	55	dBμ
AM Rejection Ratio	AMR	FM: Δf = ±75KHz dev AM: 30% Mod V_I = 80dBμ		50		dB
Detector Output Voltage	V_O	Δf = ±75KHz dev V_I = 80dBμV	300	500	700	mV
Total Harmonic Distortion	THD	Δf = ±22.5KHz dev V_I = 80dBμV		0.2		%
Signal to Noise Ratio	S/N	Δf = ±75KHz dev V_I = 80dBμV		60		dB

TEST CIRCUIT



APPLICATION CIRCUIT

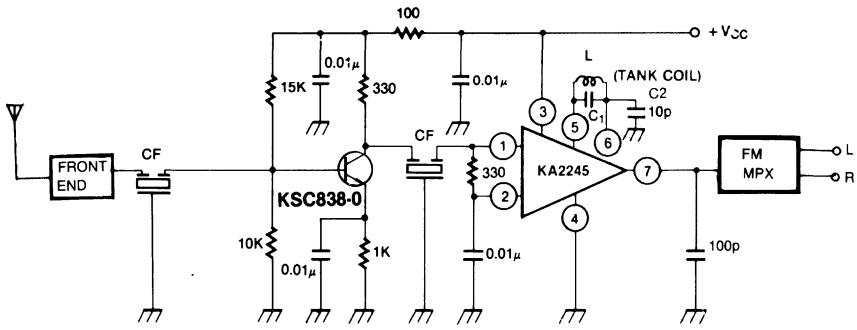
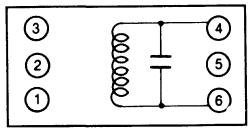


Fig. 3

$$\left(f_o = \frac{1}{2\pi\sqrt{L(C1 + \frac{C2}{2})}}\right)$$

COIL SPECIFICATIONS

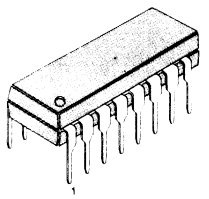


C_o (pF)	f (MHz)	O_o (%)	Turns		
			4 – 6		
27	10.7	150	18		

FM IF/AM TUNER SYSTEM

The KA2247 is a monolithic integrated circuit developed for the radio cassette tape recorder.

16 DIP



FUNCTIONS

- AM SECTION: RF amplifier, Mixer, OSC (with ALC), IF amplifier, Detector, AGC, Tuning indicator.
- FM SECTION: IF amplifier, Quadrature detector, AF preamplifier, Tuning indicator.

FEATURES

- **Minimum number of external parts required.**
- **Very good S/N: FM (81dB), AM (53dB).**
- **AM oscillator circuit with ALC: Oscillation output voltage of pin 16.**
  MW 130mV
  SW 70mV ~ 90mV
  (7MHz) ~ (24MHz)
- **Excellent AM whistle performance: Whistle 1% at V_i = 100dB/m.**
- **Built-in tuning indicator.**
- **Built-in AM/FM function switch.**
- **Operating supply voltage range: V_{CC} = 3V ~ 8V.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2247	16 DIP	- 20°C ~ + 70°C

BLOCK DIAGRAM

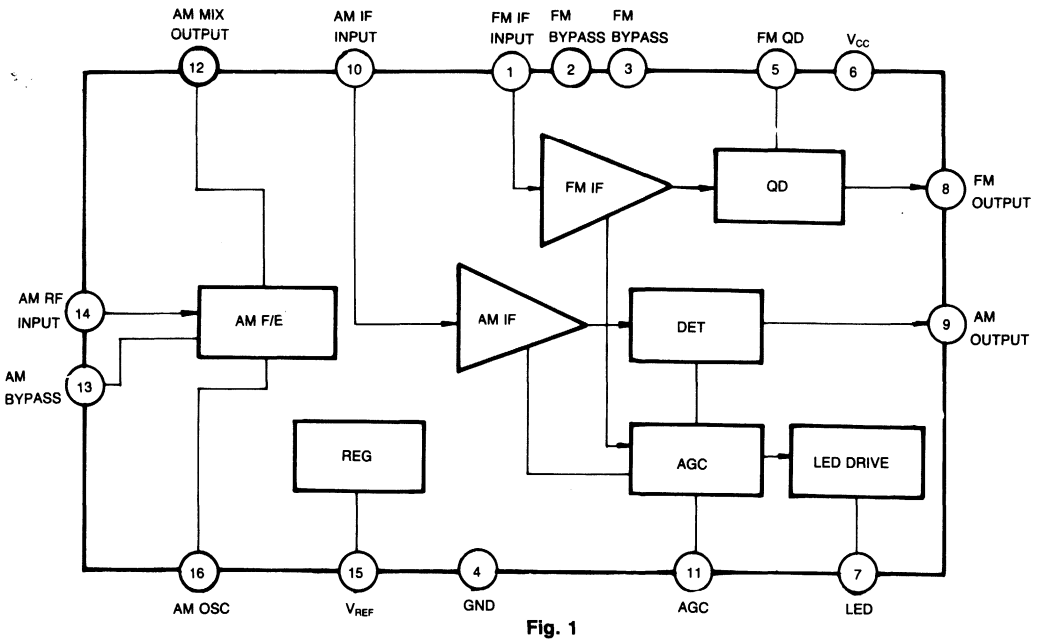


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	9	V
Circuit Current	I_{CC}	50	mA
Input Current (Pin 7)	I_7	20	mA
Output Current (Pin 15)	I_{15}	0.1	mA
Power Dissipation	P_D	450	mW
Operating Temperature	T_{OPR}	−20 ~ +70	°C
Storage Temperature	T_{STG}	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(T_a =25°C, V_{CC} =4.5V)

FM Section (f=10.7MHz, Δf=±75KHz, fm=400Hz)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CCQ}	V_I = 0		8.5	12.0	mA
−3dB Limiting Sensitivity	$V_{I\,(LIM)}$	V_O (V_I = 80dBμ) −3dB down		35	42	dBμ
Detector Output Voltage	$V_{O\,(DET)}$	V_I = 80dBμ	183	260	367	mV
Total Harmonic Distortion	THD 1	V_I = 80dBμ		0.55	1.2	%
	THD 2	V_I = 80dBμ, Δf = ±22.5KHz		0.05		
AM Rejection Ratio	AMR	V_I = 80dBμ, AM: fm = 1KHz, 30% Mod		60		dB
Signal to Noise Ratio	S/N 1	V_I = 80dBμ	77	81		dB
	S/N 2	V_I = 80dBμ, Δf = ±22.5KHz		71		
Tuning Indication Voltage	V_L	I_{LAMP} = 1mA		39	49	dBμ

AM Section (f=1MHz, fm=400Hz, 30% Mod)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CCQ}	V_I = 0		7.5	10.5	mA
Detector Output Voltage	$V_{O\,(DET)\,1}$	V_I = 23dBμ	17.3	31	55	mV
Detector Output Voltage	$V_{O\,(DET)\,2}$	V_I = 60dBμ	87	122	174	mV
Total Harmonic Distortion	THD 1	V_I = 60dBμ		0.45	1.3	%
	THD 2	V_I = 100dBμ		1.5	3.0	
Signal to Noise Ratio	S/N 1	V_I = 23dBμ	18.0	21.5		dB
	S/N 2	V_I = 60dBμ	48	53		
Tuning Indication Voltage	V_L	I_{LAMP} = 1mA	22	30	38	dBμ
Oscillator Voltage	V_{OSC}	f=24MHz	60	86	120	mV

TEST CIRCUIT

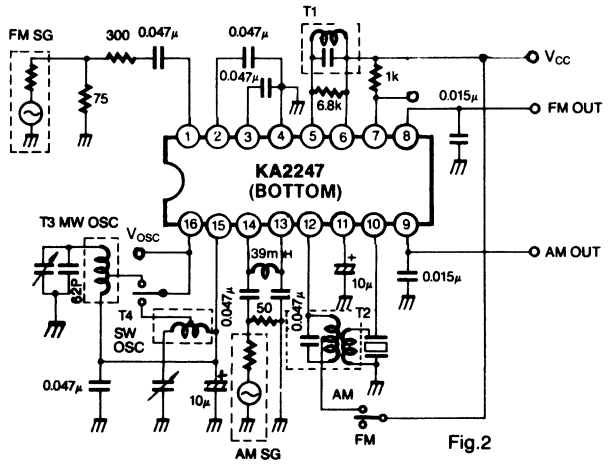
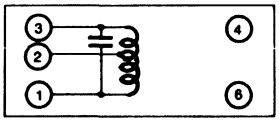


Fig.2

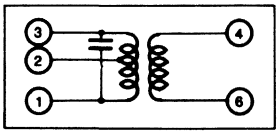
COIL SPECIFICATIONS

T1 FM IF (DET)



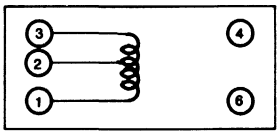
C_o (PF)	f (MHz)	Q_o	TURNS	
1-3		1-3	1-3	Seoul Jupa 0.12mmϕ UEW
56	10.7	95	12	

T2 AM IFT (MIX OUT)



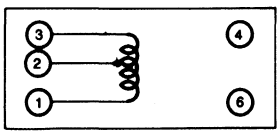
C_o (PF)	f (KHz)	Q_o	TURNS			
1-3		1-3	1-2	2-3	4-6	Seoul Jupa 0.07mmϕ UEW
180	455	110	90	62	8	

T3 (MW OSC)



f (KHz)	L (μH)	Q_o	TURNS		
	1-3	1-3	1-2	2-3	Seoul Jupa 0.07mmϕ UEW
796	140	140	32	32	

T4 (SW OSC)

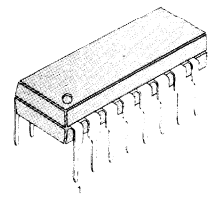


L (μH)	Q_o	TURNS		
1-3	1-3	1-2	2-3	Seoul Jupa 0.1mmϕ UEW
12	80	12	12	

FM IF/AM TUNER SYSTEM

The KA22471 is a monolithic integrated circuit developed for the radio cassette tape recorder.

16 DIP



FUNCTIONS

- AM SECTION: Converter, IF amplifier, Detector, Tuning indicator.
- FM SECTION: IF amplifier, Quadrature detector, Tuning indicator.

FEATURES

- **Low quiescent circuit current.**
  AM: 7mA (Typ) FM: 10mA (Typ)
- **A minimum number of external parts required.**
- **Built-in AM/FM function switch.**
- **Tuning indicator: direct LED driving capability: I_{LAMP} = 10mA (MAX)**
- **One terminal AM/FM detector output.**
- **Advanced performance at high input signal.**
- **Operating supply voltage range: V_{CC} = 3V ~ 8V.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA22471	16 DIP	−20°C ~ +70°C

BLOCK DIAGRAM

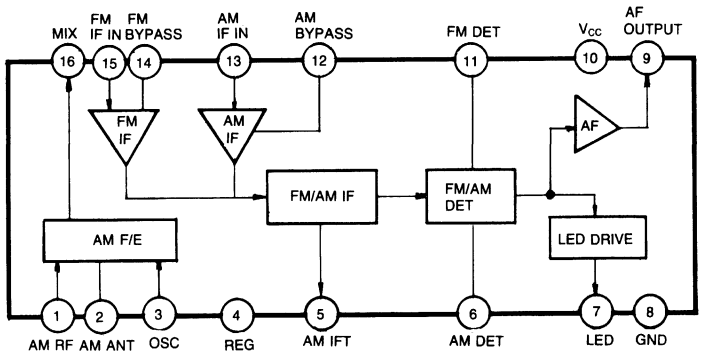


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	8	V
Power Dissipation	P_D	600	mW
Operating Temperature	T_{OPR}	−20 ~ +70	°C
Storage Temperature	T_{STG}	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(T_a =25°C, V_{CC} =5V, unless otherwise specified)

FM Section (f=10.7MHz, fm=400Hz, Δf= ±22.5KHz)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CCQ}	V_I = 0		10	15	mA
−3dB Limiting Sensitivity	$V_{I\,(LIM)}$	V_O (V_I =80dBμ) −3dB down		40	46	dBμ
Detector Output Voltage	$V_{O\,(DET)}$	V_I = 66dBμ, R_{DUMP} = 4.7KΩ	57	85	114	mV
Total Harmonic Distortion	THD	V_I = 80dBμ		0.05		%
AM Rejection Ratio	AMR	V_I = 80dBμ, AM: fm = 1KHz, 30% Mod		38		dB
Signal to Noise Ratio	S/N	V_I = 80dBμ		65		dB
Signal Meter Output	V_M	V_I = 100dBμ	1.55	1.7	1.85	V
Tuning Indication Voltage	V_L	I_{LAMP} = 1mA		46	52	dBμ

AM Section (f=1MHz, 30% Mod, fm=400Hz)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CCQ}	V_I = 0		7	10	mA
Voltage Gain	G_V	V_I = 26dBμ	20	30	60	mV
Detector Output Voltage	$V_{O\,(DET)}$	V_I = 60dBμ	65	95	125	mV
Total Harmonic Distortion	THD	V_I = 60dBμ		1.0		%
Signal to Noise Ratio	S/N	V_I = 60dBμ		47		dB
Signal Meter Output	V_M	V_I = 100dBμ	1.55	1.7	1.85	V
Tuning Indication Voltage	V_L	I_{LAMP} = 1mA		32		dBμ
Oscillator Stop Voltage	V_{STOP}	R_{DUMP} = ∞		1.5		V

TEST CIRCUIT

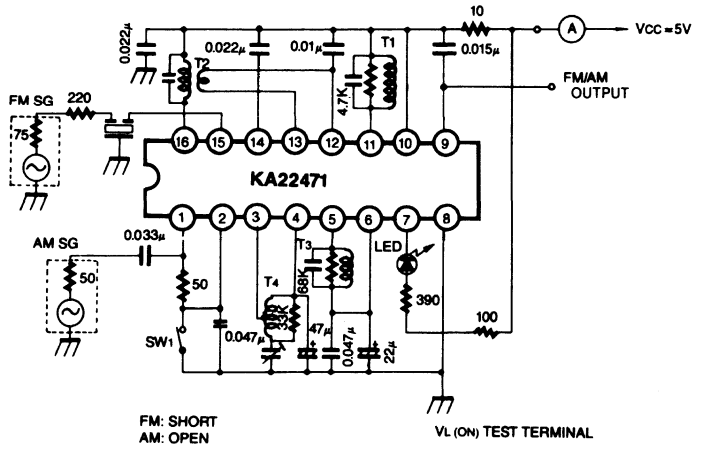
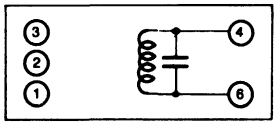


Fig. 2

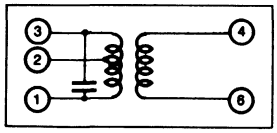
COIL SPECIFICATIONS

T1 FM IF (DET)



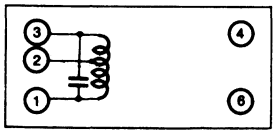
C_o (pF)	f (MHz)	Q_o	TURNS	
4-6		4-6	4-6	Seoul Jupa 0.12mmϕ UEW
47	10.7	150	14	

T2 AM IFT (MIX OUT)



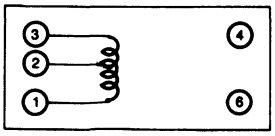
C_o (PF)	f (KHz)	Q_o	TURNS			
1-3		1-3	1-2	2-3	4-6	Seoul Jupa 0.07mmϕ UEW
180	455	110	90	62	8	

T3 AM IFT (DET)



C_o (pF)	f (KHz)	Q_o	TURNS	
1-3		1-3	1-3	Seoul Jupa 0.07mmϕ UEW
180	455	110	152	

T4 (MW OSC)



f (KHz)	L (μH)	Q_o	TURNS		
	1-3	1-3	1-2	2-3	Seoul Jupa 0.06mmϕ UEW
796	288	120	13	75	

APPLICATION CIRCUIT

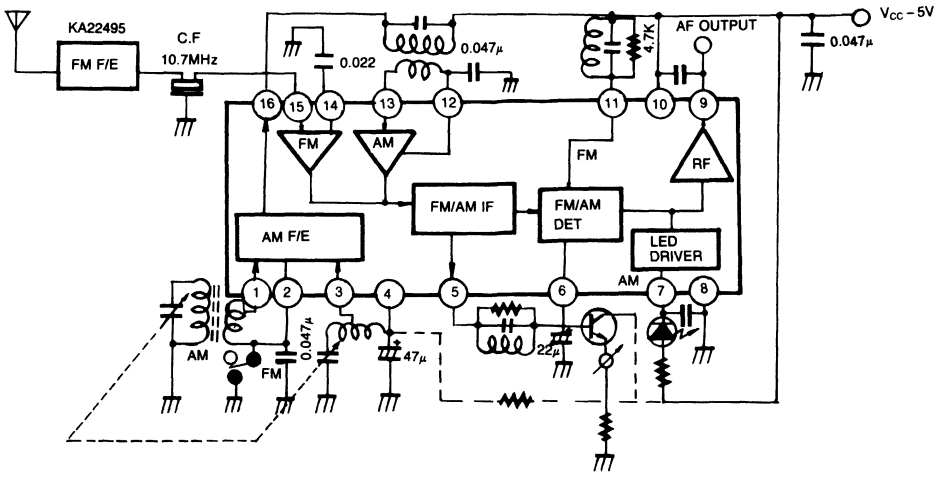
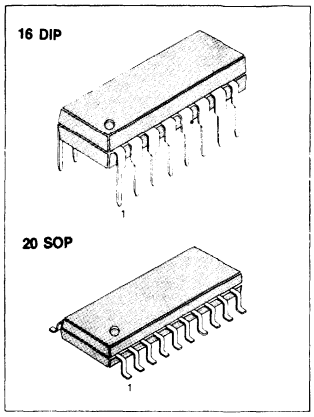


Fig. 3

3V FM IF/AM TUNER SYSTEM

The KA2248 is a monolithic integrated circuit developed the for headphone stereo.



FUNCTIONS

- AM SECTION: Converter, IF amplifier, Detector, Tuning indicator
- FM SECTION: IF amplifier, Quadrature detector, Tuning indicator

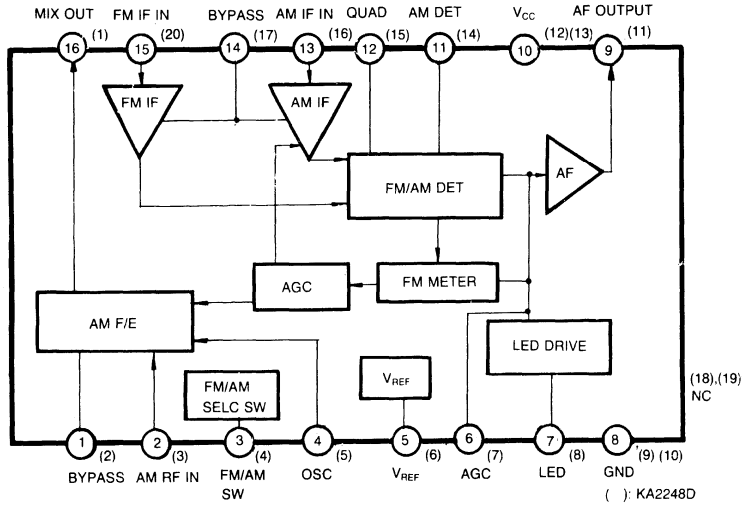
FEATURES

- **Low quiescent current: AM: I_{CCQ} = 3mA (Typ), V_{CC} = 3V**
  FM: I_{CCQ} = 8mA (Typ), V_{CC} = 3V
- **Wide operating voltage range: V_{CC} = 1.8V ~ 6V.**
- **Built-in AM/FM function switch.**
- **Tuning indicator: direct LED driving capability: 10mA (Max).**
- **One terminal AM/FM detector output.**
- A minimum number of external parts required.

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2248A	16 DIP	-20°C ~ 70°C
KA2248D	20 SOP	

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic		Symbol	Value	Unit
Supply Voltage		V_{CC}	6	V
Power Dissipation	KA2248A	P_D	600	mW
	KA2248D		350	
Operating Temperature		T_{OPR}	− 20 ~ + 70	°C
Storage Temperature		T_{STG}	− 40 ~ + 125	°C

ELECTRICAL CHARACTERISTICS

(T_a = 25°C, V_{CC} = 3V, unless otherwise specified)

* **FM Section** (f = 10.7MHz, fm = 1KHz, Δf = 22.5KHz)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CCQ}	V_I = 0		8	13	mA
− 3dB Limiting Sensitivity	$V_{I\,(LIM)}$	V_I = 86dBμ		46	52	dBμ
Detector Voltage	$V_{O\,(DET)}$	V_I = 86dBμ	60	85	120	mV
Signal to Noise Ratio	S/N	V_I = 86dBμ	50	65		dB
Total Harmonic Distortion	THD	V_I = 86dBμ		0.1	1.0	%
AM Rejection Ratio	AMR	V_I = 86dBμ	30	45		dB
Tuning Indication Voltage	V_L	I_{LAMP} = 1mA		50	58	dBμ
Output Resistance	R_O	f = 1KHz		0.7		KΩ

* **AM Section** (f = 1MHz, fm = 1KHz, 30% Mod)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Current	I_{CCQ}	V_I = 0		3	7	mA
Voltage Gain	G_V	V_I = 26dBμ	15	30	50	mV
Detector Voltage	$V_{O\,(DET)}$	V_I = 60dBμ	35	50	70	mV
Signal to Noise Ratio	S/N	V_I = 60dBμ	35	45		dB
Total Harmonic Distortion	THD	V_I = 60dBμ		1.0	3.5	%
Oscillator Stop Voltage	V_{STOP}			1.2		V
Output Resistance	R_O	f = 1KHz		8.3		KΩ
Tuning Indication Voltage	V_L	I_{LAMP} = 1mA		26	40	dBμ

TEST CIRCUIT

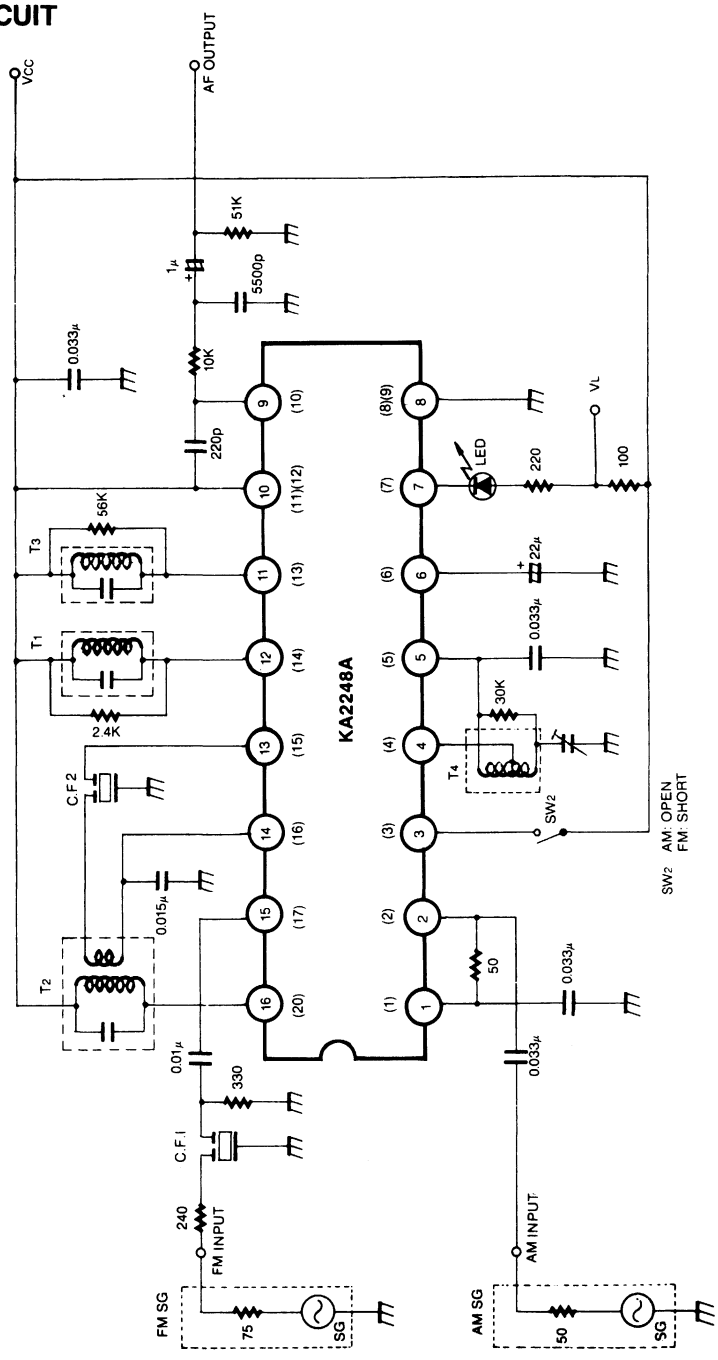
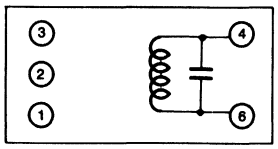


Fig. 2

COIL SPECIFICATIONS (BOTTOM VIEW)

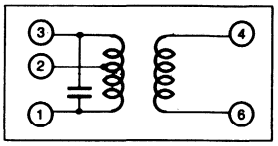
T1 FM IF (DET)



C_o (pF)	f (MHz)	Q_o	TURNS
4-6		4-6	4-6
100	10.7	150	14

Seoul Jupa
0.12mmϕ UEW

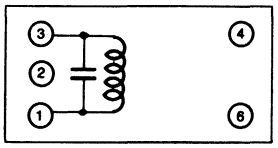
T2 AM IFT (MIX OUT)



C_o (PF)	f (KHz)	Q_o	TURNS		
1-3		1-3	1-2	2-3	4-6
180	455	110	90	62	8

Seoul Jupa
0.07mmϕ UEW

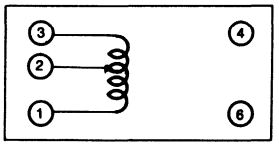
T3 AM IFT (DET)



C_o (pF)	f (KHz)	Q_o	TURNS
1-3		1-3	1-3
180	455	110	152

Seoul Jupa
0.07mmϕ UEW

T4 (MW OSC)



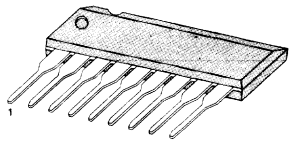
f (KHz)	L (μH)	Q_o	TURNS	
	1-3	1-3	1-2	2-3
796	288	120	13	75

Seoul Jupa
0.08mmϕ UEW

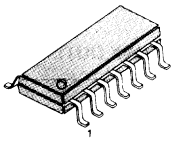
FM FRONT END

The KA22495 is a monolithic integrated circuit designed for the ƧONT FM front end of portable radio cassettes or music centers.
It consists of RF AMP, local OSC, OSC buffer and mixer. ƧetC.
Compared with conventional types, it is improved in the follow- ıarac- ing characteristics:
1) Low supply voltage.
2) Strong input.
3) Spurious radiation.

9 SIP



14 SOP



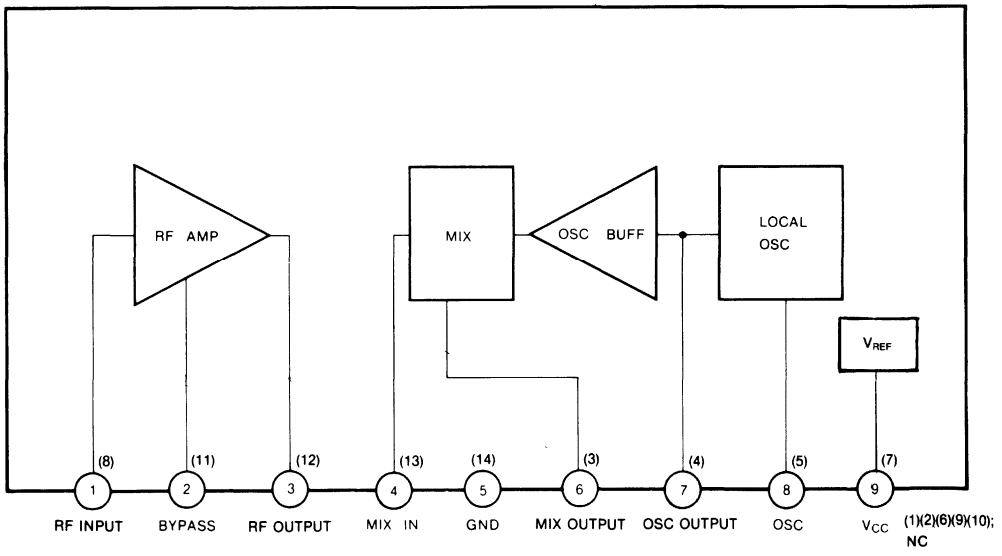
FEATURES

- **Wide supply voltage range: V_{CC} = 1.6V ~ 6.0V**
- **Low local oscillation stop voltage: V_{STOP} = 0.9V (Typ)**
- **Improved inter-modulation characteristics by double balanced type mixer circuit.**
- **Low spurious radiation.**
- **Built-in clamping diode in the mixer output stage.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA22495	9 SIP	−25°C ~ +75°C
KA22495D	14 SOP	

BLOCK DIAGRAM



( ): KA22495D

Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol		Value	Unit
Supply Voltage	V_{CC}		8	V
Power Dissipation	P_D	KA22495	600	mW
		KA22495D	300	
Operating Temperature	T_{OPR}		−25 ~ +75	°C
Storage Temperature	T_{STG}		−55 ~ +150	°C

*: Derated above Ta = 25°C in the proportion of 4mW/°C.

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 5V, f = 98MHz, fm = 1KHz, △f = ±22.5KHz, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CCQ}	V_I = 0		5.0	8.0	mA
−3dB Limiting Sensitivity	$V_{I(LIM)}$	V_D (V_I = 60dBμ) − 3dB Down		3.0	7.0	dBμ
Conversion Gain	G_V	V_I = 60dBμ	25	31		dB
Usable Sensitivity	S_{USA}	S/N = 30dB		11		dBμ
Oscillation Voltage	V_{OSC}	f_{OSC} = 108MHz	90	165	250	mV
Oscillation Stop Voltage	V_{STOP}			0.9	1.3	V

TEST CIRCUIT 1

(I_{CCO}, $V_{I\,(LIM)}$, S_{USA}, G_V, V_{OSC}, V_{STOP})

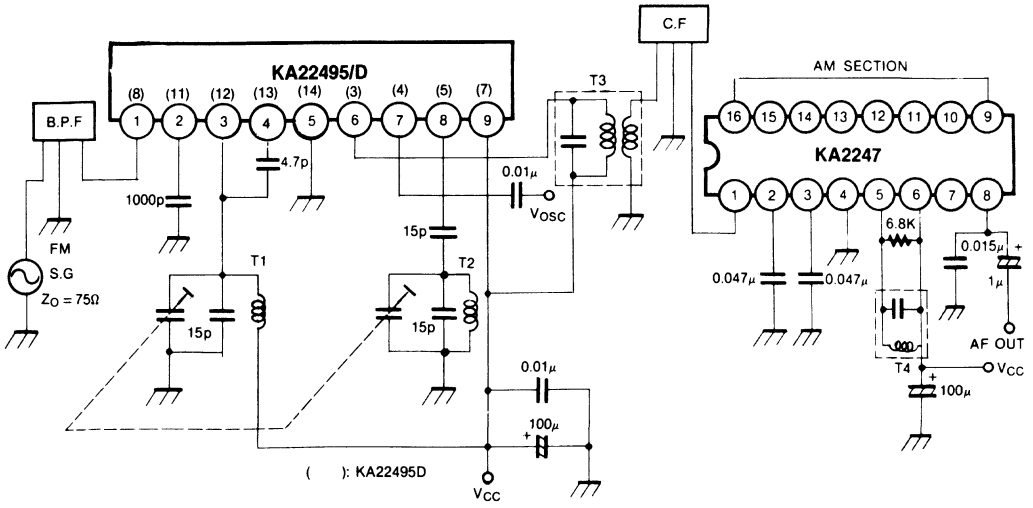


Fig. 2

When using the KA22471 for the IF stage.

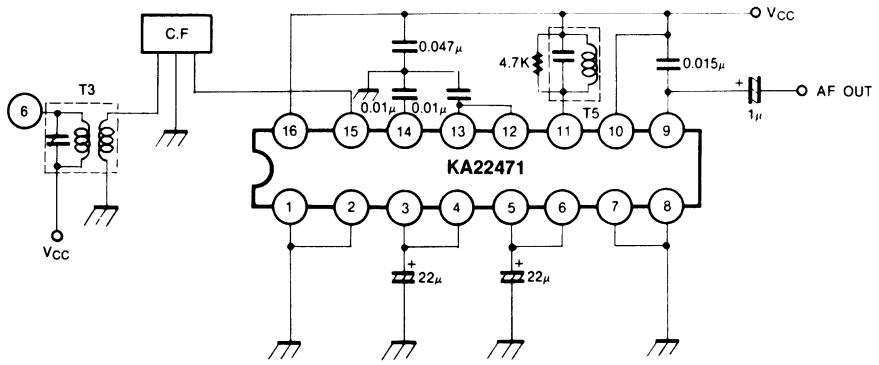
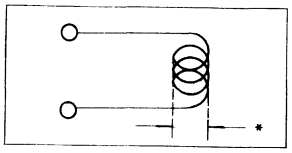


Fig. 3

COIL SPECIFICATIONS (BOTTOM VIEW)

T1 FM RF

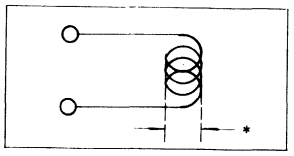


f (MHz)	Q_o	Turns
98	100	4

* In a Diameter of 5.5mm

0.8mm ø UEW

T2 FM OSC

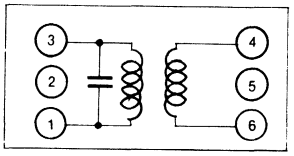


f (MHz)	Q_o	Turns
98	100	3

* In a Diameter of 5.5mm

0.8mm ø UEW

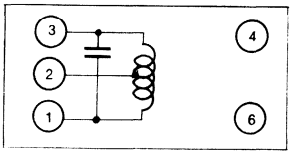
T3 FM IFT



C_o (pF)	f	Q_o	Turns	
1 – 3	(MHz)	1 – 3	1 – 3	4 – 6
75	10.7	115	12	1

KOREA TOKO
0.12mm ø UEW

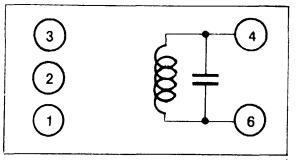
T4 FM IFT (DET)



C_o (pF)	f	Q_o	Turns
1 – 3	(MHz)	1 – 3	1 – 3
56	10.7	95	12

KOREA TOKO
0.12mm ø UEW

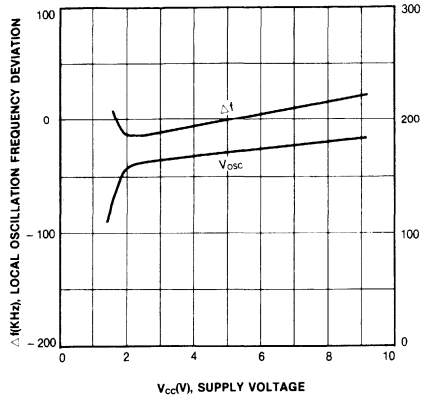
T5 FM IFT (DET)



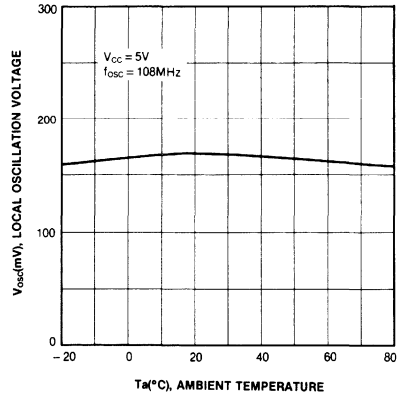
C_o (pF)	f	Q_o	Turns
4 – 6	(MHz)	4 – 6	4 – 6
47	10.7	115	14

KOREA TOKO
0.12mm ø UEW

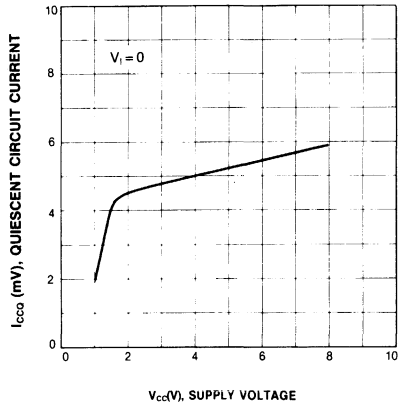
LOCAL OSCILLATION FREQUENCY DEVIATION, LOCAL OSCILLATION VOLTAGE-SUPPLY VOLTAGE



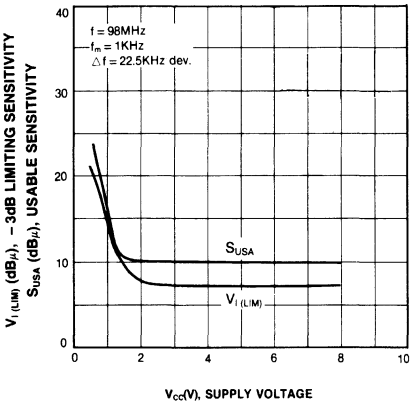
LOCAL OSCILLATION VOLTAGE ·AMBIENT TEMPERATURE



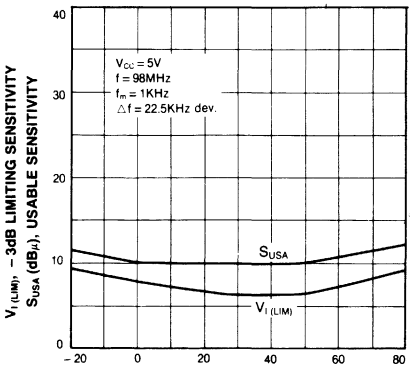
QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE



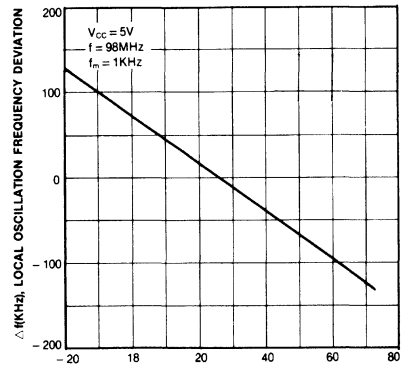
SENSITIVITY-SUPPLY VOLTAGE



SENSITIVITY-AMBIENT TEMPERATURE



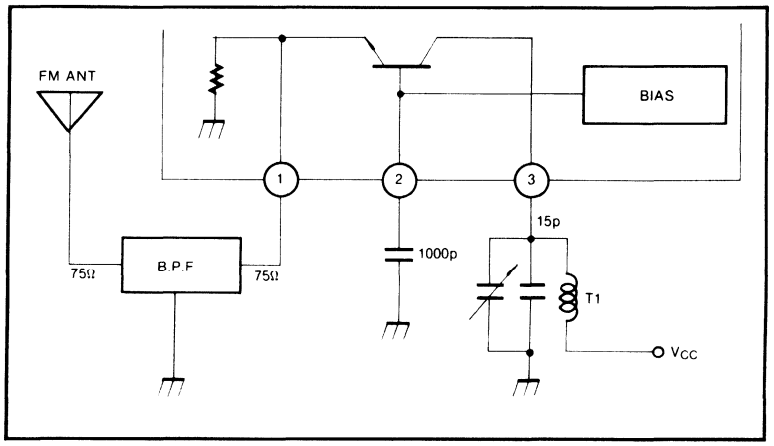
LOCAL OSCILLATION FREQUENCY DEVIATION ·AMBIENT TEMPERATURE



APPLICATION INFORMATION

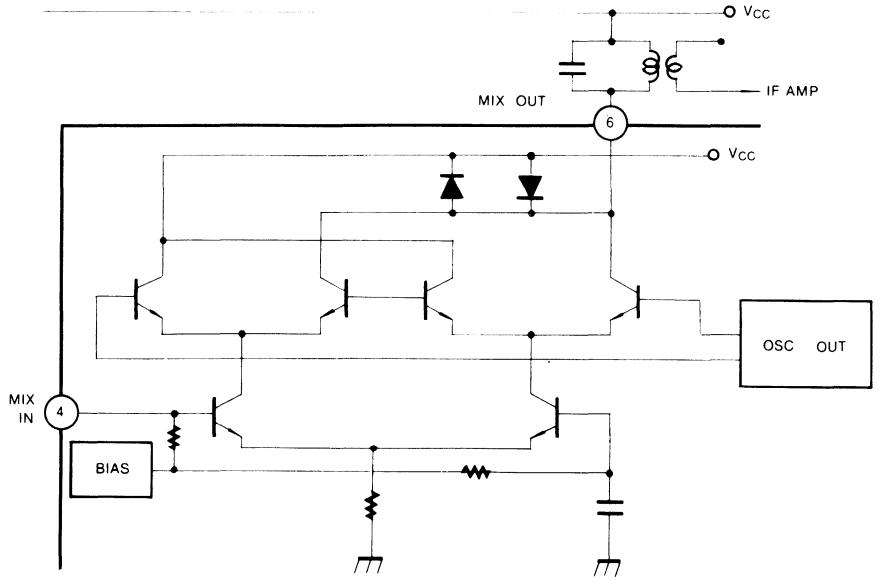
1. RF AMP

The RF AMP is a common base type, so the operating frequency range is improved. The GND of the bypass capacitor (Pin2) should be located closely at Pin 5 (GND). When using the bypass capacitor at V_{CC}-line of Pin 3, we can expect an improvement of the S/N ratio.



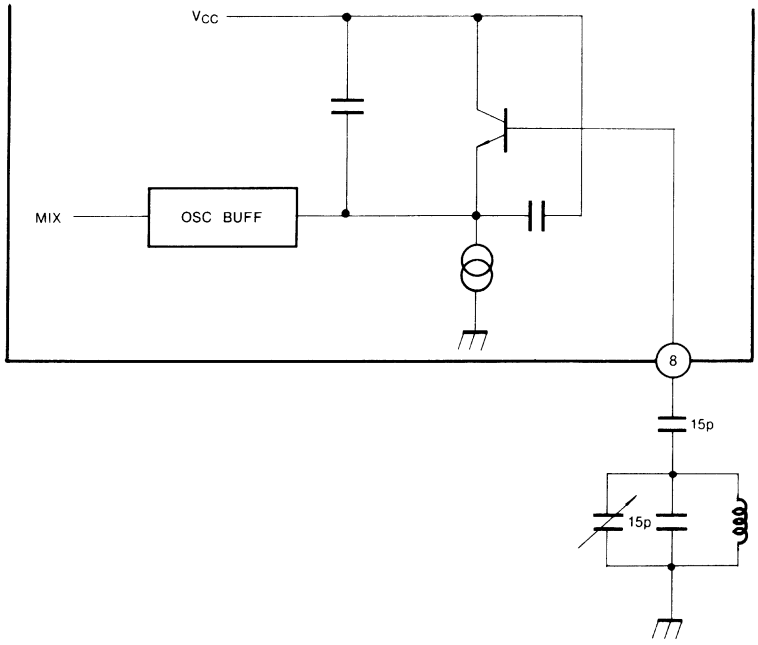
2. MIXER

The mixer stage uses a double balanced type in order to protect the leakage of OSC, spurious radiation. Also, this is built into the limiter in order to improve the strong input characteristic.



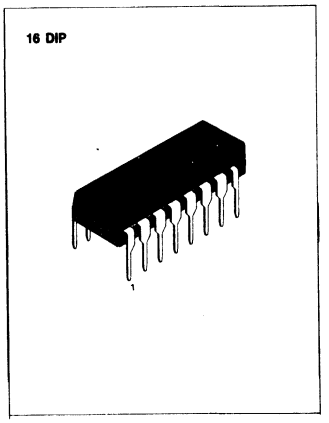
LOCAL OSCILLATION

The local oscillator uses a colpitts oscillator for stable oscillation at high frequency. This is built into the OSC buffer in order to stably operate the OSC frequency and OSC voltage at strong input.



DUAL ELECTRONIC VOLUME CONTROL

The KA2250 is a CMOS designed for electronization of dual volumes.
It is suitable for M/C, car stereos.



FEATURES

- **Wide supply voltage range: V_{DD} = 6V ~ 12V (Backup is possible up to 4V)**
- **Attenuation can be controlled from 0dB to −66dB by 2dB/step.**
- **Controlling attenuation by means of the built in osc and the up/down terminals.**
- **Single power supply operation as well as split power supply operation.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2250	16DIP	−20°C ~ +70°C

BLOCK DIAGRAM

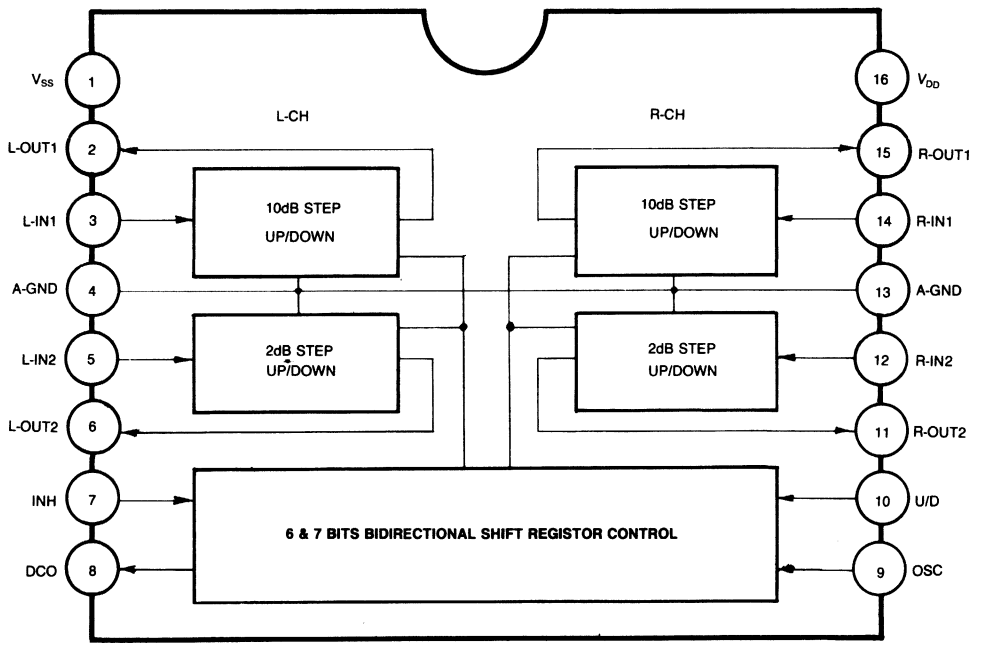


Fig. 1

PIN CONFIGURATION

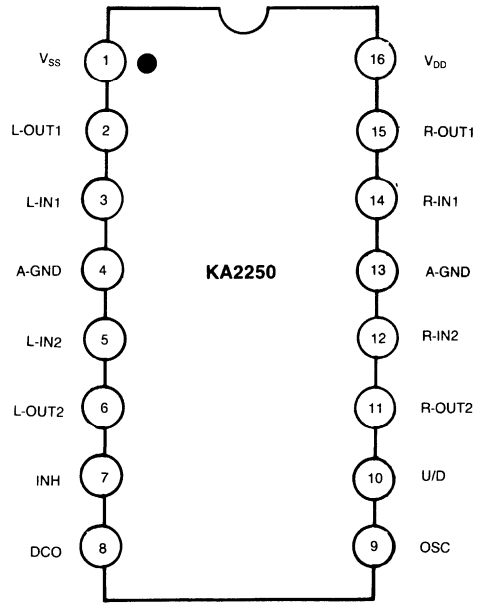


Fig. 2

PIN DESCRIPTION

Pin No.	Symbol	Description
1	V_{SS}	(−) power supply (GND)
2 15	L-OUT1 R-OUT1	10dB/step attenuator output. A signal applied to IN is attenuated in 7 steps from 0dB to 60dB at 10dB
3 14	L-IN1 R-IN1	10dB/step attenuator inputs.
4 13	A-GND	ANALOG GROUND
5 12	L-IN2 R-IN2	2dB/step attenuator inputs
6 11	L-OUT2 R-OUT2	2dB/step attenuator output. A signal applied to IN is attenuated in 5 steps from 0dB to 60dB at 2dB
16	V_{DD}	(+) power supply (V_{DD})
7	INH	When at "H" level, the operates normally.
8	DCO	DC current output for displaying attenuation.
9	OSC	R,C connecting pin for the oscillator.
10	U/D	Attenuation up/down control input.

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{DD}	13	V
Power Dissipation	P_D	150	mW
Operating Temperature	T_{OPR}	−20 ~ +75	°C
Storage Temperature	T_{STG}	−55 ~ +125	°C
Input Voltage	V_I	V_{DD} + 0.3 ~ V_{SS} − 0.3	V

ELECTRICAL CHARACTERISTICS

(V_{DD} = 12V, f = 1KHz, Ta = 25°C, unless otherwise noted)

Characteristics	Symbol	Test Condition	Min	Typ	Max	Unit
Circuit Current	I_{DD1}	V_{DD} = 13V	0.1	1.0	2.5	mA
	I_{DD2}	V_{DD} = 6V	0.1	0.8	2.0	
Attenuator Resistor	R_{ATT1}	pin3-pin4 pin14-pin13	25	50	70	KΩ
	R_{ATT2}	pin5-pin4 pin12-pin13	10	20	30	
Backup Current	I_{BACKUP}	V_{DD} = 4V, s/w1 = b			10	uA
Input High Voltage	V_{IH}	up (down) s/w on	9.6	11.8	12.3	V
Input Low Voltage	V_{IL}	s/w1 = a		0.5	1.2	
Total Harmonic Distortion	THD	V_I = 1.0Vpp, A_{TT} = 10dB, f = 15KHz		0.005	0.01	%
Attenuator error	$V_{ATT\ (ERR)}$	Vo = 5step	−2	0	2	dB
Max input Amplitude	$V_{I\ (MAX)}$	THD = 1%, V_{OL} = max	1.0	2.5	4.0	Vrms
DCO output current	$I_{O\ (DCO)}$	1 step	70	100	140	uA
Cross talk	CT	A_{TT} = −10dB	55	65		dB
Operating frequency	f_{OSC1}	up/sw on, s/w 3 = a	5	13	20	Hz
	f_{OSC2}	s/w 3 = d	9	11	13	KHz

APPLICATION INFORMATION

1. SETTING OF ATTENUATION

Attenuation is automatically set at the −40dB position when power is applied.

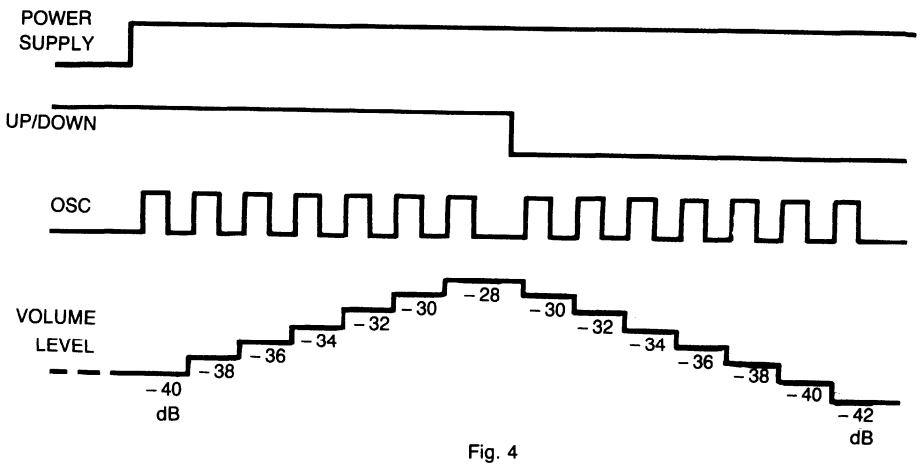


Fig. 4

As soon as the UP key is pressed after power on, the U/D pin is placed in the up state at "H" level, and the oscillator is actuated. When the DOWN key is pressed, the U/D pin is kept at "L" level as long as the DOWN key is pressed, and the oscillator is actuated in the down state and therefore, attenuation is decreased. Oscillation frequency is decided by Cx & Rx.

$$f_{osc} = \frac{1}{0.7Cx * Rx} \text{ (Hz) } (Rs \geqq 3Rx)$$

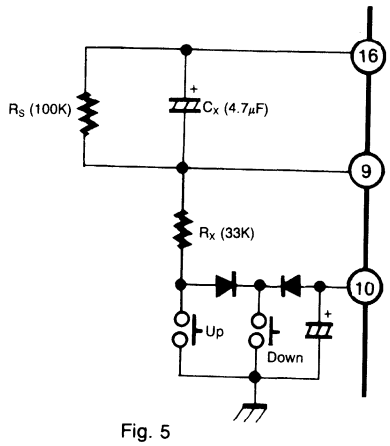


Fig. 5

TEST CIRCUIT

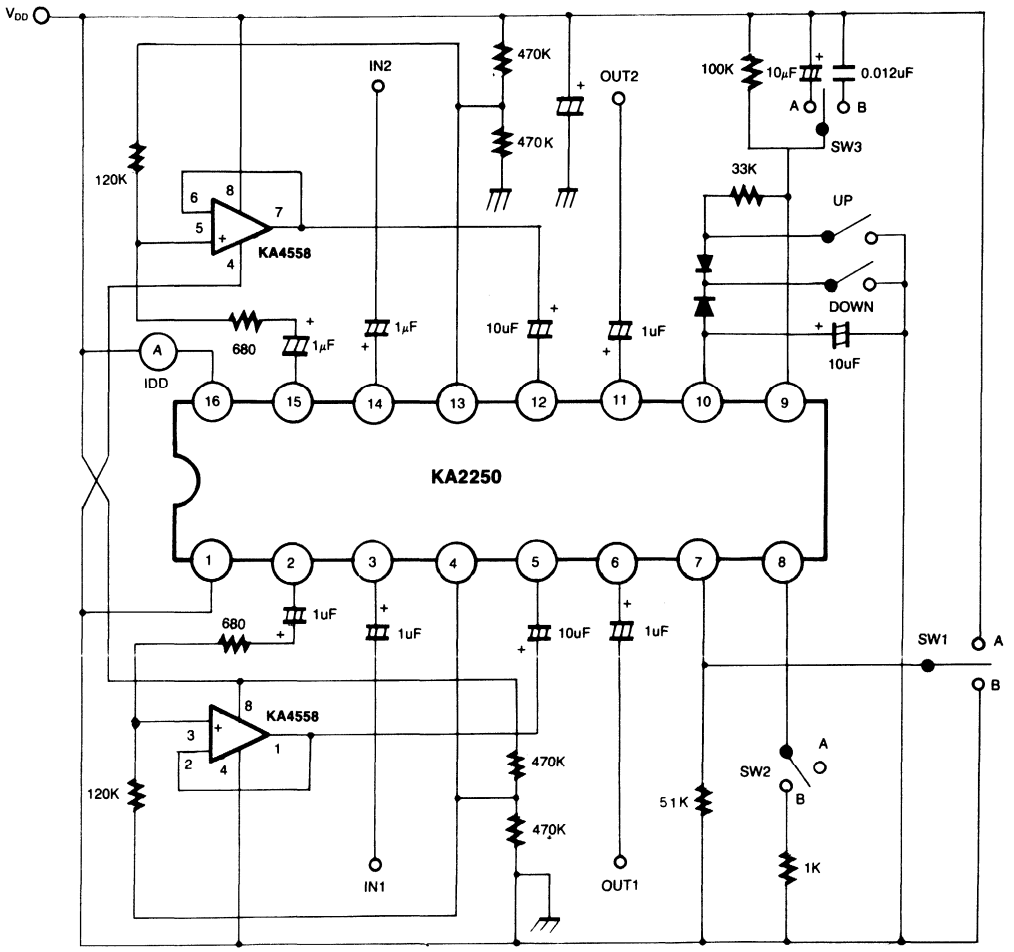


Fig. 3

2. Attenuation Display Output

The KA2250 is provided with the DC current output pin for displaying attenuation.
There are is steps attenuation with 0dB ~ - ∞
The current of each step is increased or decreased approximately 100uA.

STEP	DCO	ATTENUATION
0	0	- 64dB ~ - ∞
1	I = 100uA + 30uA	- 60dB ~ - 62dB
2	2*I	- 54dB ~ - 58dB
3	3*I	- 50dB ~ - 52dB
4	4*I	- 44dB ~ - 48dB
5	5*I	- 40dB ~ - 42dB
6	6*I	- 34dB ~ - 38dB
7	7*I	- 30dB ~ - 32dB
8	8*I	- 24dB ~ - 28dB
9	9*I	- 20dB ~ - 22dB
10	10*I	- 14dB ~ - 18dB
11	11*I	- 10dB ~ - 12dB
12	12*I	- 4dB ~ - 8dB
13	13*I	0dB ~ - 2dB

*Current value may fluctuate depending upon IC.
When high precision is required use a variable resistor as a load resistor.

3. BACKUP

On the KA2250, when power is off (S1 spen) or the INH pin is set as "L" (– V_{SS}) level, all I/O pin are shut off and current consumption is reduced to the minimum.
The backup by means of a capacitor (C1) becomes possible in this condition. Fig 6. shows an example of application when a backup capacitor is used.

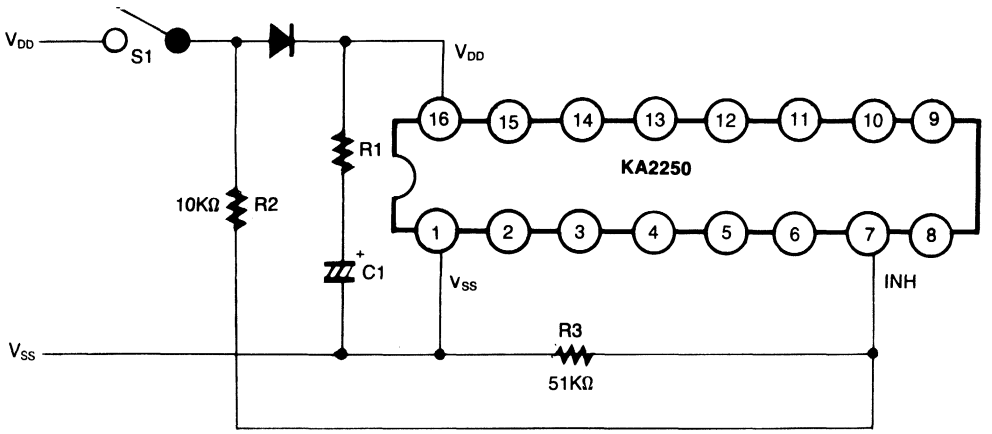


Fig. 6

*If V_{DD}-V_{SS} become below 4.0V, the backup is impossible.

4. INITIALIZATION WHEN POWER ON

The KA2250 built-in auto-initializing function for initialization when power on. As the initializing system through detection of supply voltage level is adopted, if rise of power supply is too fast, the initialization may not be fully effected. (no external initialization is necessary.) In additions for effective initialization it is necessary that the INH pin is raised simultaneously with supply voltage. Further, the initializing level is – 40dB. It is recommended to rise supply voltage and the INH pin as illustrated Fig. 7.

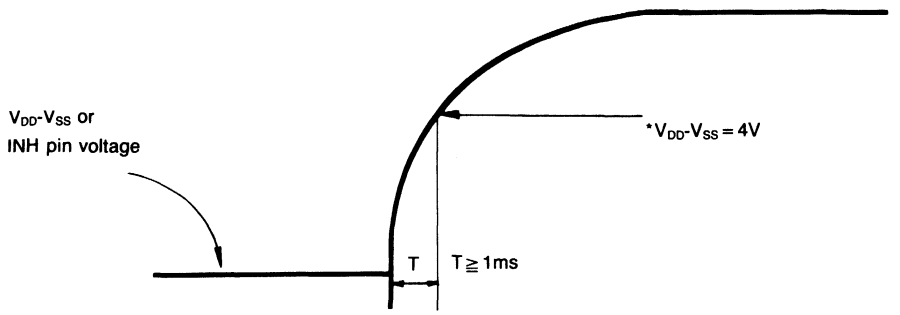


Fig. 7

If the voltage between V_{DD} and V_{SS} is below 4.0V, the auto-initializing function is actuated.

5. POWER SUPPLY

Single power supply operation as well as split power supply operation.

1) SPLIT POWER SUPPLY

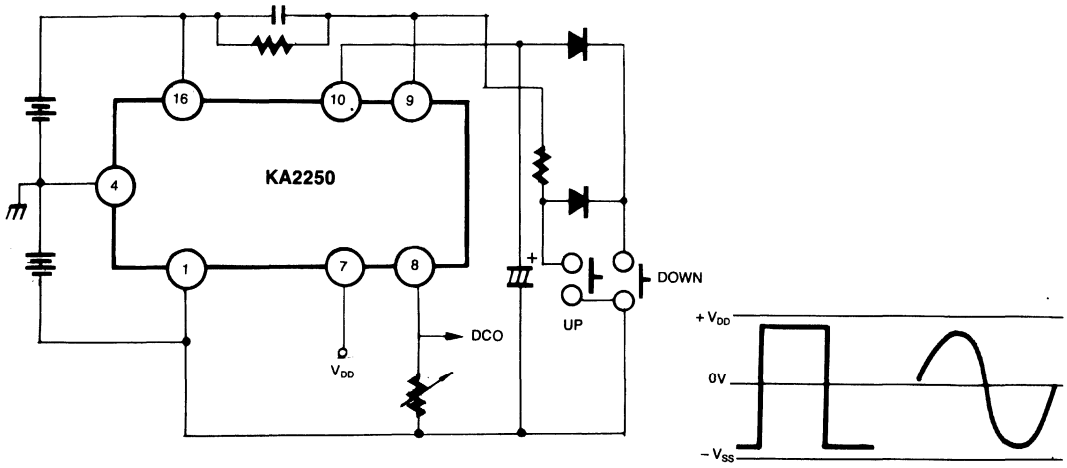


Fig. 8

2) SINGLE POWER SUPPLY

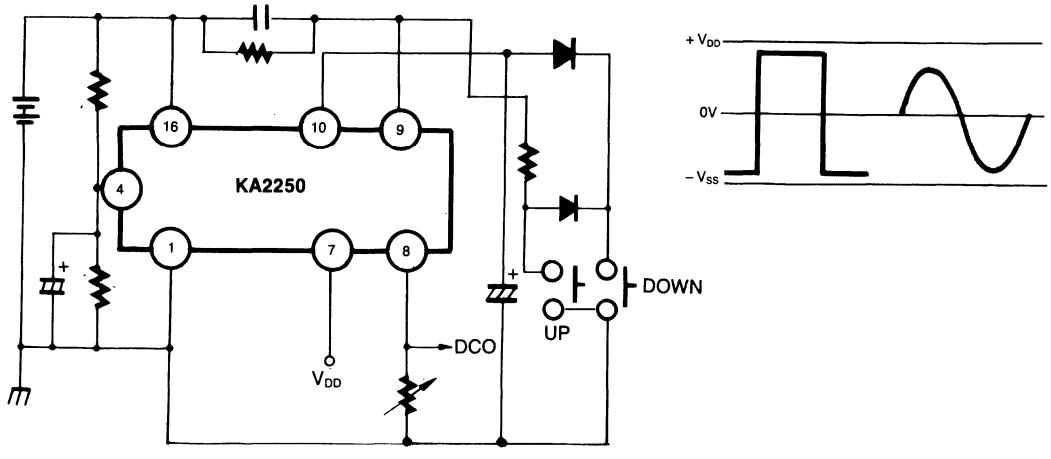
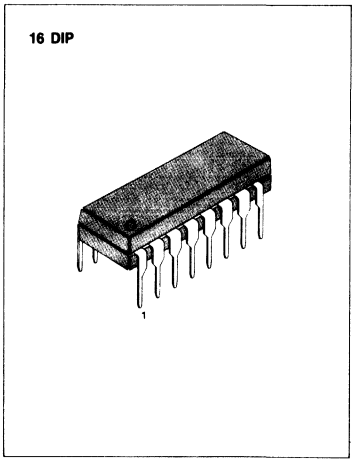


Fig. 9

FM STEREO MULTIPLEX DECODER

The KA2261 is a monolithic integrated circuit consisting of a phase locked loop FM stereo demodulator. It was designed for use in car stereos, cassette recorders and other equipment.



FEATURES

- **A PLL is used for high multiplexing performance.**
- **Wide operating supply voltage range: V_{CC} = 3V ~ 14V**
- **Low quiescent circuit current (I_{CCQ} = 8.5mA, Typ).**
- **High SCA rejection ratio.**
- **High channel separation (45dB, Typ) and can be controlled by an external resistor.**
- **Built-in VCO disable and monaural muting circuits.**
- **Built-in stereo indicator lamp drive circuit.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2261	16 DIP	−20°C ~ +70°C

BLOCK DIAGRAM

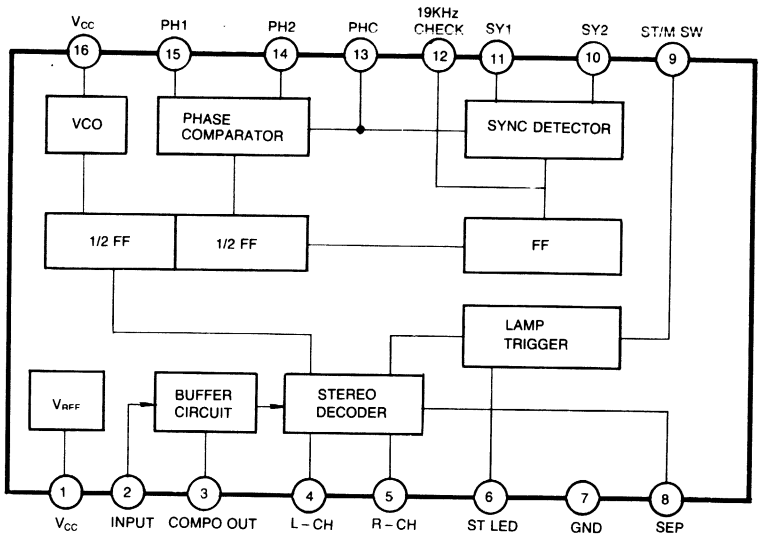


Fig. 1.

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Lamp Current	I_{LAMP}	40	mA
Power Dissipation	P_D	400	mW
Operating Temperature	T_{OPR}	−20 ~ +70	°C
Storage Temeprature	T_{STG}	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(T_a =25°C, V_{CC} =6V, f=1KHz, R_L =3.3KΩ, unless otherwise specified)

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current		I_{CCQ}	V_I = 0		8.5	12	mA
Channel Separation		CS	V_I = 100mV, L + R = 90% P=10%, f=1KHz	35	45		dB
Total Harmonic Distortion	Mono	THD 1	V_I = 100mV		0.2		%
	Stereo	THD 2	L+R=90mV, P=10mV		0.7		%
Output Voltage		V_O	V_I = 100mV, f = 1KHz	66	85	115	mV
Channel Balance		CB	V_I = 100mV, f = 1KHz		0.5	1.5	dB
Lamp on Level		$VL_{(ON)}$	L+R=90%, P=10%		65		mV
Lamp Hysteresis		HY			3.5	6.0	dB
Maximum Input Level		$VI_{(MAX)}$	THD=2%		450		mV
SCA Rejection Ratio		SCA_{REJ}	L+R=90%, P=10%		70		dB
Signal to Noise Ratio		S/N	V_I = 100mV, f = 1KHz		75		dB
Carrier Leakage		V_{LKG}	V_I = 100mV, L + R = 90% P=10%		32		dB
Capture Range		CR	V_I = 100mV, L + R = 90% P=10%		±3		%
Input Impedance		Z_I		15	20		KΩ

TEST CIRCUIT

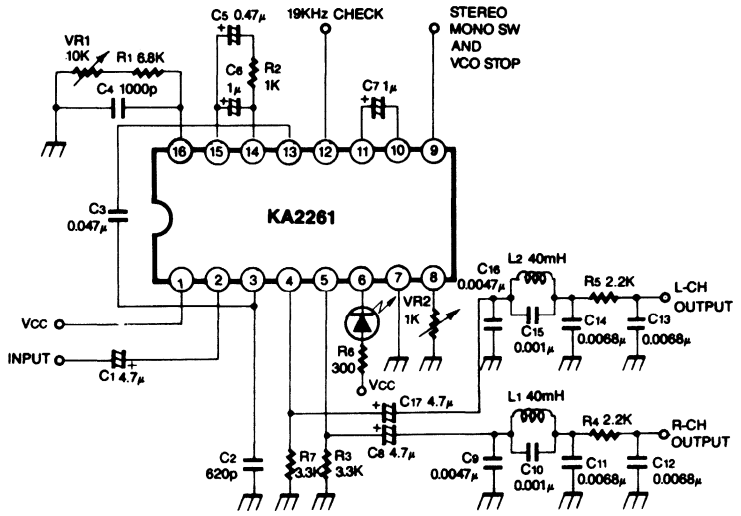
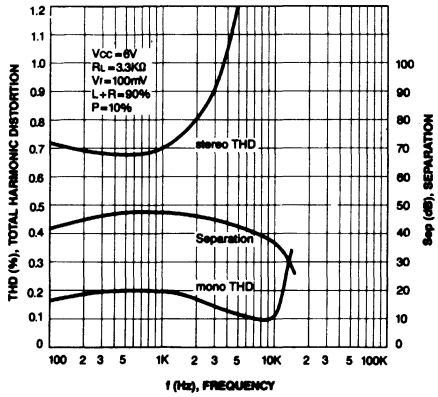
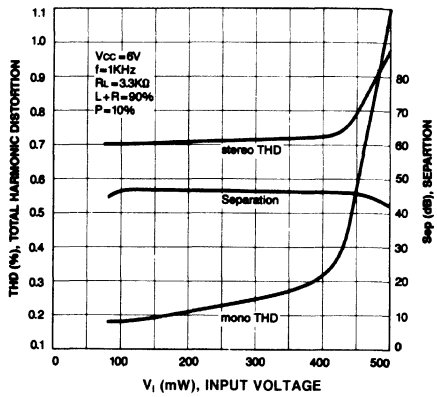


Fig. 2

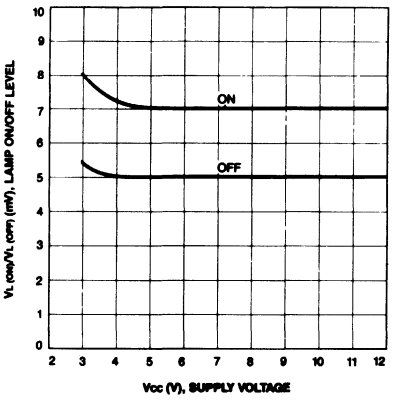
SEPARATION —FREQUENCY
TOTAL HARMONIC DISTORTION



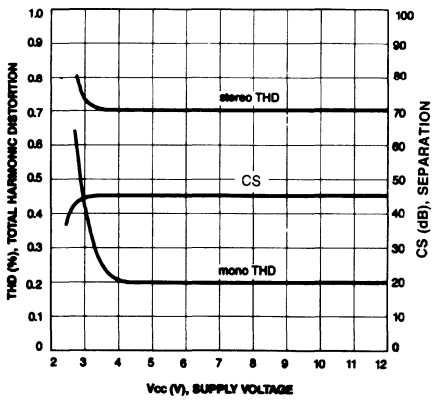
SEPARATION — INPUT VOLTAGE
TOTAL HARMONIC DISTORTION



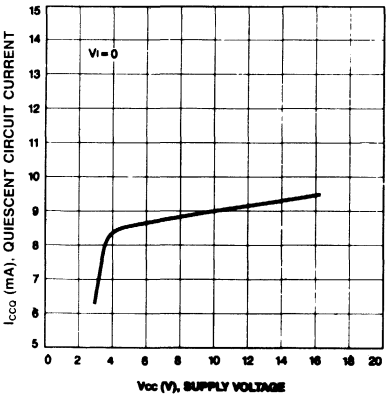
LAMP ON/OFF LEVEL-SUPPLY VOLTAGE



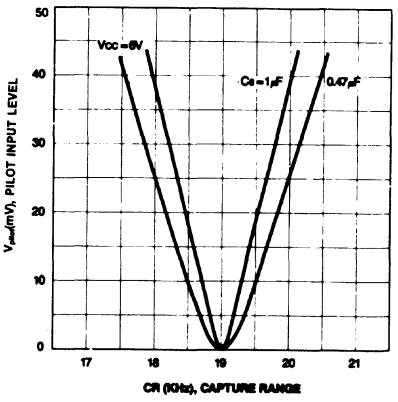
SEPARATION — SUPPLY VOLTAGE
TOTAL HARMONIC DISTORTION



QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE



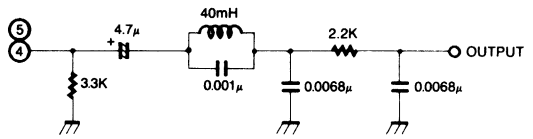
CAPTURE RANGE



APPLICATION INFORMATION
External Components (Refer to Test Circuit)

1. Input coupling capacitor (Pin 2)
   The recommended value is 4.7μF. If smaller values than 4.7μF are used, low frequency separation will worsen, and if larger values are used, the DC operating point will require time for stabilization.

2. Demodulator output (Pin 4, 5)
   These components provide R and L channel output load circuits. The recommended circuits are follows:



3. Separation control (Pin 8)
   This component is a variable resistor used to adjust the out signal separation.

4. Low pass filter (Pins 10, 11)
   This capacitor is used to filter the 19KHz signal detected by the phase comparator. The recommended value is 1μF. If made too small, the lamp may light improvely when a large mono input signal or external noise is received, too large a capacitance value will take more time to switch between mono and stereo modes.

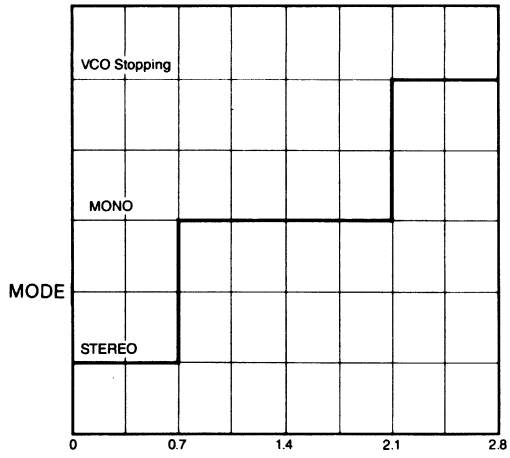
5. Preamplifier output capacitor (Pins 3, 13)
   This capacitor coupled preamplified with phase comparator. The recommanded value is 0.047μF.

6. Phase compensation capacitor (Pin 3, GND)
   This capacitor is prepared in order to compensate the phase advanced.

7. Loop filter (Pins 14, 15)
   This is the low pass filter for the PLL, which is determined the capture range. The recommended value as follows:
   $V_i \leq 250mV$ $C_{14\text{-}15} = 0.47\mu F$
   $V_i \geq 250mV$ $C_{14\text{-}15} = 1\mu F$

8. Control of Pin 9
   Function of Pin 9 is a change-over of stereo/mono and VCO stopping.

SCHEMATIC DIAGRAM of PIN 9 CONTROL

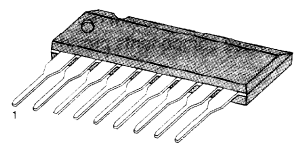


9. VCO network (Pin 16)
   Since the VCO has a negative temperature coefficient, the RC network compensates by using a polyester film capacitor and a resistor.

FM STEREO MULTIPLEX DECODER

The KA2263 is a monolithic integrated circuit consisting of a phase locked loop FM stereo demodulator. It was designed for use in car stereo, cassette recorder and other equipment.

9 SIP



FEATURES

- **Wide operating supply voltage range: V_{CC} = 3V ~ 12V**
- **High pilot lamp ON sensitivity.**
  $VL_{(ON)}$ = 9mV (Typ).
- **Built-in stereo indicator lamp drive circuit.**
  Maximum lamp current: 20mA (continuous).
- **High channel separation: CS = 45dB (Typ).**
- **Low distortion**
  THD = 0.08% (Typ) at V_I = 200mV.
- **VCO stop and stereo lamp turn off are simultaneously operated by connected pin 7 to V_{CC}.**
- **Minimum number of external parts required.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2263	9 SIP	– 20°C ~ + 70°C

BLOCK DIAGRAM

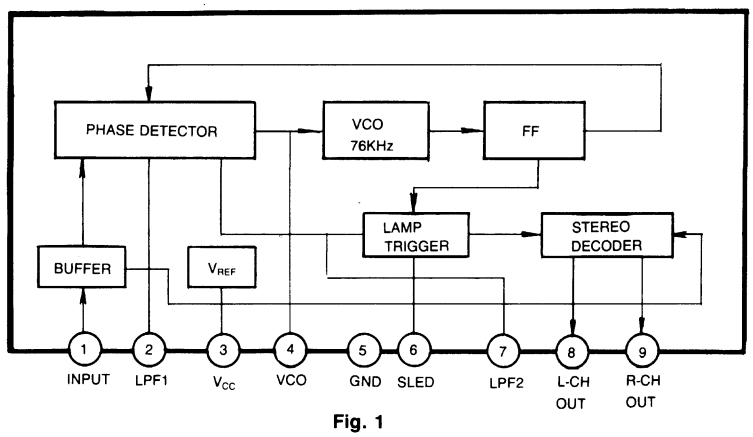


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	12	V
Lamp Voltage	V_{LAMP}	16	V
Lamp Current	I_{LAMP} (continuous)	20	mA
	$I_{LAMP(PEAK)}$	40	mA
Power Dissipation	P_D	500*	mW
Operating Temperature	T_{OPR}	−20 ~ +70	°C
Storage Temeprature	T_{STG}	−40 ~ +125	°C

*Derated above T_a =25°C in the proportion of 4mW/°C

ELECTRICAL CHARACTERISTICS

(T_a =25°C, V_{CC} =8V, f=1KHz, unless otherwise specified)

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current		I_{CCQ}	V_I = 0		11	18	mA
Maximum Input Voltage		$V_{I(MAX)}$	L+R=90%, P=10%, THD=1%		550		mV
Channel Separation		CS	L+R=180mV P=20mV	36	45		dB
Total Harmonic Distortion	Mono	THD 1	V_I =200mV		0.08	0.3	%
	Stereo	THD 2	L+R=180mV P=20mV		0.08		%
Voltage Gain		G_V	V_I =200mV	−2.0	0	+2.0	dB
Channel Balance		C B	V_I =200mV		0	1.5	dB
Lamp ON Level		$VL_{(ON)}$	Pilot only		9	15	mV
Lamp OFF Level		$VL_{(OFF)}$	Pilot only	2	6		mV
Lamp Hysteresis		HY			3		mV
Carrier Leakage	19KHz	V_{LKG}	L+R=180mV		34		dB
	38KHz		P=20mV		42		dB

TEST CIRCUIT

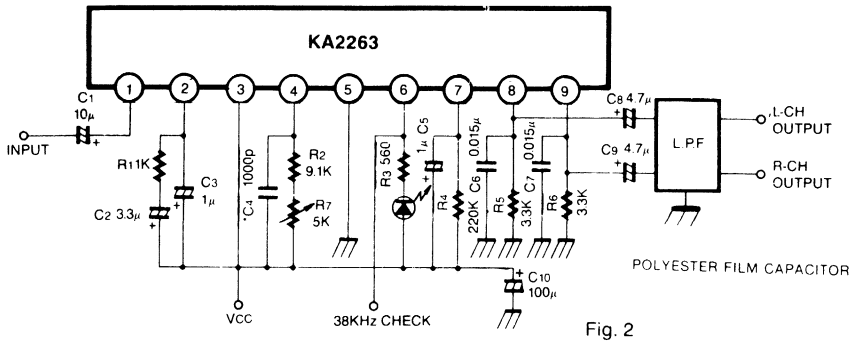
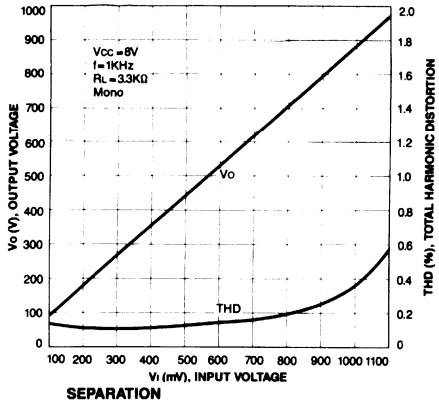
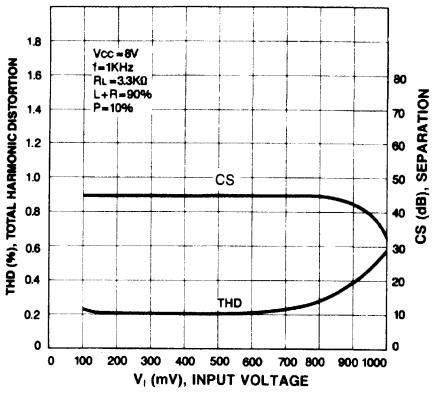


Fig. 2

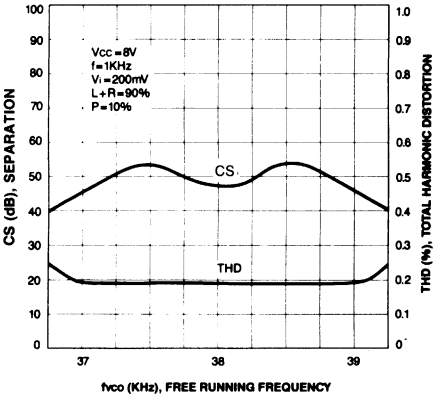
OUTPUT VOLTAGE TOTAL HARMONIC DISTORTION —INPUT VOLTAGE



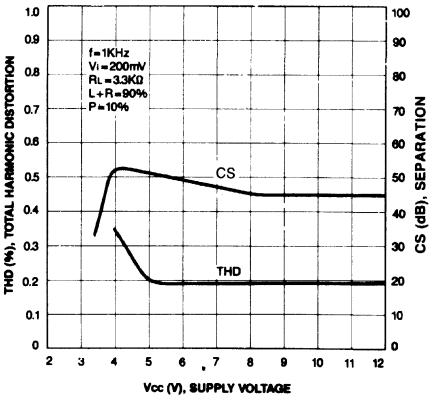
SEPARATION TOTAL HARMONIC DISTORTION —INPUT VOLTAGE



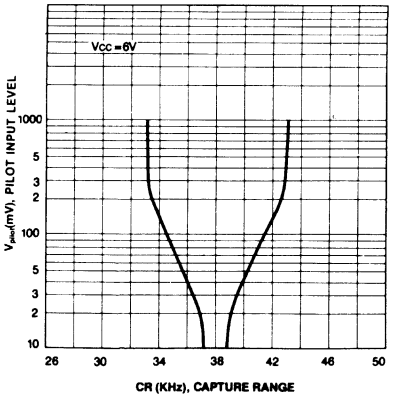
SEPARATION TOTAL HARMONIC DISTORTION —FREE RUNNING FREQUENCY



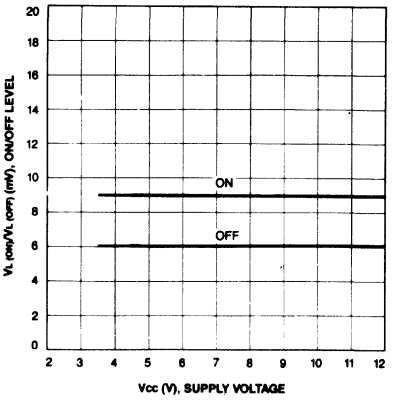
SEPARATION TOTAL HARMONIC DISTORTION —SUPPLY VOLTAGE



CAPTURE RANGE

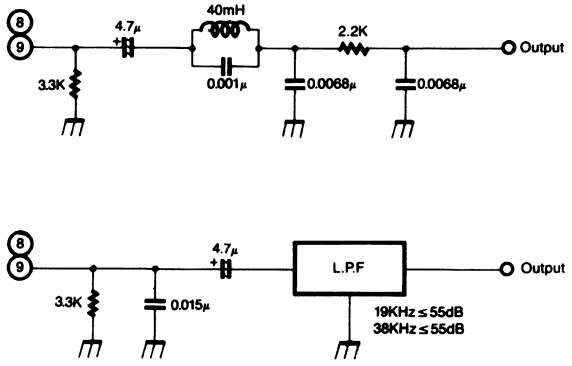


LAMP ON/OFF LEVEL-SUPPLY VOLTAGE

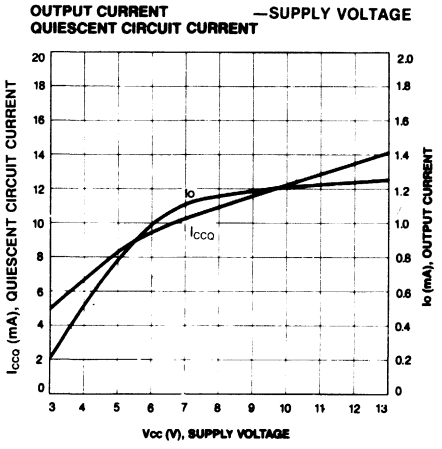


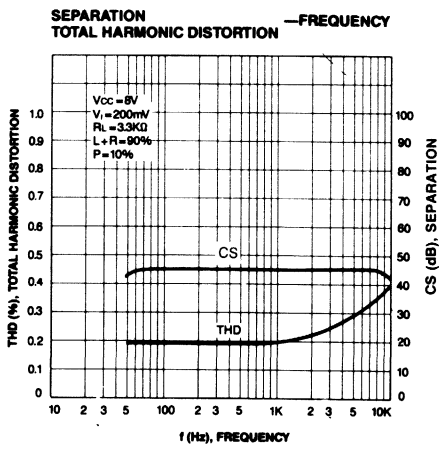
APPLICATION INFORMATION
External Components (Refer to Test Circuit)

1. Input coupling capacitor (C_1)
   The recommended value is 10μF. If smaller values than 10μF are used, low frequency separation will worsen, and if larger values are used, pop noise occurs strongly.
2. Low pass filter (C_2, C_1, R_1)
   This is the low pass filter fr the PLL, which is determined the capture range and THD at low frequency.
3. VCO network (C_4, R_2, R_7)
   The VCO free running frequency is adjusted by connecting a frequency counter to monitor the 38KHz output of Pin 6.
4. Decoder output (Pins 8, 9)
   These components provide R and L channel output load circuits. The recommended circuits as follows:



5. Lamp sensitivity control (R_4)
   Lamp on level can be controlled by this resistor.

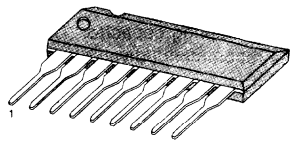




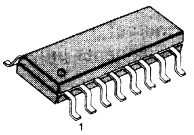
FM STEREO MULTIPLEX DECODER

The KA2264 is a monolithic integrated circuit consisting of a phase locked loop FM stereo demodulator. It is designed for use in 3V radio cassette recorders.

9 SIP



16 SOP



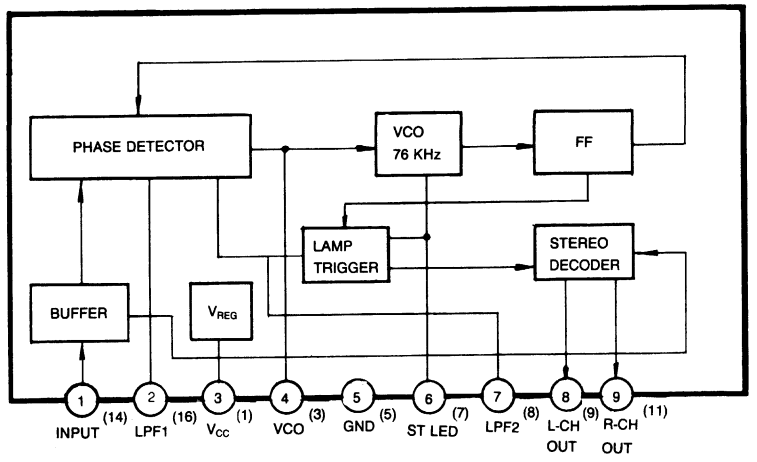
FEATURES

- **Low voltage operation: V_{CC} = 1.8V ~ 5V.**
- **Excellent space-factor: 9 SIP/16 SOP.**
- **Minimum number of external parts required.**
- **Easy monitoring of VCO free running frequency is available at Pin 6.**
- **High pilot sensitivity: $VL_{(ON)}$ = 9mV (Typ).**
- **Lamp drive current: max lamp current = 8mA.**
- **VCO stop and stereo lamp turn-off are simultaneously operated by connecting Pin 7 to V_{CC}.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2264	9 SIP	−20°C ~ +70°C
KA2264D	16 SOP	

BLOCK DIAGRAM



( ): KA2264D

Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Characteristic		Symbol	Value	Unit
Supply Voltage		V_{CC}	6	V
Lamp Voltage		V_{LAMP}	8	V
Lamp Current		I_{LAMP}	8	mA
Power Dissipation	KA2264	P_D	500	mW
	KA2264D		350	
Operating Temperature		T_{OPR}	−20 ~ +70	°C
Storage Temperature		T_{STG}	−40 ~ +125	°C

* Derated above T_a = 25°C in the proportion of 4mW/°C (KA2264D: 2.8mW/°C)

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 3V, f = 1KHz, unless otherwise specified)

Characteristic		Symbol	Test Conditions		Min	Typ	Max	Unit
Circuit Current		I_{CCQ}	V_I = 0			4.5	8.0	mA
Maximum Input Voltage		$V_{I\,(MAX)}$ Stereo	L + R = 90%, P = 10% f = 1KHz, THD = 5%			400		mV
Channel Separation		CS	L + R = 180mV P = 20mV	f = 100Hz		35		dB
				f = 1KHz	30	35		
				f = 10KHz		35		
Total Harmonic Distortion	Mono	THD 1	V_I = 200mV			0.4	1.0	%
	Stereo	THD 2	L + R = 180mV, P = 20mV			0.5		
Voltage Gain		G_V	V_I = 200mV		−6.5	−5.0	−3.5	dB
Channel Balance		CB	V_I = 200mV			0	1.5	dB
Signal to Noise Ratio		S/N	V_I = 200mV R_G = 620Ω			82		dB
Lamp Level	ON	$VL_{(ON)}$	Pilot only			9	15	mV
	OFF	$VL_{(OFF)}$			2	6		
Lamp Hysteresis		HY				3		mV
Capture Range		CR	P = 20mV			±3		%
Carrier Leakage	19KHz	V_{LKG}	P = 20mV L + R = 180mV			32		dB
	38KHz					60		

TEST CIRCUIT 1

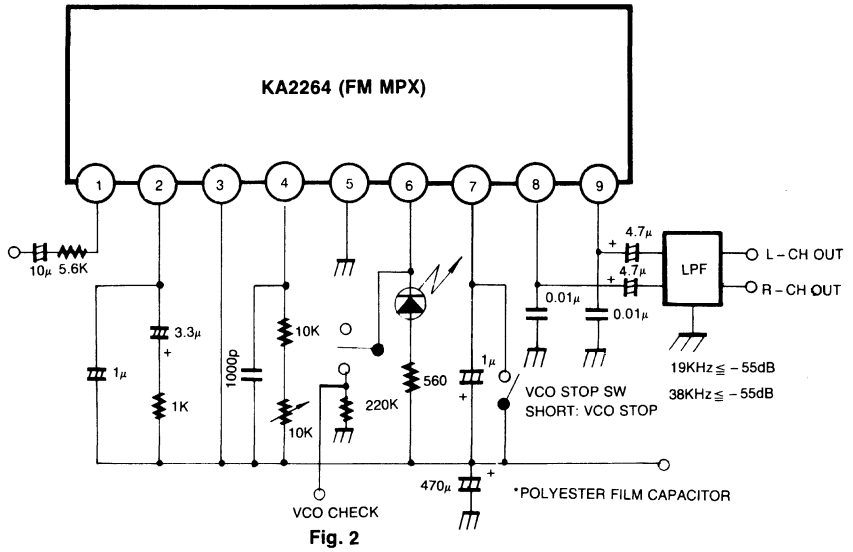


Fig. 2

TEST CIRCUIT 2

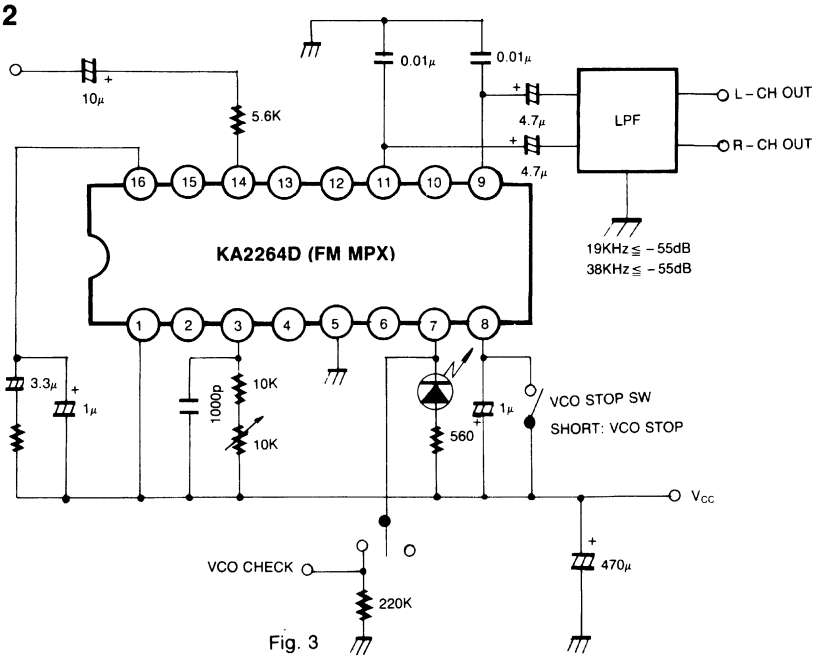
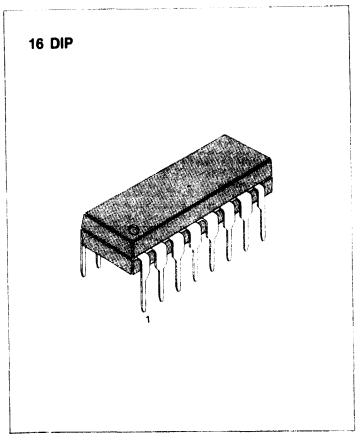


Fig. 3

VCO NON-ADJUSTING FM STEREO MULTIPLEX DECODER

The KA2265 is a monolithic integrated circuit consisting of a VCO non-adjusting FM stereo demodulator with a phase locked loop. It is designed for use in home stereo, portable Hi-Fi.



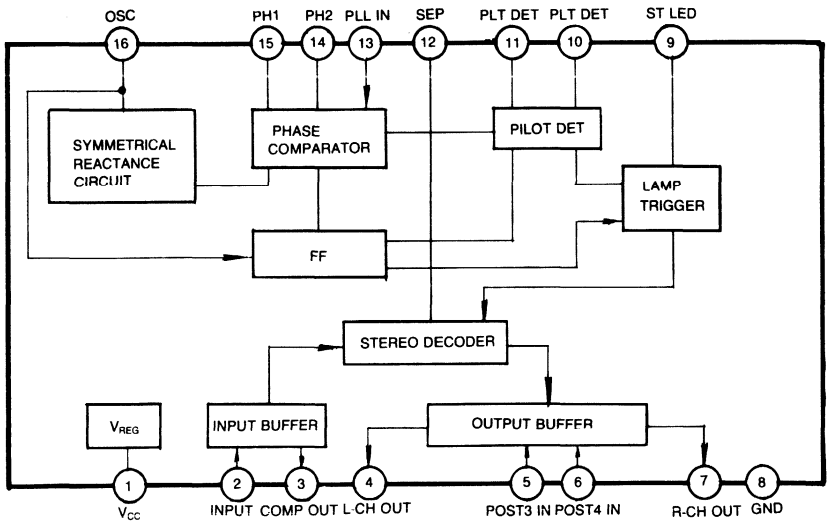
FEATURES

- **Non-adjusting VCO: non-adjusting of free-running frequency.**
- **Excellent temperature characteristics of VCO: ± 0.1% (Typ) at ± 50°C.**
- **Excellent stereo high frequency distortion. (f=10KHz: 0.06% (Typ)).**
- **Excellent distortion: f = 1KHz, V_I = 300mV, mono: 0.025% (Typ). stereo: 0.02% (Typ)**
- **High S/N: 91dB (Typ) (mono V_I = 300mV, LPF). 92dB (Typ) (mono V_I = 300mV, IHF BPF).**
- **High gain: about 8.5dB.**
- **Wide dynamic range: mono 800mV (f=1KHz, THD=1%)**
- **Good ripple rejection: 34dB (Typ).**
- **Operating voltage range: V_{CC} = 6.5V ~ 14V**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2265	16 DIP	– 20°C ~ + 70°C

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

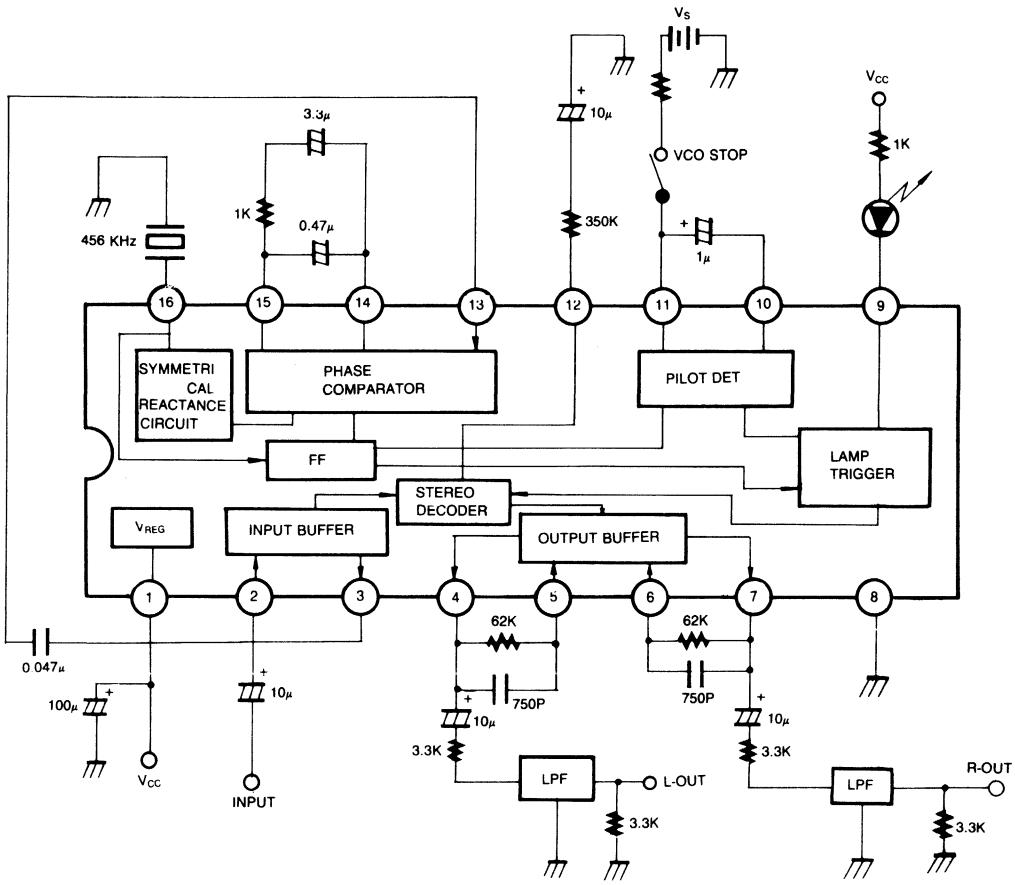
Characteristic	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	16	V
Lamp Current	I_{LAMP}	30	mA
Power Dissipation	P_D	480	mW
Operating Temperature	T_{OPR}	− 20 ~ + 70	°C
Storage Temperature	T_{STG}	− 40 ~ + 125	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 12V, f = 1KHz, T_a = 25°C, unless otherwise specified)

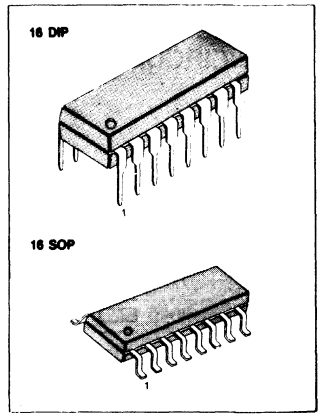
Characteristic		Symbol	Test Conditions		Min	Typ	Max	Unit
Circuit Current		I_{CC}	V_I = 0			18.5	28	mA
Channel Separation		CS	P=30mV, L+R=270mV	f=100Hz		45		dB
				f = 1KHz	40	55		
				f = 10KHz		42		
Total Harmonic Distortion	Stereo	THD 1	P = 30mV L + R = 270mV	f = 100Hz		0.025	0.15	%
				f=1KHz		0.02		
				f = 10KHz		0.06	0.15	
	Mono	THD 2	V_I = 300mV			0.025	0.15	
Output Voltage		V_O	V_I = 300mV		500	730	1000	mV
Channel Balance		CB	V_I = 300mV			0	1	dB
Lamp ON Level		$VL_{(ON)}$	Pilot Level		4	8	17	mV
Lamp Hysteresis		HY				3		dB
Capture Range		CR	P=30mV			+0.8 −1.2		%
Signal to Noise Ratio		S/N	V_I = 300mV R_G = 5.1KΩ		80	91		dB
Input Impedance		Z_I				20		KΩ
Maximum Input Level		$V_{I\,(MAX)}$	Mono, THD=1%		700	800		mV
Carrier Leakage		V_{LKG}	P=30mV, L+R=270mV			31		dB
VCO Stop Voltage		$V_{STOP\,(VCO)}$			5.5		V_{CC}-3	V
Ripple Rejection Ratio		RR				34		dB

TEST CIRCUIT



DOLBY* B-TYPE NOISE REDUCTION PROCESSOR

The KA2271 is a monolithic integrated circuit designed for use in Dolby*B-type noise reduction systems.



FEATURES

- **Few external components**
- **Low quiescent circuit current (typ I_{CCQ} = 4.3mA)**
- **High crosstalk rejection ratio**
- **Built in NR-switch, REC/PB-switch**
- **Recommended supply voltage: V_{CC} = 8V ~ 16V**

BLOCK DIAGRAM

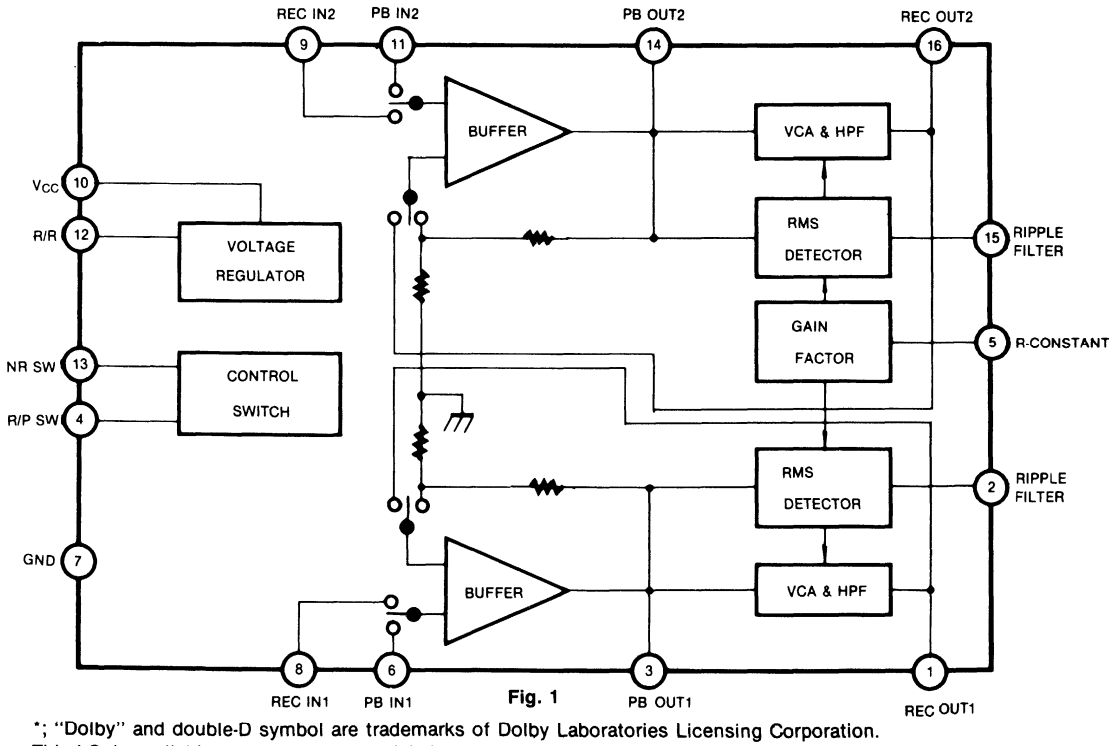


Fig. 1

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2271	16 DIP	−30°C ~ +85°C

*; "Dolby" and double-D symbol are trademarks of Dolby Laboratories Licensing Corporation.
This I.C. is available only to licensees of Dolby Laboratories Licensing Corporation, San Francisco, from whom licensing and application information must be obtained.

PIN CONFIGURATION

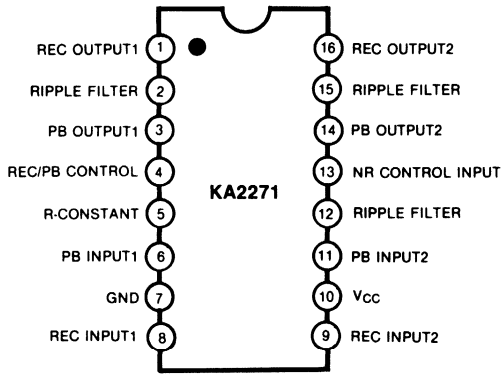


Fig. 2

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Power Dissipation	P_D	750	mW
Operating Temperature	T_{OPR}	− 30 ~ + 85	°C
Storage Temperature	T_{STG}	− 40 ~ + 125	°C

Note: Derated above Ta = 25°C in the propation of 10mW/°C

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 12V, f = 1KHz, 0dB = 245mV (– 10dBm). at REC OUT, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CCQ}	REC mode, NR-off, V_I = 0	3.5	4.3	6	mA
Buffer Voltage Gain	G_V	REC mode, PBout = 0dB	25	27	29	dB
NR-REC Boost	$G_{V(BST)}$	RECout = – 25dB, f = 500Hz	1.4	2.5	4.4	dB
		RECout = – 25dB, f = 2KHz	5.5	7.0	8.5	dB
		RECout = – 25dB, f = 5KHz	3.9	5.4	6.9	dB
		RECout = – 40dB, f = 10KHz	9.7	10.4	11.9	dB
		RECout = 0dB, f = 10KHz	– 1.1	0.4	1.9	dB
NR-Boost Balance	CB	NR-REC boost CH to CH ratio		0	1	dB
MAX. RECout level	$V_{O(MAX)}$	REC mode, NR-off THD = 1%	14	16		dB
REC Output Voltage	THD	REC mode, NR-off RECout = 10dB		0.04	0.1	%
		REC mode, NR-on RECout = 10dB		0.04	0.1	%
NR-effect S/N	S/N	REC mode, R_G = 2.2K Filter = CCIR/ARM	65	69		dB
Crosstalk	CT	NR-off OUTPUT = 0dB PB to REC		– 70	– 65	dB
		CH to CH, NR-off OUTPUT = 0dB		– 70	– 65	dB
Input Impedance	Z_I		30	47	60	KΩ
Switch Control Voltage	V_{CTL}	High mode	2.4			V
		Low mode	0		0.4	V
Input Level	REC V_I	REC mode, NR-off RECout = 0dB	19.5	24.5	31.0	mV
	PB V_I	PB mode, NR-off RECout = 0dB	19.5	24.5	31.0	mV
Output Level	V_O	REC mode, NR-off RECout = 0dB Testpoint = PB output	489	549	616	mV

TEST CIRCUIT

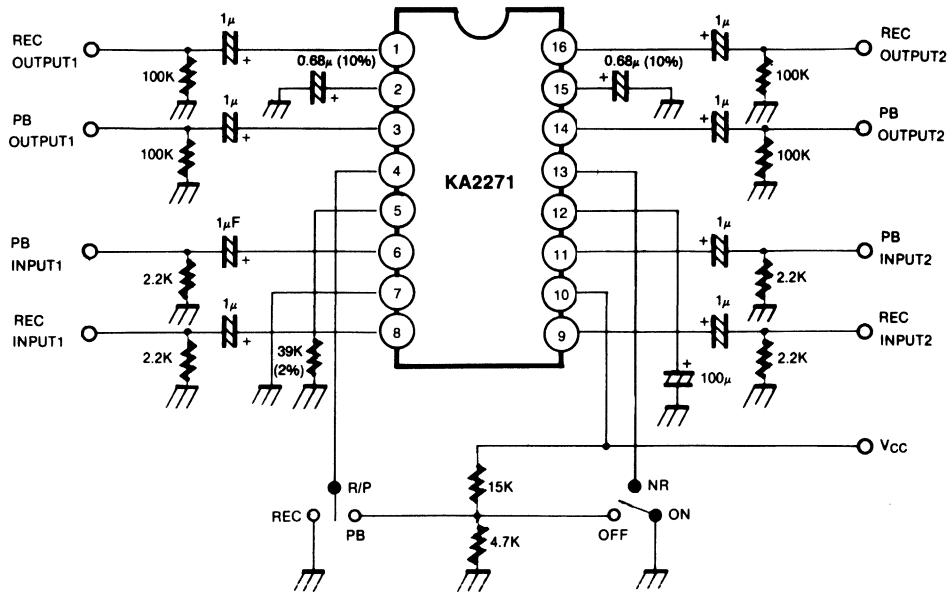
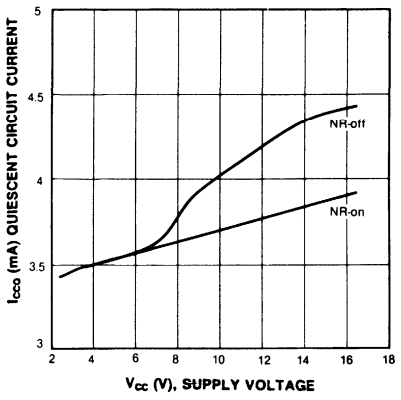
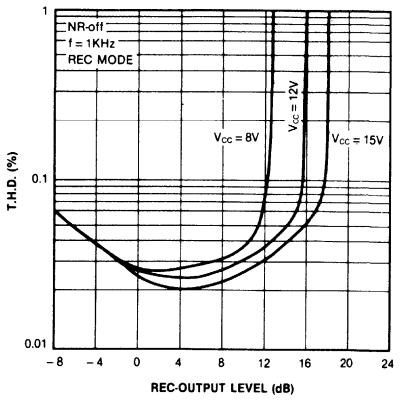


Fig. 3

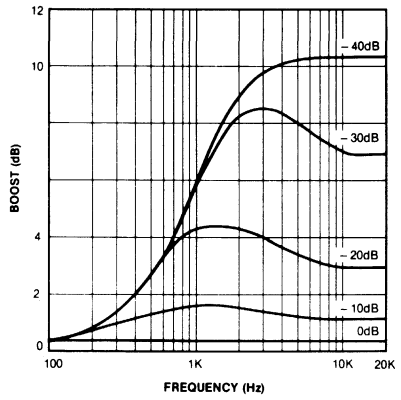
QUIESENTENT CIRCUIT CURRENT-SUPPLY VOLTAGE



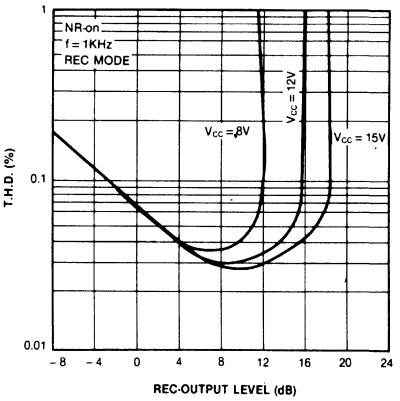
TOTAL HARMONIC DISTORTION (REC)



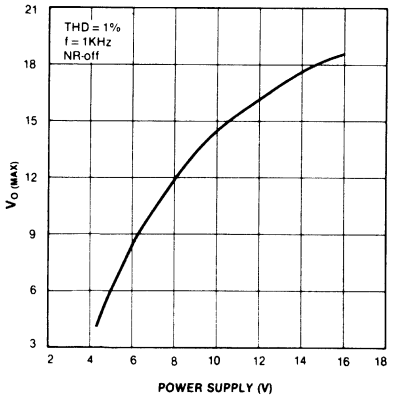
REC (ENCODE) CHARACTERISTIC



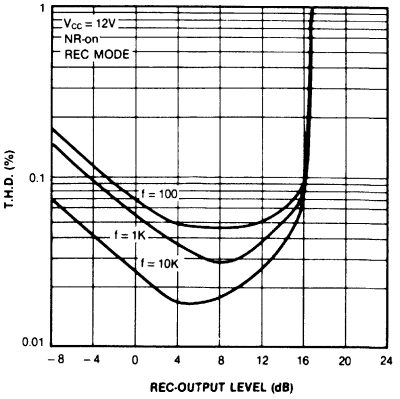
TOTAL HARMONIC DISTORTION (REC)



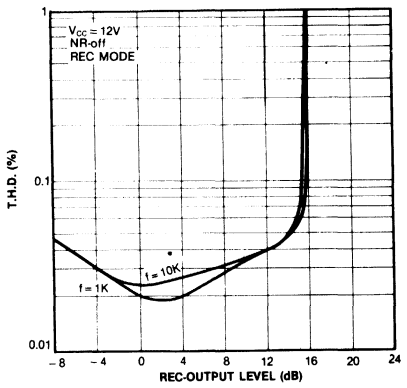
MAX REC-OUTPUT LEVEL



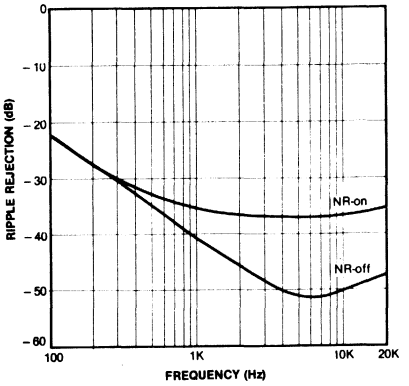
TOTAL HARMONIC DISTORTION (REC)



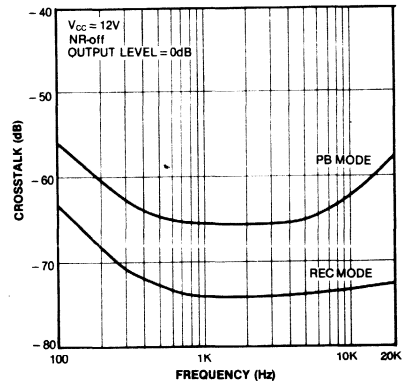
TOTAL HARMONIC DISTORTION (REC)



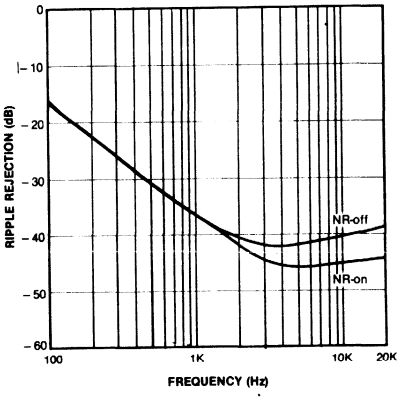
RIPPLE REJECTION (REC)



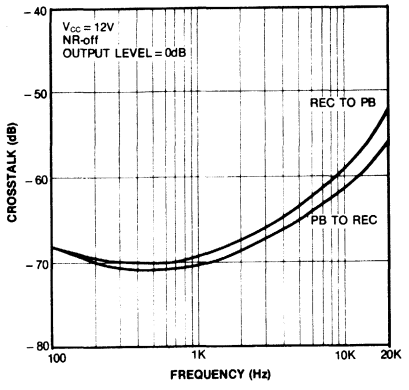
CROSSTALK (CH TO CH)



RIPPLE REJECTION (PB)



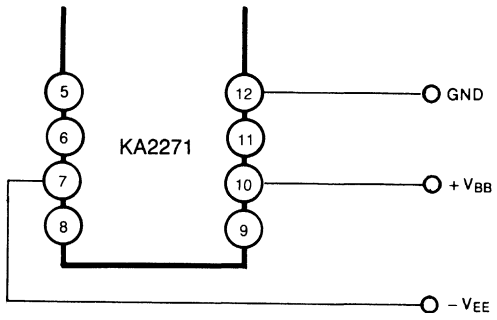
CROSSTALK (BETWEEN REC TO PB)



APPLICATION INFORMATION

1) POWER SUPPLY

The KA2271 can be operated at 8V – 16V in case of single and ±4V – ±8V in dual power supply.



Dual power connection

Fig. 4

2) SWITCH CONTROL VOLTAGE

All function of KA2271 are controlled by internal electronic switchs. The function switch is operated by D.C. voltage of NR and R/P control pins.

NR, R/P	V_H	V_L
Condition	PB	REC
	NR-off	NR-on

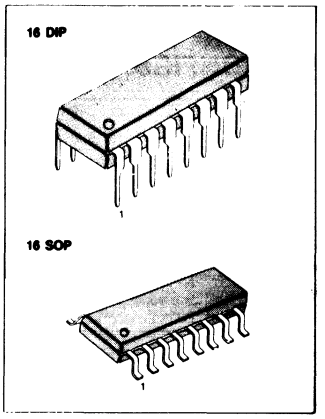
Single Power	Dual Power
$2.4V \leq V_H$ $0.4V \geq V_L$	$V_H \geq V_{EE} + 2.4V$ $V_{EE} + 0.4V \geq V_L$

3) REFERENCE LEVEL

The reference output level of Dolby noise reduction system is defined as Dolby level. The Dolby level of KA2271 is 245mV (– 10dBm) at f = 400Hz.

DOLBY* B-TYPE NOISE REDUCTION PROCESSOR

The KA22711 is a monolithic integrated circuit designed for use in Dolby*B-type noise reduction systems.



FEATURES

- **Few external components**
- **Low quiescent circuit current (typ I_{CCO} = 4.5mA)**
- **High crosstalk rejection ratio**
- **Built in NR-switch, REC/PB-switch**
- **Recommended supply voltage: V_{CC} = 5V ~ 16V**

BLOCK DIAGRAM

ORDERING INFORMATION

Device	Package	Operating Temperature
KA22711	16 DIP	−30°C ~ +85°C

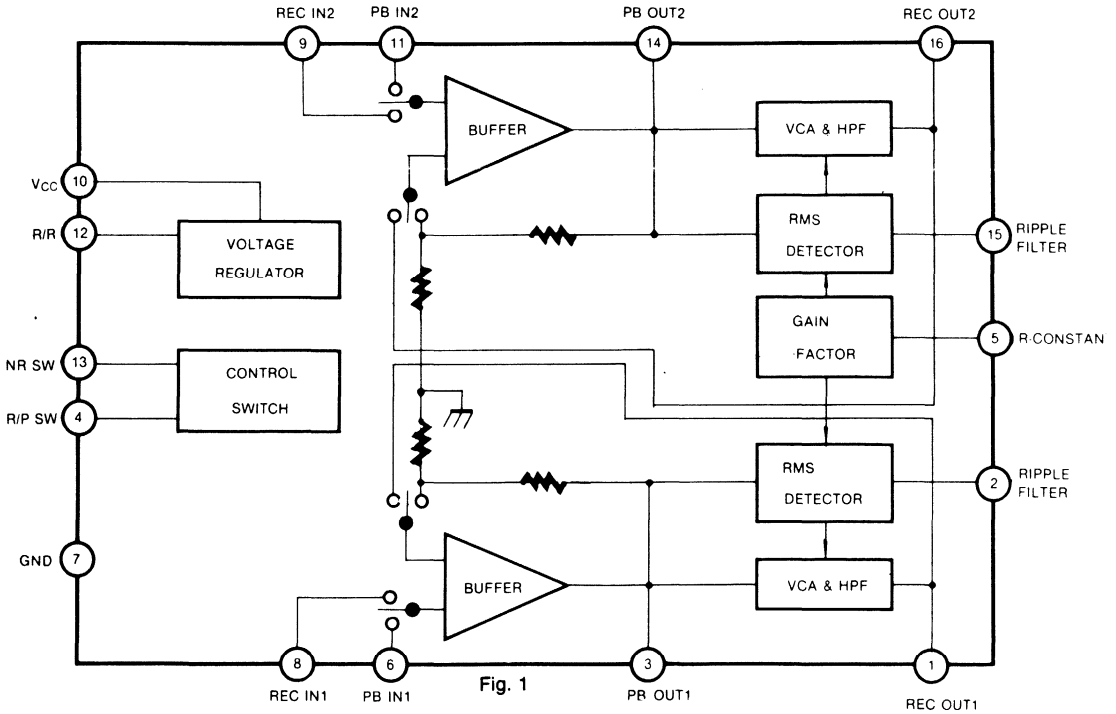


Fig. 1

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PIN CONFIGURATION

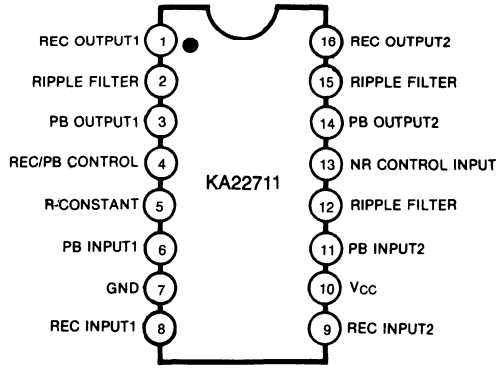


Fig. 2

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Power Dissipation	P_D	750	mW
Operating Temperature	T_{OPR}	−30 ~ +85	°C
Storage Temperature	T_{STG}	−40 ~ +125	°C

Note: Derated above Ta = 25°C in the propation of 10mW/°C

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 6V, f = 1KHz, 0dB = 245mV (– 10dBm) at REC OUT, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CCQ}	REC mode, NR-off, V_{IN} = 0	3.5	4.5	6	mA
Buffer Voltage Gain	G_V	REC mode, PBout = 0dB	19	21	23	dB
NR-REC Boost	$G_{V(BST)}$	RECout = – 25dB, f = 500Hz	1.4	2.9	4.4	dB
		RECout = – 25dB, f = 2KHz	5.5	7.0	8.5	dB
		RECout = – 25dB, f = 5KHz	3.9	5.4	6.9	dB
		RECout = – 40dB, f = 10KHz	9.1	10.4	11.9	dB
		RECout = 0dB, f = 10KHz	– 1.1	0.4	1.9	dB
NR-Boost Balance	CB	NR-REC boost CH to CH ratio		0	1	dB
MAX. RECout level	$V_{O(MAX)}$	REC mode, NR-off THD = 1%	14	15		dB
RECout Distortion	THD	REC mode, NR-off RECout = 10dB		0.04	0.1	%
		REC mode, NR-on RECout = 10dB		0.04	0.1	%
NR-effect S/N	S/N	REC mode, Rg = 2.2K Filter = CCIR/ARM	65	69		dB
Crosstalk	CT	NR-off OUTPUT = 0dB PB to REC		– 75	– 65	dB
		CH to CH, NR-off OUTPUT = 0dB		– 68	– 62	dB
Input Impedance	Z_I		30	47	60	KΩ
Switch Control Voltage	V_{CTL}	High mode	2.4			V
		Low mode	0		0.4	V
Input Level	REC V_I	REC mode, NR-off RECout = 0dB	19.5	24.5	31.0	mV
	PB V_I	PB mode, NR-off RECout = 0dB	19.5	24.5	31.0	mV
Output Level	V_O	REC mode, NR-off RECout = 0dB Testpoint = PB output	218	245	275	mV

TEST CIRCUIT

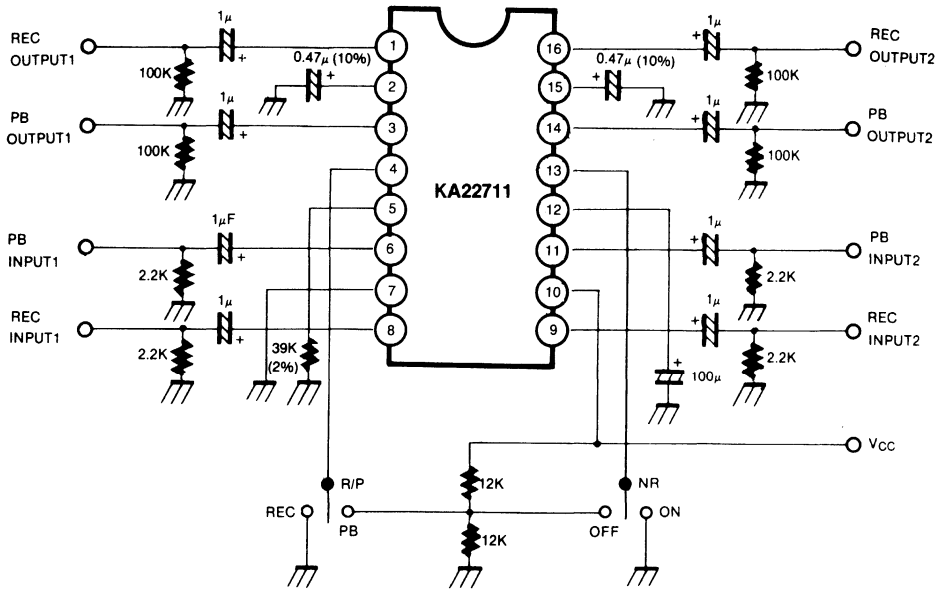
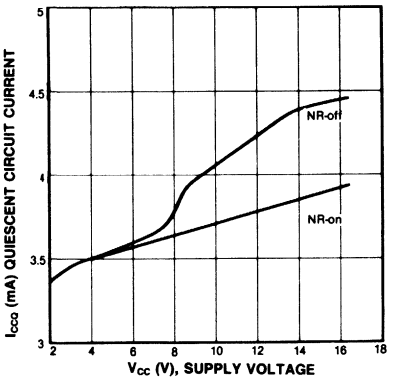
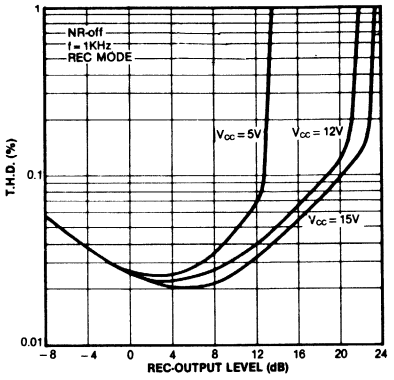


Fig. 3

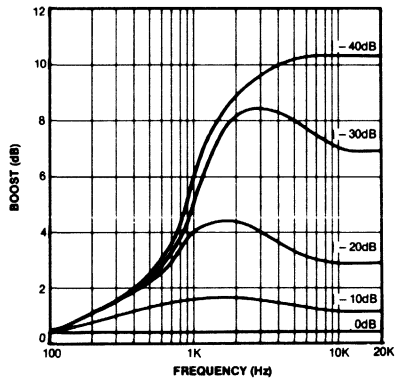
QUIECENT CIRCUIT CURRENT-SUPPLY VOLTAGE



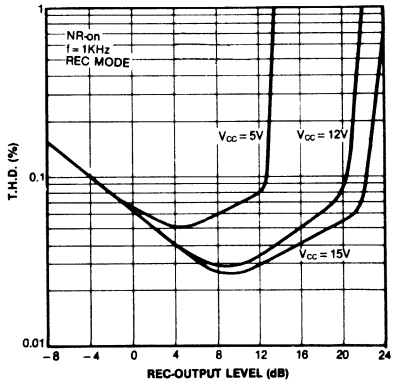
TOTAL HARMONIC DISTORTION (REC)



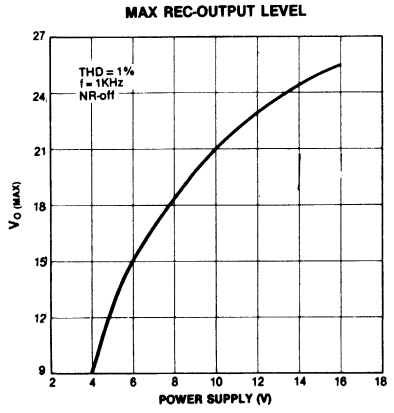
REC (ENCODE) CHARACTERISTIC



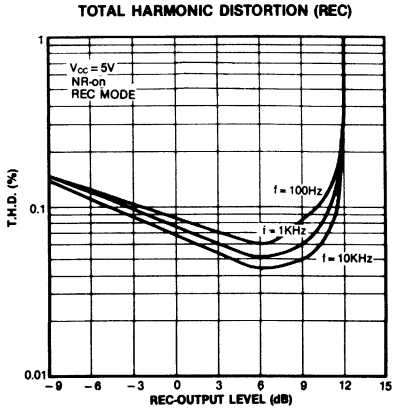
TOTAL HARMONIC DISTORTION (REC)



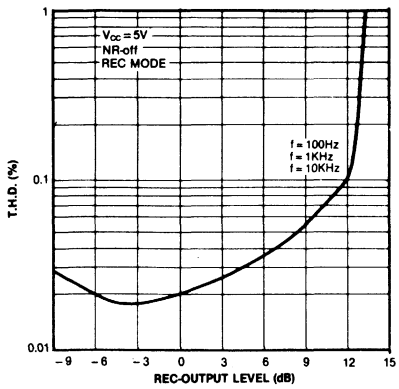
MAX REC-OUTPUT LEVEL



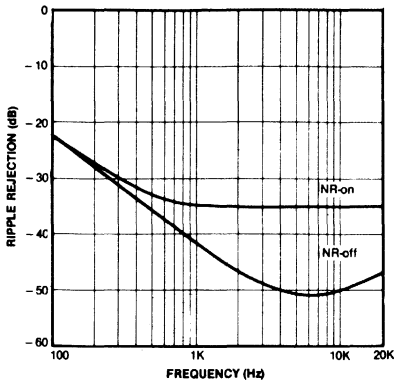
TOTAL HARMONIC DISTORTION (REC)



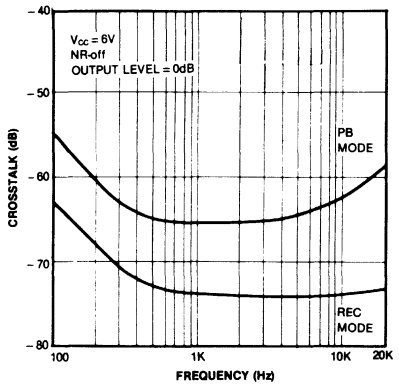
TOTAL HARMONIC DISTORTION (REC)



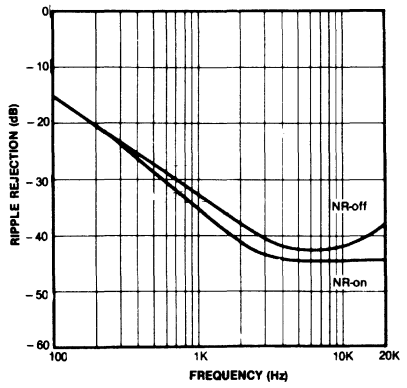
RIPPLE REJECTION (REC)



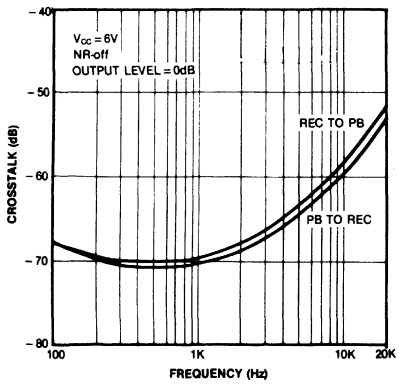
CROSSTALK (CH TO CH)



RIPPLE REJECTION (PB)



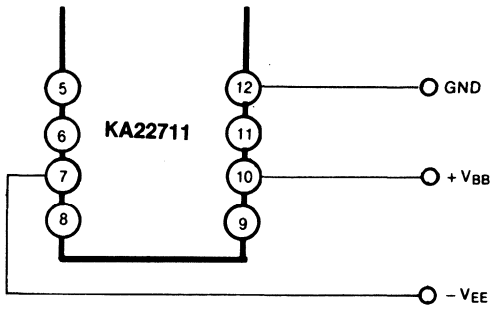
CROSSTALK (BETWEEN REC TO PB)



APPLICATION INFORMATION

1) POWER SUPPLY

The KA22711 can be operated at 8V—16V in case of single and ±2.5V – ±8V in dual power supply.



Dual power connection

Fig. 4

2) SWITCH CONTROL VOLTAGE

All function of KA22711 are controlled by internal electronic switches. The function switch is operated by D.C. voltage of NR and R/P control pins.

NR, R/P	V_H	V_L
Condition	PB	REC
	NR-off	NR-on

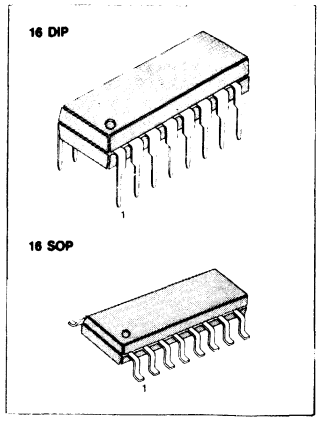
Single Power	Dual Power
$2.4V \leq V_H$ $0.4V \geq V_L$	$V_H \geq V_{EE} + 2.4V$ $V_{EE} + 0.4V \geq V_L$

3) REFERENCE LEVEL

The reference output level of Dolby noise reduction system is defined as Dolby level. The Dolby level of KA22711 is 245mV (– 10dBm) at f = 400Hz.

DOLBY* B-TYPE NOISE REDUCTION PROCESSOR

The KA22712 is a monolithic integrated circuit designed for use in Dolby*B-type noise reduction systems.



FEATURES

- Few external components
- **Low quiescent circuit current (typ I_{CCQ} = 4.5mA)**
- High crosstalk rejection ratio
- Built in NR-switch, REC/PB-switch
- **Recommended supply voltage: V_{CC} = 6.5V ~ 16V**

BLOCK DIAGRAM

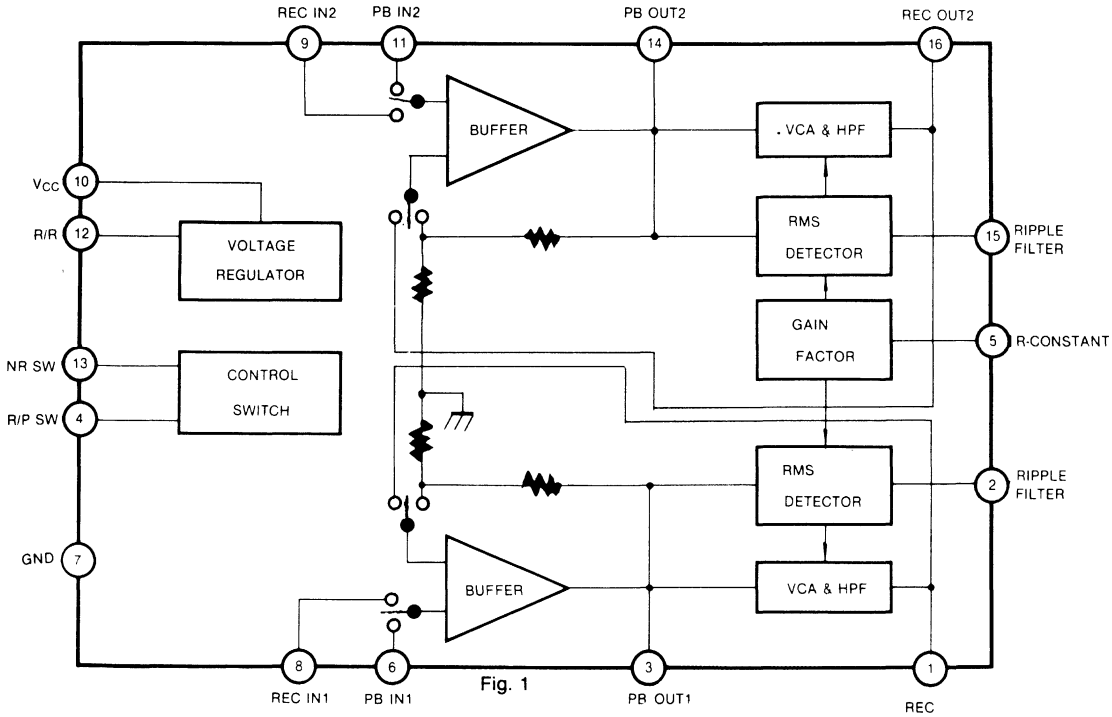


Fig. 1

ORDERING INFORMATION

Device	Package	Operating Temperature
KA22712	16 DIP	−30°C ~ +85°C

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PIN CONFIGURATION

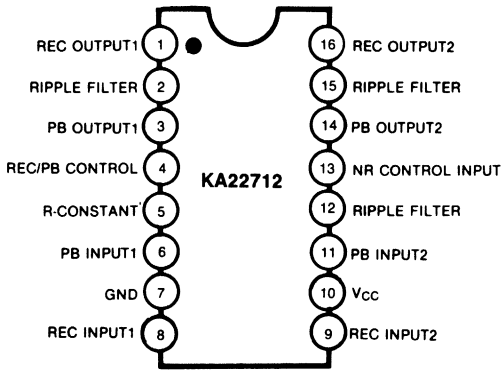


Fig. 2

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Power Dissipation	P_D	750	mW
Operating Temperature	T_{OPR}	−30 ~ +85	°C
Storage Temperature	T_{STG}	−40 ~ +125	°C

Note: Derated above Ta = 25°C in the propation of 10mW/°C

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 9V, f = 1KHz, 0dB = 245mV (−10dBm) at REC OUT, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CCQ}	REC mode, NR-off, V_I = 0	3.5	4.5	6	mA
Buffer Voltage Gain	G_V	REC mode, PBout = 0dB	22	24	26	dB
NR-REC Boost	$G_{V(BST)}$	RECout = −25dB, f = 500Hz	1.4	2.9	4.4	dB
		RECout = −25dB, f = 2KHz	5.5	7.0	8.5	dB
		RECout = −25dB, f = 5KHz	3.9	5.4	6.9	dB
		RECout = −40dB, f = 10KHz	9.1	10.4	11.9	dB
		RECout = 0dB, f = 10KHz	−1.1	0.4	1.9	dB
NR-Boost Balance	CB	NR-REC boost CH to CH ratio		0	1	dB
MAX. RECout level	$V_{O(MAX)}$	REC mode, NR-off THD = 1%	14	16		dB
RECout Distortion	THD	REC mode, NR-off RECout = 10dB		0.04	0.1	%
		REC mode, NR-on RECout = 10dB		0.04	0.1	%
NR-effect S/N	S/N	REC mode, R_G = 2.2K Filter = CCIR/ARM	65	69		dB
Crosstalk	CT	NR-off OUTPUT = 0dB PB to REC		−75	−65	dB
		CH to CH, NR-off OUTPUT = 0dB		−68	−62	dB
Input Impedance	Z_I		30	47	60	KΩ
Switch Control Voltage	V_{CTL}	High mode	2.4			V
		Low mode	0		0.4	V
Input Level	REC V_I	REC mode, NR-off RECout = 0dB	19.5	24.5	31.0	mV
	PB V_I	PB mode, NR-off RECout = 0dB	19.5	24.5	31.0	mV
Output Level	V_O	REC mode, NR-off RECout = 0dB Testpoint = PB output	346	388	436	mV

TEST CIRCUIT

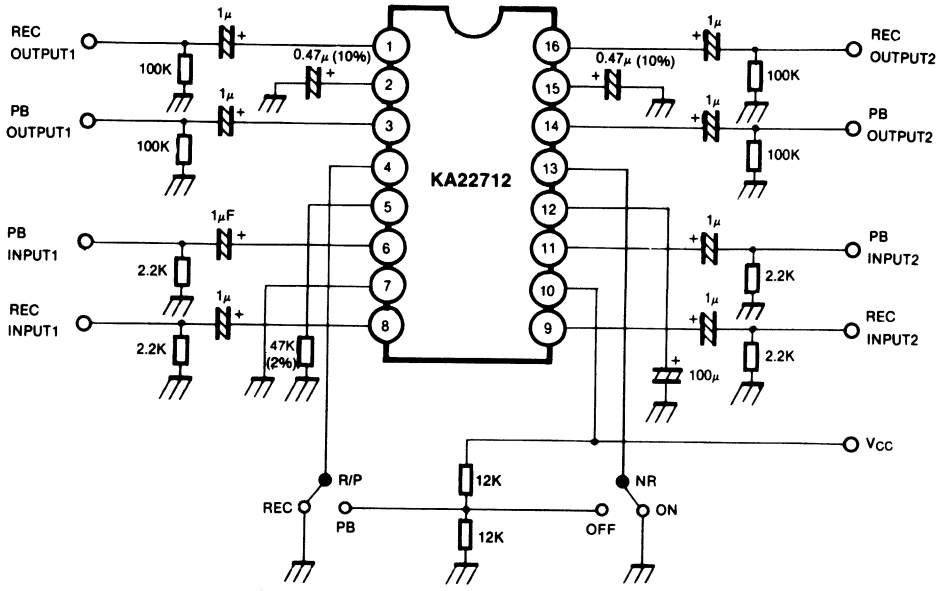
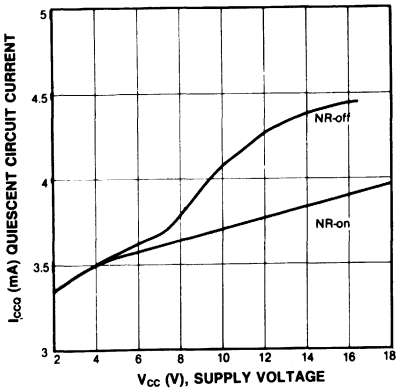
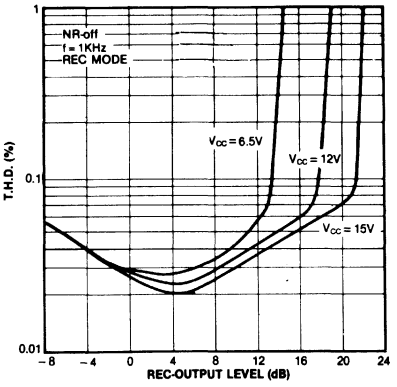


Fig. 3

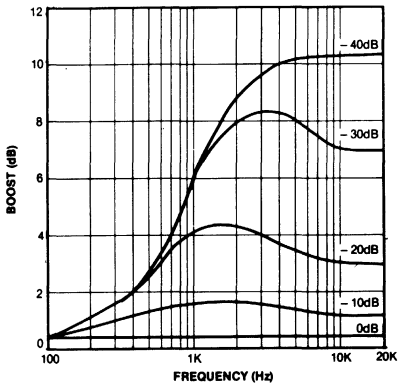
QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE



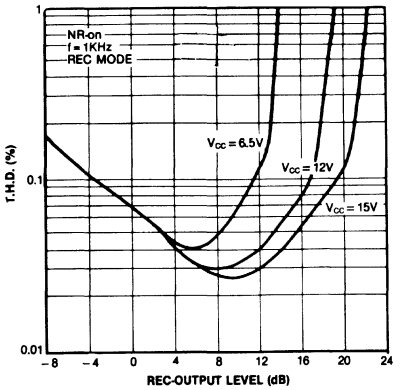
TOTAL HARMONIC DISTORTION (REC)



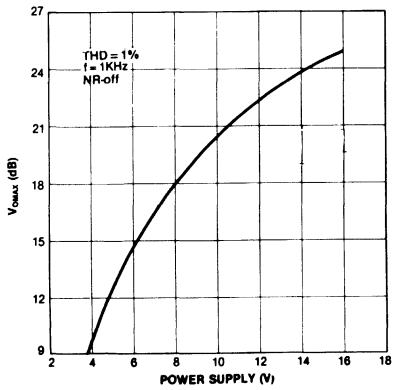
REC (ENCODE) CHARACTERISTIC



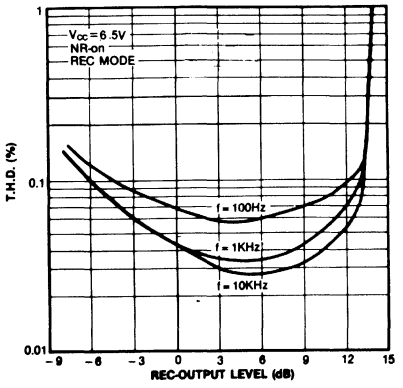
TOTAL HARMONIC DISTORTION (REC)



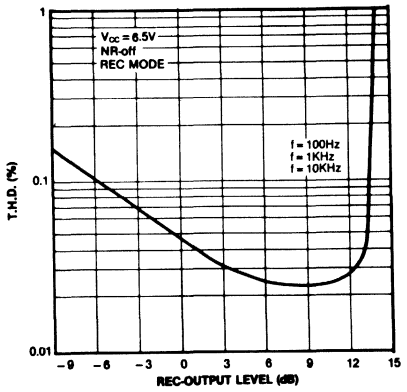
MAX REC-OUTPUT LEVEL



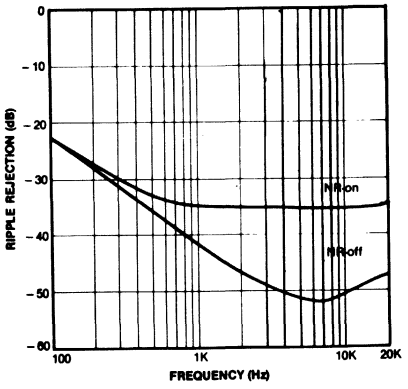
TOTAL HARMONIC DISTORTION (REC)



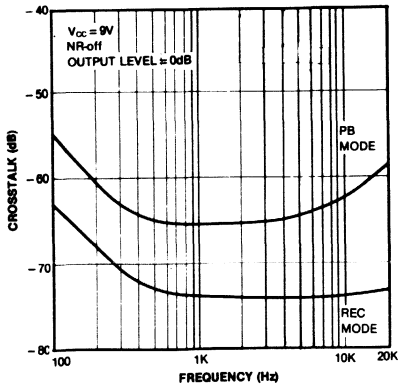
TOTAL HARMONIC DISTORTION (REC)



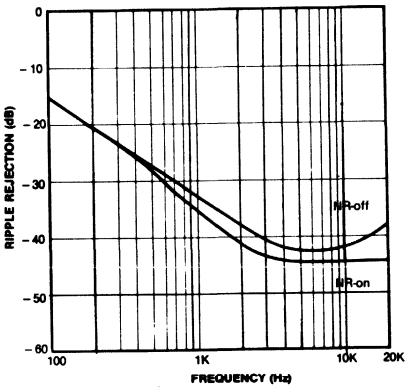
RIPPLE REJECTION (REC)



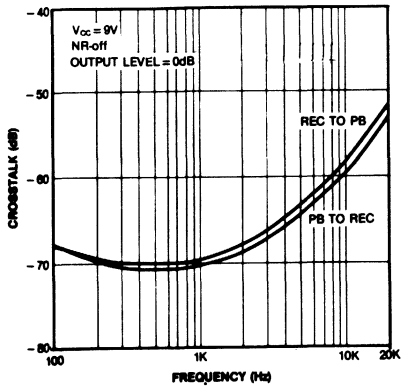
CROSSTALK (CH TO CH)



RIPPLE REJECTION (PB)



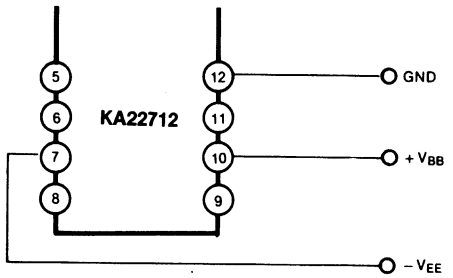
CROSSTALK (BETWEEN REC TO PB)



APPLICATION INFORMATION

1) POWER SUPPLY

The KA22712 can be operated at 6.5V—16V in case of single and ±3.25V – ±8V in dual power supply.



Dual power connection

Fig. 4

2) SWITCH CONTROL VOLTAGE

All function of KA22712 are controlled by internal electronic switches. The function switch is operated by D.C. voltage of NR and R/P control pins.

NR, R/P	V_H	V_L
Condition	PB	REC
	NR-off	NR-on

Single Power	Dual Power
$2.4V \leq V_H$ $0.4V \geq V_L$	$V_H \geq V_{EE} + 2.4V$ $V_{EE} + 0.4V \geq V_L$

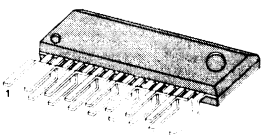
3) REFERENCE LEVEL

The reference output level of Dolby noise reduction system is defined as Dolby level. The Dolby level of KA22712 is 245mV (– 10dBm) at f = 400Hz.

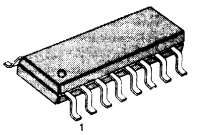
FM NOISE CANCELLER

The KA2272 is a monolithic integrated circuit for the FM noise canceller used in car stereos.
It is used in combination with a PLL FM multiplex demodulator (such as the KA2266) with a pilot signal canceller.

16 ZSIP



16 SOP



FEATURES

- **Operation voltage range: V_{CC} = 8V ~ 15V**
- **Low quiescent circuit current**
- **Low distortion: THD = 0.02% at V_I = 300mV**
- **Pilot signal compensation**
- **The space factor is advantageous because of the signal-end-package.**
- **Built-in monostable multivibrator.**
- **Variable input type noise AGC system.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2272	16 ZSIP	-20°C ~ +75°C
KA2272D	16 SOP	

BLOCK DIAGRAM

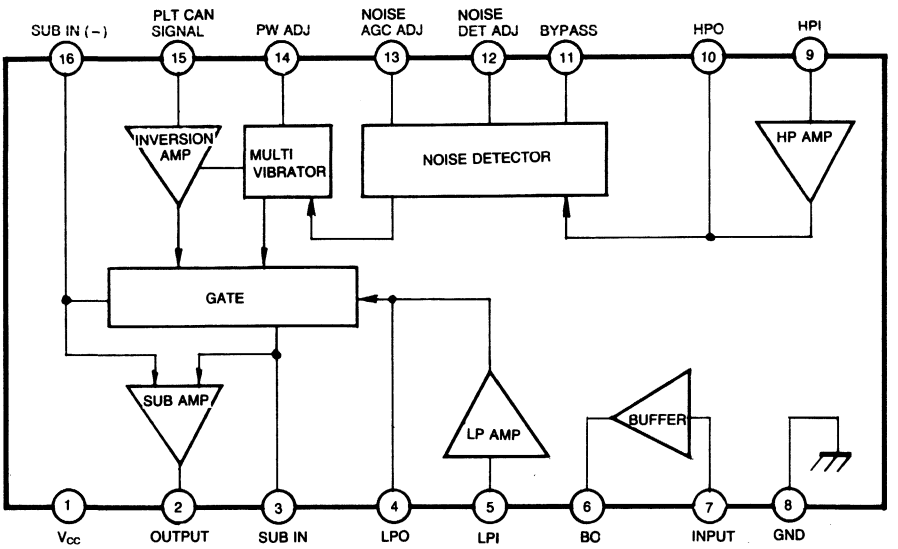


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic		Symbol	Value	Unit
Supply Voltage		V_{CC}	16	V
Power Dissipation	KA2272	P_D	450	mW
	KA2272D		300	mW
Operating Temperature		T_{OPR}	−20 ~ +75	°C
Storage Temperature		T_{STG}	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 12V, V_7 = 300mV, f = 1KHz, unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
		Input Pin	Output Pin				
Quiescent Circuit Current	I_{CCQ}				16	25	mA
Voltage Gain	G_V	V_7 = 300mV, f = 1KHz	Output	−0.2	0.8	1.8	dB
Output Voltage	V_O	V_7, f = 1KHz	Output THD = 1%	1.3			V
Total Harmonic Distortion	THD	V_7 = 300mV, f = 1KHz	Output		0.01	0.03	%
Input Resistance	R_I	V_7 = 300mV, f = 1KHz		36	51	67	KΩ
Lowpass AMP Gain	$G_{V(LP)}$	V_5 = 300mV, f = 1KHz	V_4	0	0.83	1.58	dB
Highpass AMP Gain	A_{VH}	V_9 = 100mV f = 200KHz	V_{10}	1.58	2.92	4.35	dB
Inverted Amp Distortion	THD	f = 19KHz	Output			0.1	%
Inverted Amp Dynamic Range	V_O	V_{15} = 100mV f = 19KHz	Output THD = 1%	300			mV
Inverted Amp Gain	G_V	V_{15} = 100mV f = 19KHz	Output	0	2.28	4.08	dB
Output Noise Voltage	V_{NO}	Bypass V_7, V_{15} to GND	Output, 100KHz LPF		30	60	μV
Gate Time	t_G	V_7 = 100mV$_{p-p}$, 1μs, f = 1KHz	Output	13	21	30	μsec
Noise Sensitivity	SN	V_7, 1μs, f = 1KHz	Output			30	mV$_{p-p}$

TEST CIRCUIT

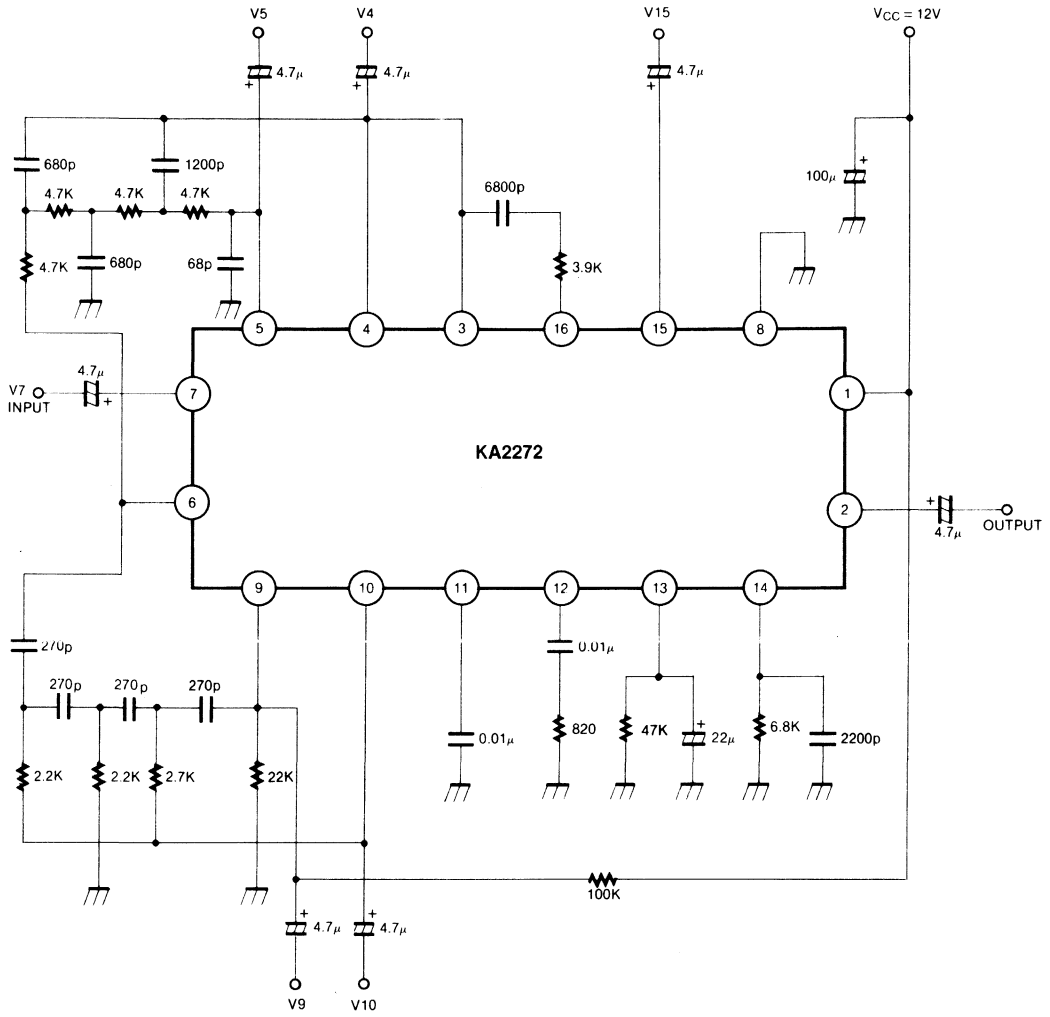
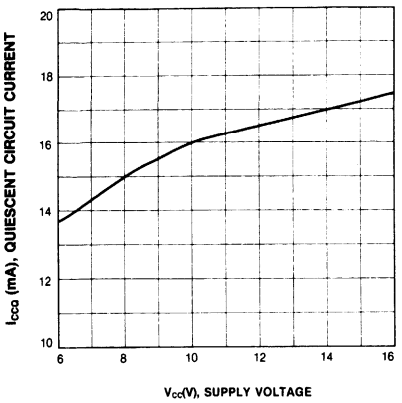
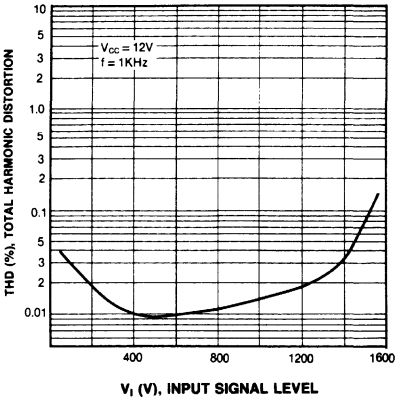


Fig. 2

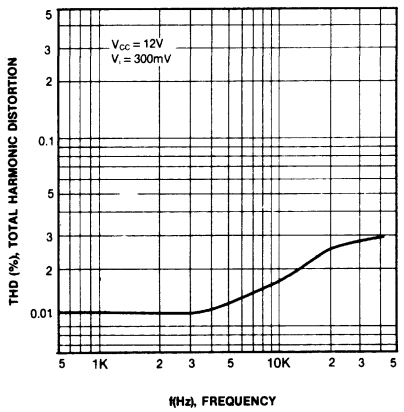
QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE



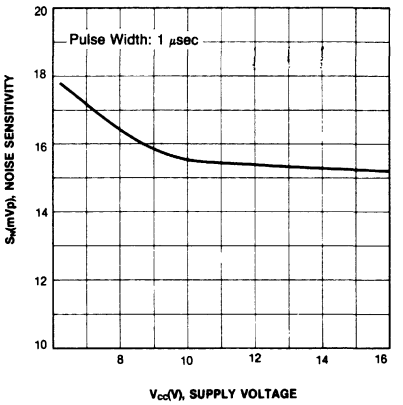
TOTAL HARMONIC DISTORTION-INPUT SIGNAL LEVEL



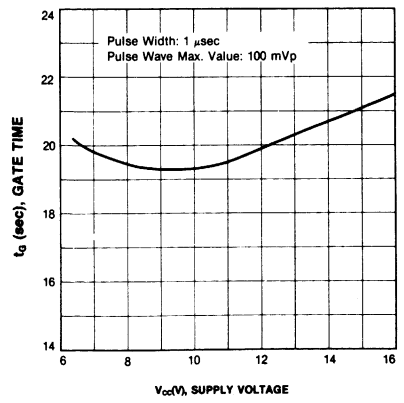
TOTAL HARMONIC DISTORTION-FREQUENCY



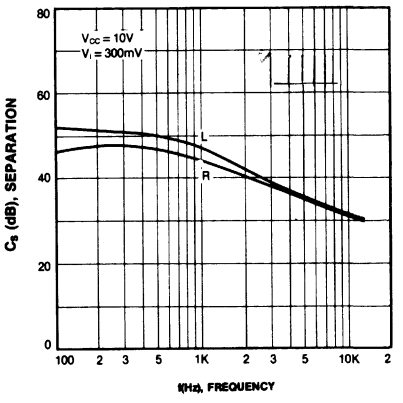
NOISE SENSITIVITY-SUPPLY VOLTAGE



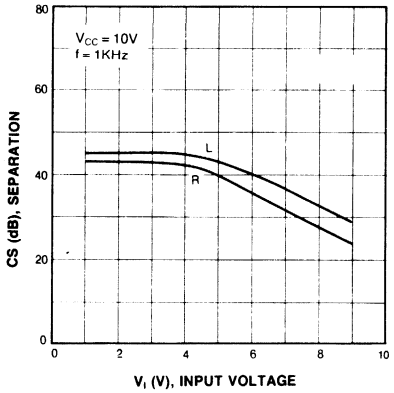
GATE TIME-SUPPLY VOLTAGE



SEPARATION-FREQUENCY



SEPARATION-INPUT VOLTAGE



APPLICATION CIRCUIT

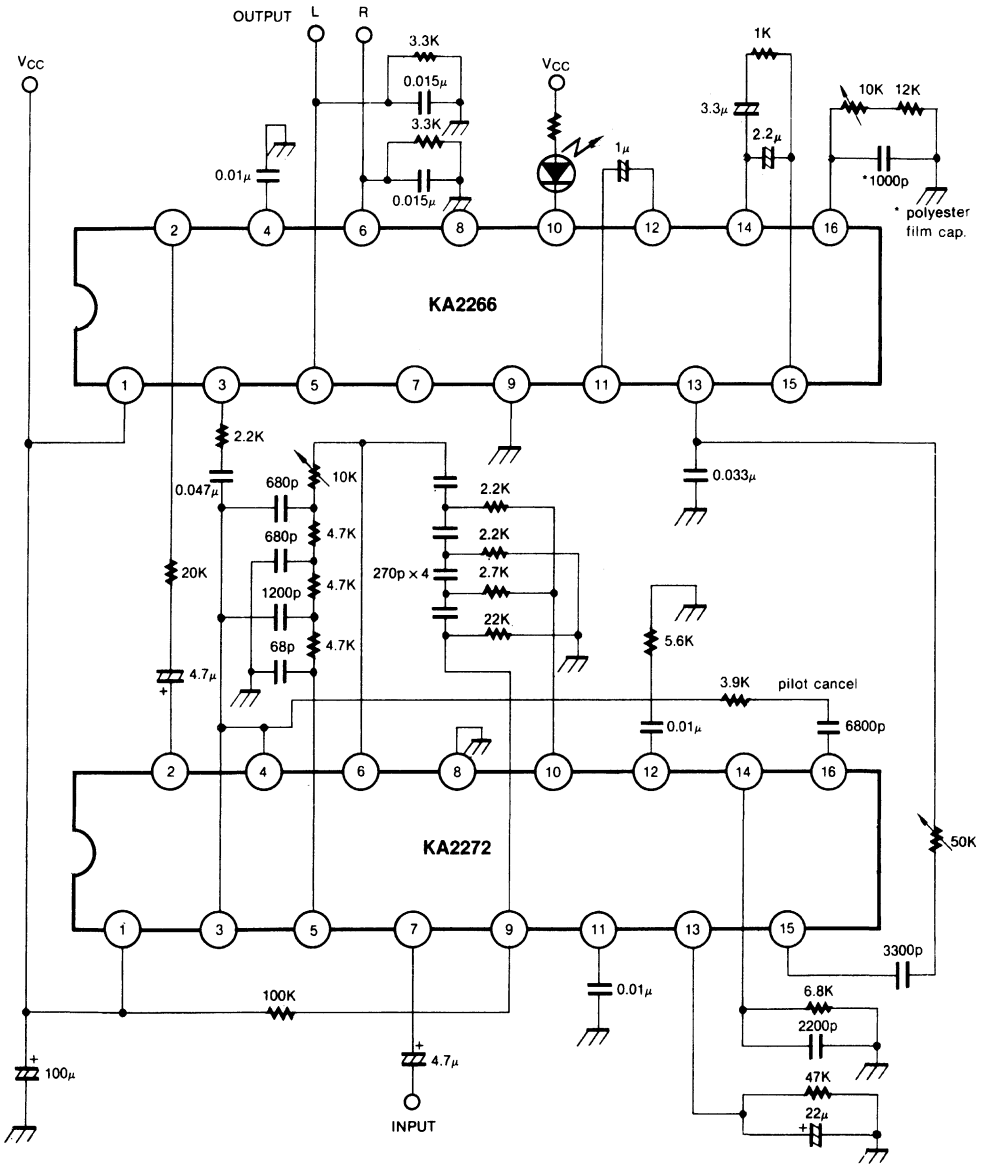
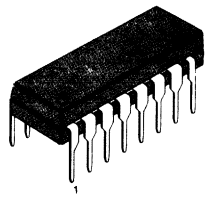


Fig. 3

5-DOT DUAL LED LEVEL METER DRIVER

The KA2281 is a monolithic integrated circuit consisting of a 2-channel LED level meter driver which was designed for use in stereo radio cassette tape recorders and home stereos.

16 DIP



FEATURES

- **Comparator AC level (−16, −11, −6, −3, 0dB)×2.**
- **Capable of driving red/green/yeollow LEDs.**
- **Externally adjustable gain of input amplifier.**
- **Wide operating supply voltage range: V_{CC} = 5V ~ 14V**
- **10-dot dual output combinated with the KA2283.**
- **Applicable to 10-dot mono output.**
- **High input impedance.**
- **A minimum number of external parts required.**

BLOCK DIAGRAM

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2281	16 DIP	−20 ~ +70°C

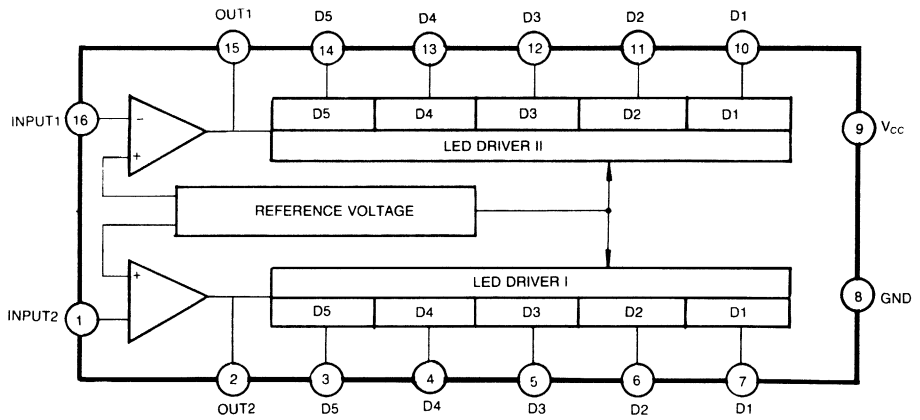


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
D Terminal Output Current	I_D	30	mA
Power Dissipation	P_D	600	mW
Operating Temperature	T_{OPR}	−20 ~ +70	°C
Storage Temperature	T_{STG}	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(T_a = 25°C, V_{CC} = 12V, f = 1KHz, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CCQ}	V_I = 0		4		mA
D Terminal ON Voltage	V_{ON}	I_O = 20mA		1.5		V
D Terminal Leakage Current	$I_{O(LKG)}$	V_I = 0			50	μA
Voltage Gain (Closed Loop)	G_V			13.4		dB
Comparator ON Level	$V_{CL(ON)1}$	G_V = 13.4dB	−1	0	1	dB
	$V_{CL(ON)2}$		−4	−3	−2	
	$V_{CL(ON)3}$		−7.5	−6	−4.5	
	$V_{CL(ON)4}$		−13	−11	−9	
	$V_{CL(ON)5}$		−19	−16	−13	
LED ON Level Difference	ΔV_{CL}	$V_{CL(ON)1-5}$-$V_{CL(ON)1-5}$ A_V = 13.4dB	−1	0	1	dB
Input Impedance of Amp	Z_I			200		KΩ

* Definition of 0dB: when the value of Input voltage is 218mVrms

TYPICAL APPLICATIONS

1. 5-dot dual application

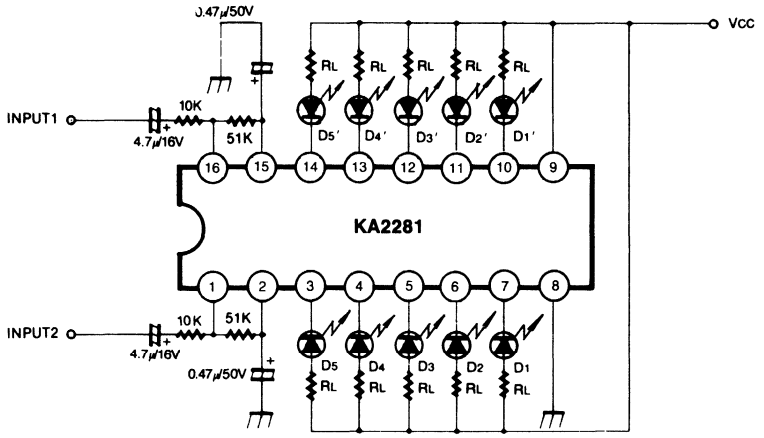


Fig. 2

2. 10-dot mono application

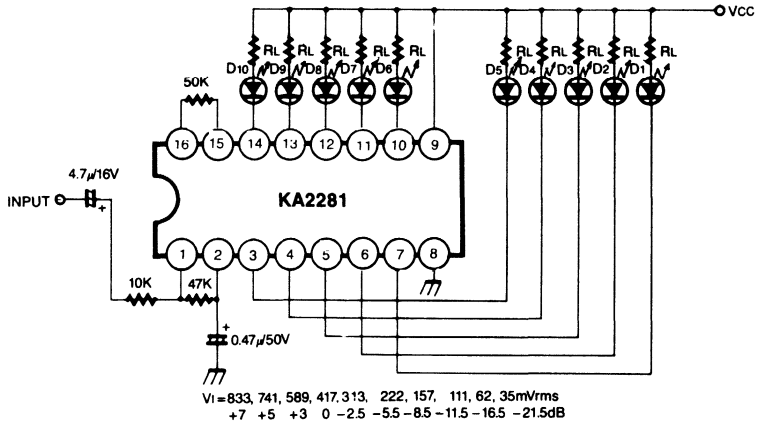
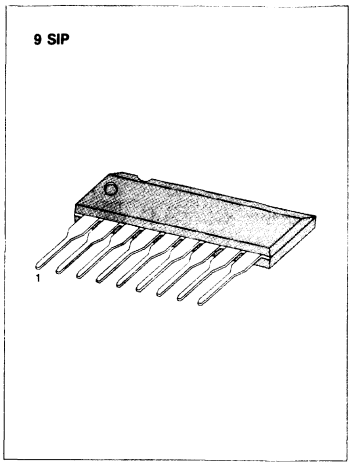


Fig. 3

5-DOT DUAL LED LEVEL METER DRIVER

The KA2284/KA2285 are a monolithic integrated circuits designed for 5-dot LED level meter drivers with a built-in rectifying amplifier; it is suitable for AC/DC level meters such as VU meters or signal meters.



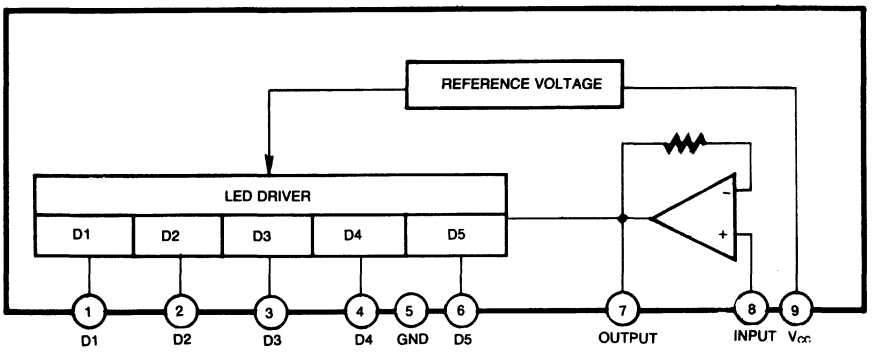
FEATURES

- **High gain rectifying amplifier included (G_V = 26dB).**
- **Low radiation noise when LED turns on.**
- **Logarithmic indicator for 5-dot LED of bar type. (−10, −5, 0, 3, 6dB)**
- **Constant current output.**
  KA2284: I_o = 15mA Typ.
  KA2285: I_o = 7mA Typ.
- **Wide operating supply voltage range: V_{CC} = 3.5V ~ 16V**
- **Minimum number of external parts required.**

ORDERING INFORMATION

Device	Package	Operating Temperature	I_D
KA2284	9 SIP	−20°C ~ +80°C	15 mA
KA2285			7 mA

BLOCK DIAGRAM



*Capacitor to be omitted when used as a DC input signal meter

Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	18	V
Amp Input Voltage	$V_{I(8-5)}$	−0.5 ~ V_{CC}	V
Pin 7 Voltage	V_{7-5}	6	V
D Terminal Output Voltage	V_D	18	V
Circuit Current	I_{CC}	12	mA
D Terminal Output Current	I_D	20	mA
Power Dissipation	P_D	1100	mW
Operating Temperature	T_{OPR}	−20 ~ +80	°C
Storage Temperature	T_{STG}	−40 ~ +125	°C

−11mW/°C is decreased at higher temperature than T_a = 25°C.

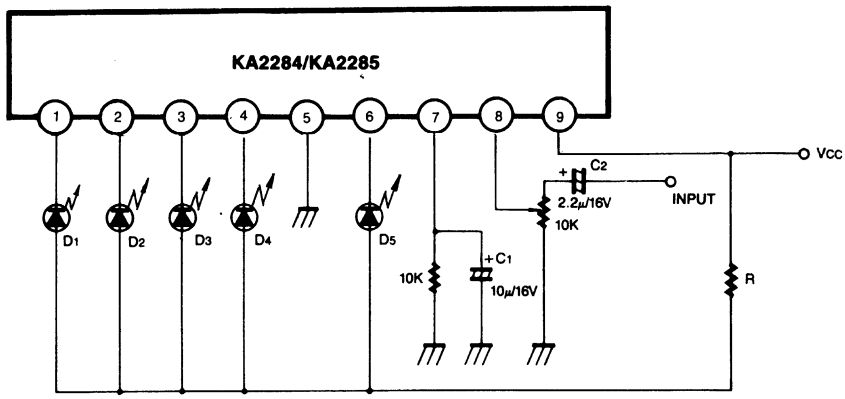
ELECTRICAL CHARACTERISTICS

(T_a = 25°C, V_{CC} = 6V, f = 1KHz, unless otherwise specified)

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit
Circuit Current		I_{CCQ}	V_i = 0V		6	8.5	mA
D Output Current	KA2284	I_O	V_i = 0.15V	11	15	18.5	mA
	KA2285			5	7	9.5	
Input Bias Current		I_{BIAS}		−1		0	μA
Amp Gain		G_V	V_i = 0.1V	24	26	28	dB
Comparator ON Level	$V_{CL(ON)}$	$V_{CL(ON)1}$		−12	−10	−8	dB
		$V_{CL(ON)2}$		−6	−5	−4	
		$V_{CL(ON)3}$			0		
		$V_{CL(ON)4}$		2.5	3	3.5	
		$V_{CL(ON)5}$		5	6	7	

* Definition of 0dB: input voltage level when $V_{CL(ON)3}$ turn ON. (50mV)

TEST CIRCUIT



C2: AC in, 2.2μ is used.
DC in, 2.2μ is shorted

Fig. 2

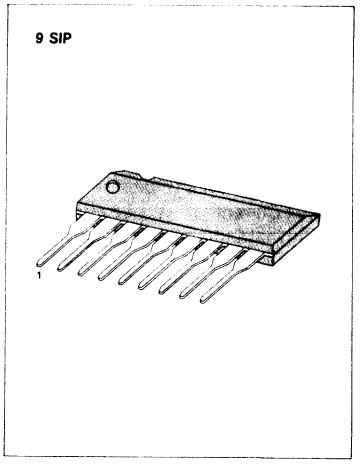
The recommended value of R at T_a (max)=60°C.

V_{CC} (V)	8 ~ 12	10 ~ 14	12 ~ 16
R (Ω)	47	68	91

By changing the time constant C_1 and C_2, the response, attack and release time, may be varied. In the above application conditions, power dissipation may be operated at higher levels than the absolute maximum ratings. The wattage of R is to be determined by the total LED current and R value recommended by the R table.

5-DOT LED LINEAR LEVEL METER DRIVER

The KA2287 are a monolithic integrated circuit designed for 5-dot LED level meter drivers with a built-in rectifying a amplifier, it is suitable for AC/DC level meters such as VU meters or signal meters.



FEATURES

- **High gain rectifying amplifier included (G_V = 26dB).**
- **Low radiation noise when LED turns on.**
- **Linear indicator for 5-dot LED of bar type. (0.33, 0.67, 1, 1.33, 1.67)**
- **Constant current output. KA2287: I_o =15mA Typ.**
- **Wide operating supply voltage range: V_{CC} = 3.5V ~ 16V**
- **Minimum number of external parts required.**

ORDERING INFORMATION

Device	Package	Operating Temperature	I_D
KA2287	9 SIP	-20°C ~ +80°C	7 mA
			15 mA

BLOCK DIAGRAM

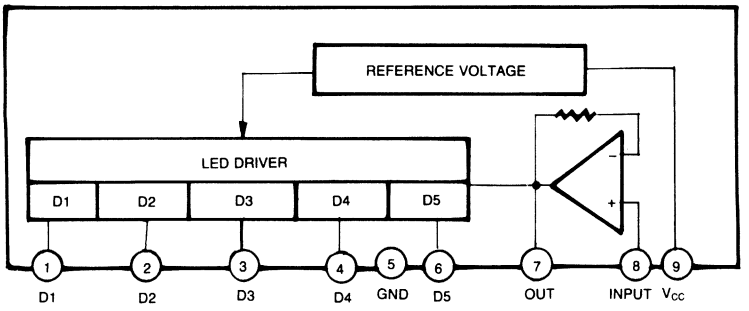


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	18	V
Amp Input Voltage	$V_{I(8-5)}$	−0.5 ~ V_{CC}	V
Pin 7 Voltage	V_{7-5}	6	V
D Terminal Output Voltage	V_D	18	V
Circuit Current	I_{CC}	12	mA
D Terminal Output Current	I_D	20	mA
Power Dissipation	P_D	1100	mW
Operating Temperature	T_{OPR}	−20 ~ +80	°C
Storage Temperature	T_{STG}	−40 ~ +125	°C

−11mW/°C is decreased at higher temperature than T_a = 25°C.

ELECTRICAL CHARACTERISTICS

(T_a = 25°C, V_{CC} = 6V, f = 1KHz, unless otherwise specified)

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current		I_{CCQ}	V_I = 0V		6	8.5	mA
D Output Current		I_O	V_I = 0.15V	11	15	18.5	mA
Input Bias Current		I_{BIAS}		−1		0	μA
Amp Gain		G_V	V_I = 0.1V	24	26	28	dB
Comparator On Level	$V_{CL(ON)}$	$V_{CL(ON)1}$		0.28	0.33	0.40	V_3
		$V_{CL(ON)2}$		0.59	0.67	0.75	
		$V_{CL(ON)3}$			1		
		$V_{CL(ON)4}$		1.25	1.33	1.42	
		$V_{CL(ON)5}$		1.48	1.67	1.87	

* Definition of 1; Pin 3 voltage when $V_{CL(ON)3}$ turn on. (65mV)

TEST CIRCUIT

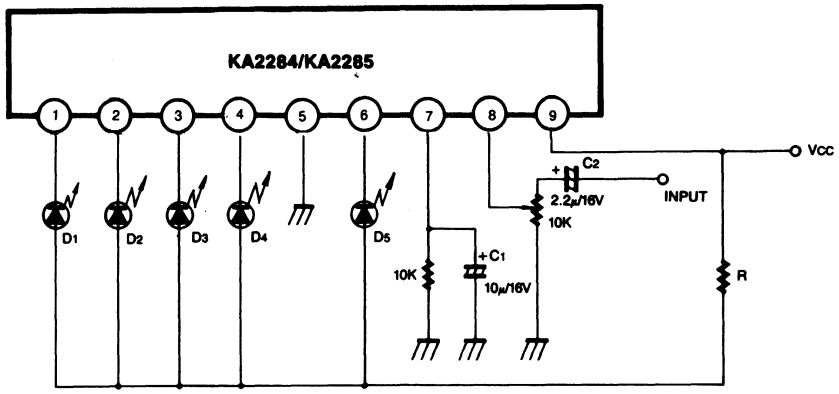


Fig. 2

C2: AC in, 2.2μ is used.
DC in, 2.2μ is shorted

The recommended value of R at T_a (max)=60°C.

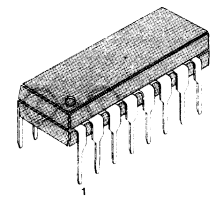
V_{CC} (V)	8 ~ 12	10 ~ 14	12 ~ 16
R (Ω)	47	68	91

By changing the time constant C_1 and C_2, the response, attack and release time, may be varied. In the above application conditions, power dissipation may be operated at higher levels than the absolute maximum ratings. The wattage of R is to be determined by the total LED current and R value recommended by the R table.

7-DOT LED LEVEL METER DRIVER

The KA2288 is a monolithic integrated circuit consisting of 7-dot LED level meter drivers. The KA2288 employs a low noise comparator which provides 10dB lower noise in the LW, MW band than the previously mentioned LED drivers.

16 DIP



FEATURES

- **LED current can be set by an external resistor**
- **Internal detection amplifier**
- **Internal voltage regulator**
- **Constant current output**
- **Fitted with a signal detect output pin**
- **VU meter scale**

BLOCK DIAGRAM

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2288	16 DIP	−20°C ~ +70°C

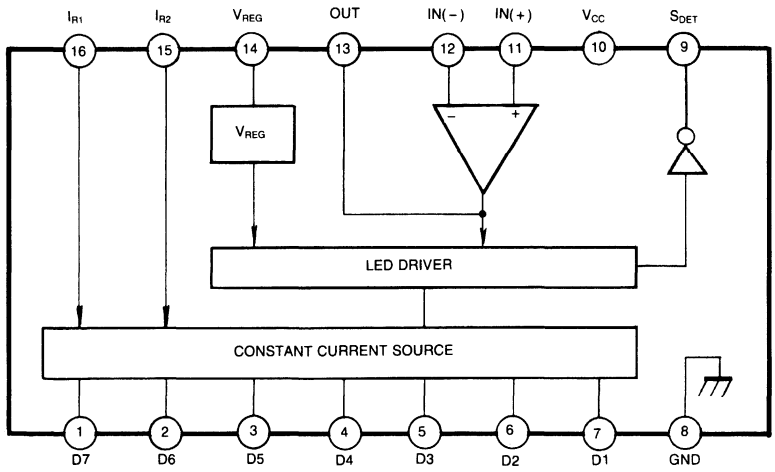


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	18	V
Amp Input Voltage	V_I	0 ~ V_{CC}	V
D Terminal Output Current	I_D	30	mA
D Terminal Output Voltage	V_D	V_{CC}	V
Power Dissipation	P_D	650	mW
Operating Temperature	T_{OPR}	−20 ~ +70	°C
Storage Temperature	T_{STG}	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CCQ}	R_1 = 4.7K, R_2 = ∞		8	12	mA
Input Bias Current	I_{BIAS}			−200	−800	nA
Input Offset Voltage	V_{IO}			2	10	mV
Amp Gain	G_V	Open loop	50	70		dB
Reference Voltage	V_{REF}	V_{CC} = 6.2 ~ 16V, R_L = 10K	2.4	2.6	2.9	V
Signal Detection Output High Level	$V_{OH\ (DET)}$	R_L = 10K	10	10.3	V	
Output Current 1	I_{O1}	R_1 = 10K, R_2 = ∞	4.2	7.1	10.0	mA
Outut Current 2*	I_{O2}	R_1 = 10K, R_2 = 22K	6.3	10.6	15.0	mA
Output Leakage Current	I_{LEK}	R_1 = 4.7K, R_2 = ∞			20	μA
Comparator On Level	$V_{CL\ (ON)\ 1}$	V_{CC} = 6.2V ~ 16V	−22	−20	−18	dB
	$V_{CL\ (ON)\ 2}$		−11	−10	−9	
	$V_{CL\ (ON)\ 3}$		−6.5	−6	−5.5	
	$V_{CL\ (ON)\ 4}$		−3.5	−3	−2.5	
	$V_{CL\ (ON)\ 5}$			0		
	$V_{CL\ (ON)\ 6}$		+2.5	+3	+3.5	
	$V_{CL\ (ON)\ 7}$		+5	+6	+7	
0dB Level	$V_{CL\ (ON)\ 5}$	V_{CC} = 6.2 ~ 16V, V_{REF} = 2.4 ~ 2.9V	1.2	1.3	1.45	V

* : Applied pin: 4, 5, 6, 7

TEST CIRCUIT

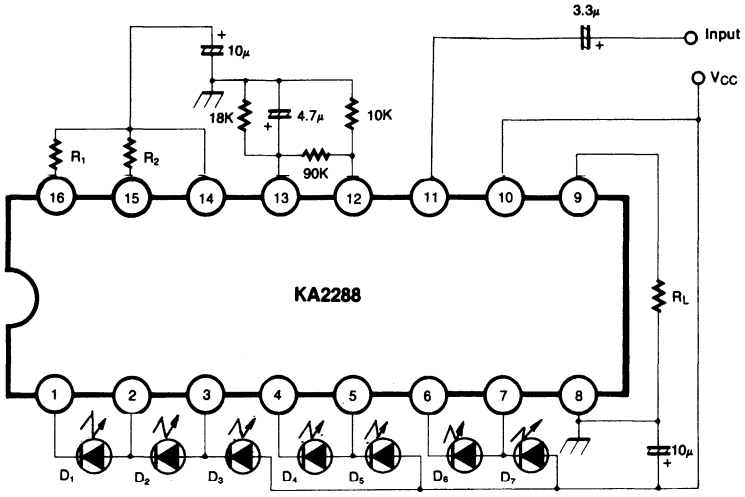
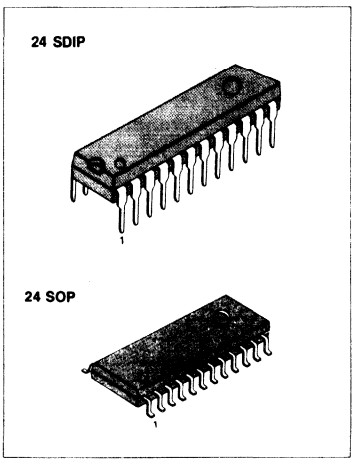


Fig. 2

AM/FM TUNER + MPX

The KA2292 is a monolithic integrated circuit which consists of a 3V one chip tuner and FM multiplex for AM/FM radios and headphone radios.



FUNCTIONS

* FM Stage : RF/IF/AF amp, Quadrature Detector, MIX, OSC, Tuning Indicator.
* AM Stage : RF/IF/AF amp, Detector, MIX, OSC, AGC, Tuning Indicator.
* MPX Stage : PLL amp, Decoder, Flip Flop, VCO Stop, Phase Detector, Stereo Indicator.

FEATURES

- **3V one chip tuner with built-in FM Multiplex**
- **No AM detect coil, IF coupling capacitor, FM IF by-pass capacitor needed.**
- **Built-in tuning indicator function.**
- **Built-in AM/FM selection switch.**
- **Minimum number of external parts required.**
- **Wide operating voltage range: V_{CC} = 1.8V ~ 7V**
- **Low distortion (FM IF: 0.4%, AM IF: 1%, 0.2% (Typ)).**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2292	24 SDIP	−20°C ~ +75°C
KA2292D	24 SOP	

BLOCK DIAGRAM

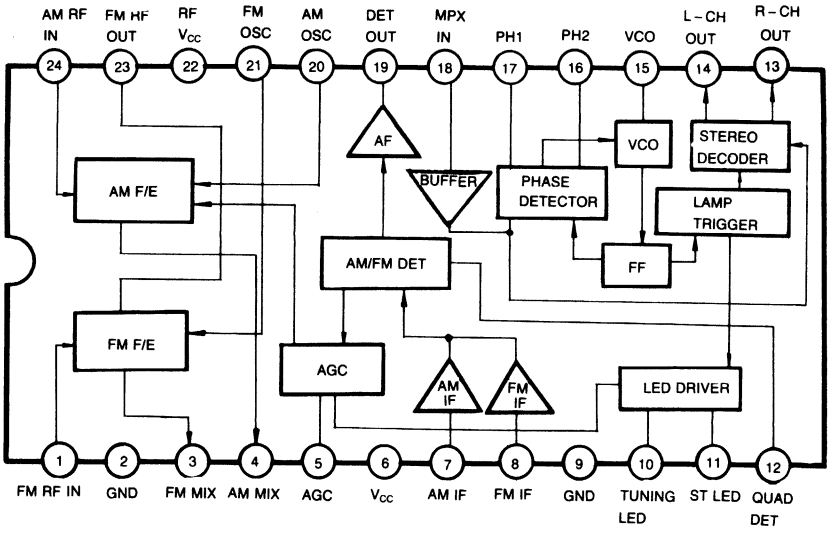


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	8	V
Power Dissipation	P_D	1200	mW
Operating Temperature	T_{OPR}	−20 ~ +75	°C
Storage Temperature	T_{STG}	−55 ~ +150	°C
LED Drive Voltage	V_{DR}	10	V
LED Drive Current	I_{DR}	10	mA

ELECTRICAL CHARACTERISTICS

(T_a = 25°C, V_{CC} = 3V, unless otherwise specified)
FM F/E : f = 98MHz, fm = 1KHz, △f = 22.5KHz AM : f = 1MHz, fm = 1KHz, 30% Mod
FM IF : f = 10, 7MHz, fm = 1KHz, △f = 22.5KHz MPX : f = 1KHz, L + R = 90%, P = 10%, V_I = 150mV

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit	Test Circuit
Quiescent Circuit Current		I_{CCQ1}	FM, V_I = 0	8.4	13.2	20.0	mA	1
		I_{CCQ2}	AM, V_I = 0	4.4	8.4	13.4	mA	1
F/E	−3dB Limiting Sensitivity	$V_{I\,(LIM)\,1}$	V_O = −3dB		10		dBμ	1
	Oscillation Voltage	V_{OSC}	fosc = 98MHz	40	70	110	mV	2
FM IF	−3dB Limiting Sensitivity	$V_{I\,(LIM)\,2}$	V_O = −3dB	40	46	53	dBμ	1
	Detector Output Voltage	$V_{O\,(DET)\,1}$	V_I = 80dBμ	55	80	110	mV	1
	Signal to Noise Ratio	S/N_1	V_I = 80dBμ	60	70		dB	1
	Total Harmonic Distortion	THD_1	V_I = 80dBμ		0.4	1	%	1
	AM Rejection Ratio	AMR	V_I = 80dBμ	22	32		dB	1
	Tuning Indication Voltage	V_{LI}	I_{LED} = 1mA	45	51	56	dBμ	1
AM IF	Voltage Gain	G_{V1}	V_I = 26dBμ	40	70	110	mV	1
	Detector Output Voltage	$V_{O\,(DET)\,2}$	V_I = 60dBμ	55	80	110	mV	1
	Signal to Noise Ratio	S/N_2	V_I = 60dBμ	32	42		dB	1
	Total Harmonic Distortion	THD_2	V_I = 60dBμ		1	2	%	1
	Tuning Indication Voltage	V_{L2}	I_{LED} = 1mA	20	25	30	dBμ	1
MPX	Maximum Input Voltage	$V_{I\,(MAX)}$	Stereo, THD = 3%	250	350		mV	1
	Channel Separation	CS_1	Stereo, f = 100Hz	32	42		dB	1
		CS_2	Stereo, f = 1KHz	32	42		dB	1
		CS_3	Stereo, f = 10KHz	32	42		dB	1
	Total Harmonic Distortion	THD_3	Mono		0.2	1	%	1
		THD_4	Stereo		0.2	1	%	1
	Voltage Gain	G_{V2}	Mono	−5	−3	−1	dB	1
	Channel Balance	CB	Mono	−2	0	2	dB	1
	Lamp on Level	$VL_{(ON)}$	Pilot only		8	16	mV	1
		$VL_{(OFF)}$	Pilot only	2	6		mV	1
	Lamp Hysteresis	HY			2		mV	1
	Capture Range	CR	Pilot only	±1	±3	±5	%	1
	Signal to Noise Ratio	S/N_3	Mono	60	70		dB	1

TEST CIRCUIT 1

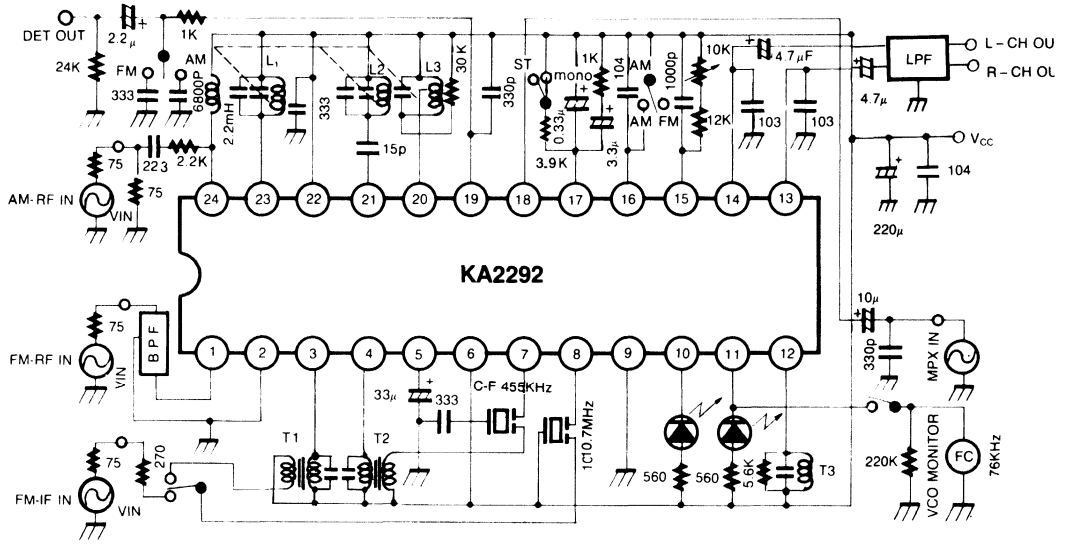


Fig. 2

*POLYESTER FILM CAPACITOR

TEST CIRCUIT 2

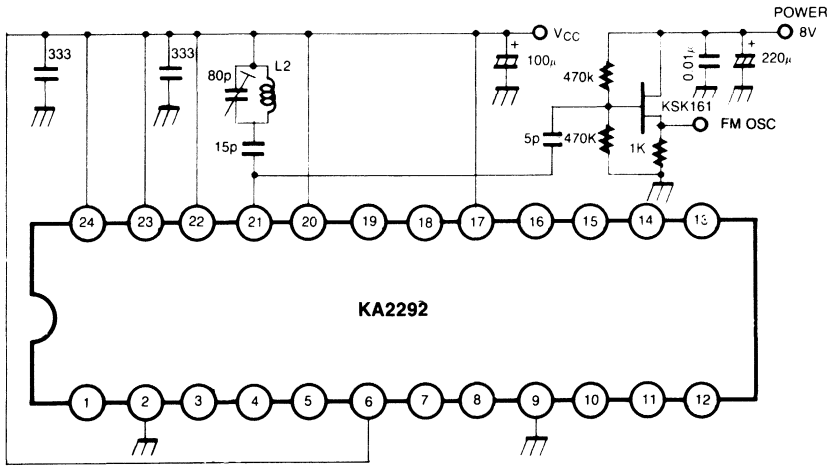
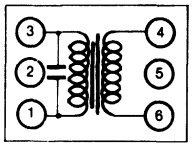


Fig. 3

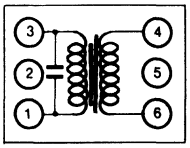
COIL SPECIFICATION

T1 FM IFT (MIX OUT)



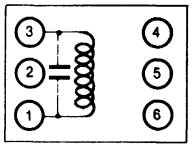
C_O(pF)	f (MHz)	Q_O	TURNS			
1-3			1-3	4-6		KOREA TOKO
75	10.7	70(min)	11	2		0.1mmϕ

T2 AM IFT (MIX OUT)



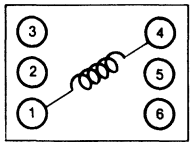
C_O(pF)	f (MHz)	Q_O	TURNS			
1-3			1-3	4-6		KOREA TOKO
180	455	70(min)	180	15		0.08mmϕ

T3 FM IFT (DET)



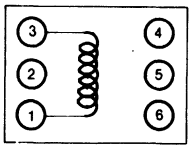
C_O(pF)	f (MHz)	Q_O	TURNS			
1-3			1-3			KOREA TOKO
47	10.7	80(min)	14			0.1mmϕ

L1 FM RF



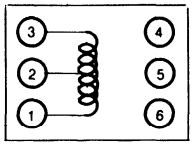
f (MHz)	Q_O	TURNS			
		1-4			
100	100	2½			0.5mmϕ

L2 FM OSC



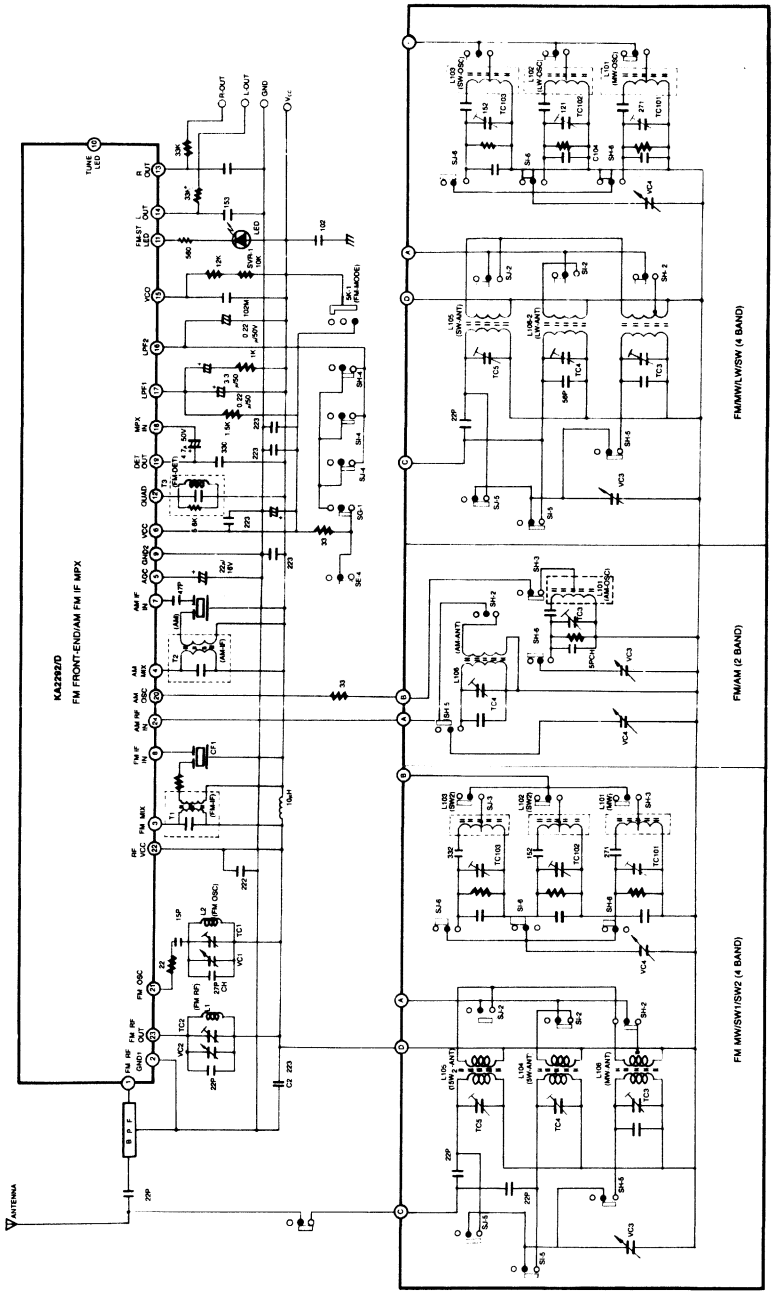
f (MHz)	Q_O	TURNS			
		1-3			
100	100	2¾			0.5mmϕ

L3 AM OSC



f (KHz)	Q_O	TURNS			L	
		1-2	2-3		(μH)	KOREA TOKO
796	80(min)	13	73		288	0.08mmϕ

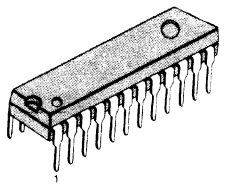
APPLICATION CIRCUIT



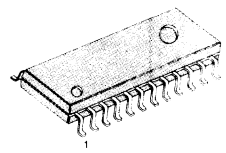
FM/AM TUNER + MPX

The KA2293 is a monolithic integrated circuit which consists of a one chip tuner and no adjustment FM multiplex for AM/FM radios and headphone radios.

24 SDIP



24 SOP



FEATURES

- **One-chip tuner with built-in FM multiplex.**
- **No adjustment for FM detector and VCO.**
- **No AM detect coil, IF coupling capacitor, FM IF bypass capacitor needed.**
- **Built-in AM/FM selection switch.**
- **Minimum number of external parts required.**
- **Wide operating voltage range: V_{CC} = 1.8V ~ 7V**
- **Low distortion (FM IF: 0.4%, AM IF: 1%, MPX: 0.2% (Typ)).**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2293	24 SDIP	-20°C ~ +75°C
KA2293D	24 SOP	

BLOCK DIAGRAM

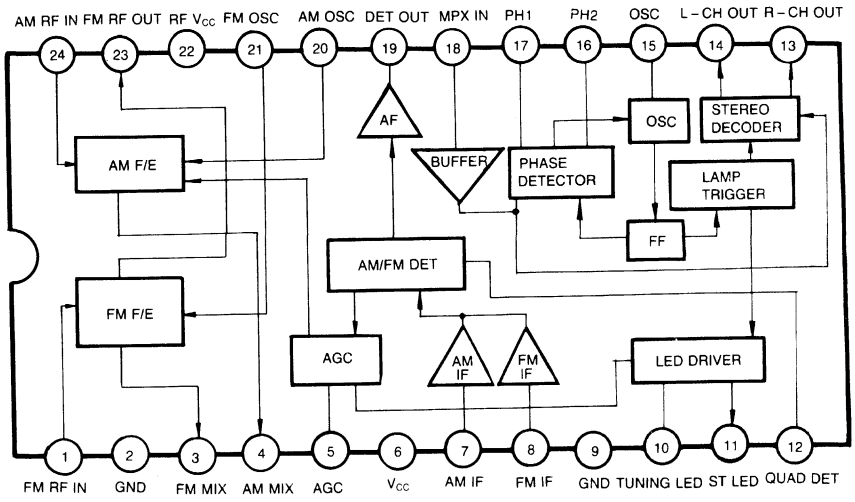


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	8	V
Power Dissipation	P_D	1200	mW
Operating Temperature	T_{OPR}	−20 ~ +75	°C
Storage Temperature	T_{STG}	−55 ~ +150	°C
LED Drive Voltage	V_{DR}	10	V
LED Drive Current	I_{DR}	10	mA

ELECTRICAL CHARACTERISTICS

(T_a = 25°C, V_{CC} = 3V, unless otherwise specified)
FM F/E : f = 98MHz, fm = 1KHz, △f = 22.5KHz
FM IF : f = 10, 7MHz, fm = 1KHz, △f = 22.5KHz
AM : f = 1MHz, fm = 1KHz, 30% Mod
MPX : f = 1KHz, L + R = 90%, P = 10%, V_I = 150mV

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit	Test Circuit
Quiescent Circuit Current		I_{CCQ1}	FM, V_I = 0	10	14	18	mA	1
		I_{CCQ2}	AM, V_I = 0	3.5	6.0	9	mA	1
F/E	−3dB Limiting Sensitivity	$V_{I(LIM)1}$	V_O = −3dB	10	14	18	dBμ	1
	Oscillation Voltage	V_{OSC}	f_{OSC} = 72.3MHz	70	105	140	mV	2
FM IF	−3dB Limiting Sensitivity	$V_{I(LIM)2}$	V_O = −3dB	39	44	49	dBμ	1
	Detector Output Voltage	V_{O1}	V_I = 80dBμ	55	80	110	mV	1
	Signal to Noise Ratio	S/N_1	V_I = 80dBμ	60	70		dB	1
	Total Harmonic Distortion	THD_1	V_I = 80dBμ		0.4	1	%	1
	AM Rejection Ratio	AMR	V_I = 80dBμ	40	50		dB	1
	Tuning Indication Voltage	V_{L1}	I_{LED} = 1mA	43	48	53	dBμ	1
AM IF	Voltage Gain	G_{V1}	V_I = 23dBμ	20	40	80	mV	1
	Detector Output Voltage	$V_{O(DET)2}$	V_I = 60dBμ	50	60	100	mV	1
	Signal to Noise Ratio	S/N_2	V_I = 60dBμ	34	44		dB	1
	Total Harmonic Distortion	THD_2	V_I = 60dBμ		1	2	%	1
	Tuning Indication Voltage	V_{L2}	I_{LED} = 1mA	19	24	30	dBμ	1
MPX	Maximum Input Voltage	$V_{I(MAX)}$	Stereo, THD = 3%	250	350		mV	1
	Channel Separation	CS_1	Stereo, f = 100Hz	35	42		dB	1
		CS_2	Stereo, f = 1KHz	35	42		dB	1
		CS_3	Stereo, f = 10KHz	35	42		dB	1
	Total Harmonic Distortion	THD_3	Mono		0.2	1	%	1
		THD_4	Stereo		0.2	1	%	1
	Voltage Gain	G_{V2}	Mono	−5	−3	−1	dB	1
	Channel Balance	CB	Mono	−2	0	2	dB	1
	Lamp on Level	$V_{L(ON)}$	Pilot only		8	16	mV	1
		$V_{L(OFF)}$	Pilot only	2	6		mV	1
	Lamp Hysteresis	HY			2		mV	1
	Capture Range	CR	Pilot only		±3		%	1
	Signal to Noise Ratio	S/N_3	Mono	60	70		dB	1

TEST CIRCUIT 1

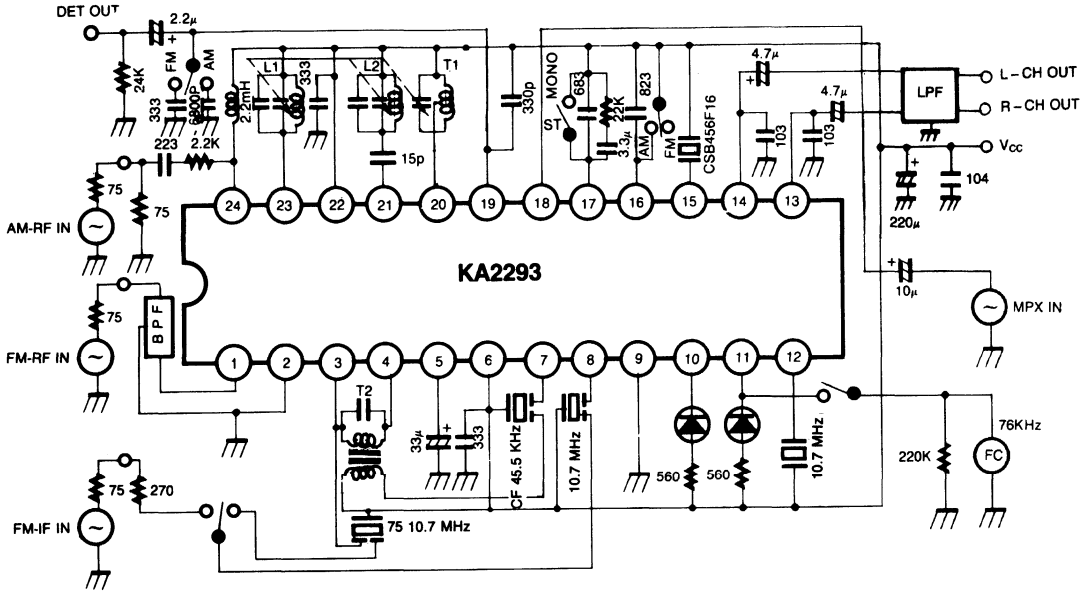


Fig. 2

TEST CIRCUIT 2

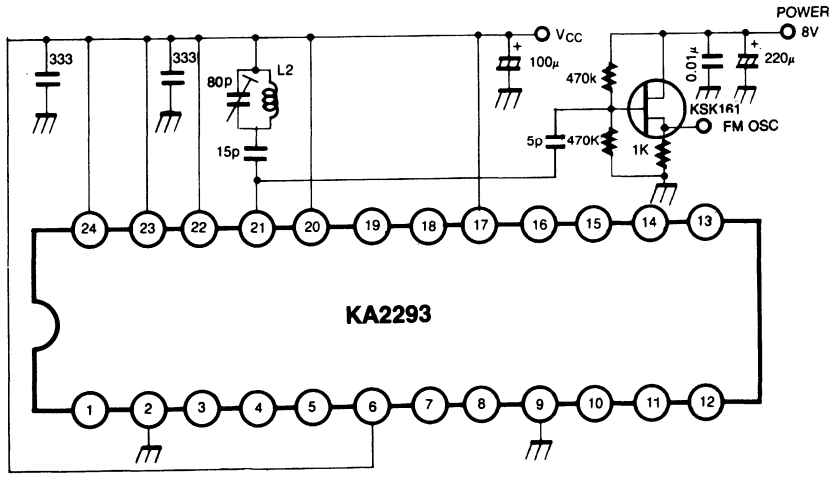
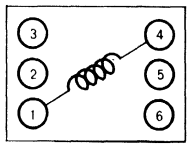


Fig. 3

COIL SPECIFICATION

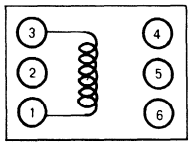
L1 FM RF



f (MHz)	Qo	TURNS 1-4		
100	100	2½		

0.5mmϕ

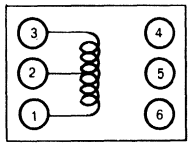
L2 FM OSC



f (MHz)	Qo	TURNS 1-3		
100	100	2¾		

0.5mmϕ

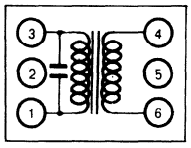
T1 AM OSC



f (MHz)	Qo	TURNS 1-2	2-3		L (μH)
796	115	13	73		288

KOREA TOKO
0.08mmϕ

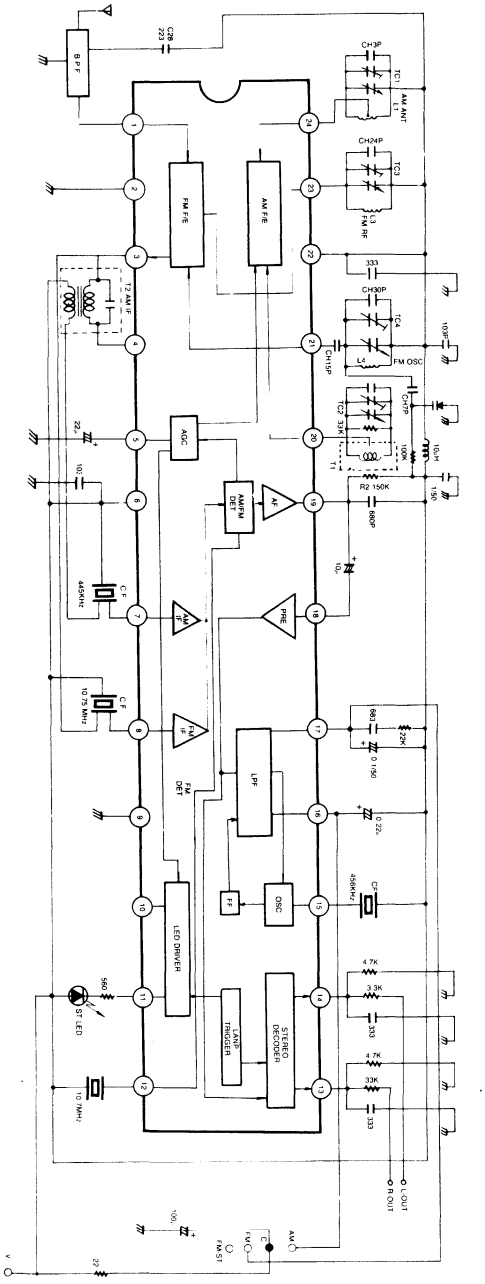
T2 AM IFT (MIX OUT)



Co(pF) 1-3	f (KHz)	Qo	TURNS 1-3	4-6	
180	455	120	180	15	

KOREA TOKO
0.08mmϕ

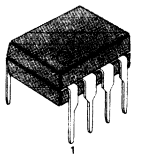
APPLICATION CIRCUIT



DC MOTOR SPEED CONTROLLER

The KA2401 is a monolithic integrated circuit designed for DC motor speed controllers.

8 DIP



FEATURES

- **Suitable for DC motor speed controllers of cassette tape recorders and radio cassettes.**
- **Excellent stability of each characteristics against ambient temperature.**
- **Low quiescent current (0.8mA; Typ).**
- **Low reference voltage.**
- **Wide operating supply voltage range (4V ~ 12V).**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2401	8 DIP	- 20°C ~ + 70°C

BLOCK DIAGRAM

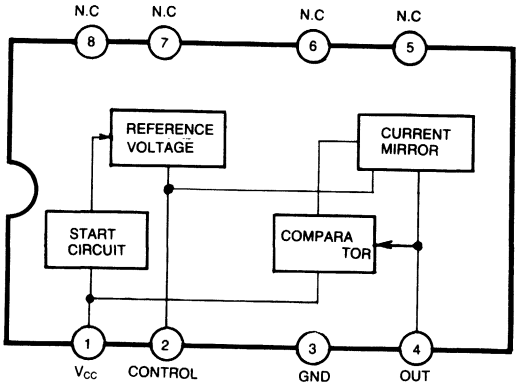


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Circuit Current	I_4	*2	A
Power Dissipation	P_D	600	mW
Operating Temperature	T_{OPR}	-20 ~ +70	°C
Storage Temperature	T_{STG}	-40 ~ +125	°C

*t<5 sec

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 6V, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Test Fig
Reference Voltage	V_{REF}	I_4 = 10mA	1.10	1.27	1.40	V	2
Quiescent Circuit Current	I_{CCQ}	R_M = 180Ω	0.5	0.8	1.2	mA	5
Current Coefficient	K	Rm_1 = 44Ω, Rm_2 = 33Ω	18	20	22		3
Saturation Voltage	$V_{4\,(SAT)}$	V_{CC} = 4.2V, Rm = 4.4Ω		1.5	20	V	4
Voltage Characteristic of Shunt-Current Coefficient	$\frac{\Delta K}{K}/\Delta V_{CC}$	I_4 = 100mA, V_{CC} = 4 ~ 12V		0.4		%/V	3
Voltage Characteristic of Reference Voltage	$\frac{\Delta V_{REF}}{V_{REF}}/\Delta V_{CC}$	I_4 = 100mA, V_{CC} = 4 ~ 12V		0.6		%/V	2
Current Characteristic of Current Coefficient	$\frac{\Delta K}{K}/\Delta I_4$	I_4 = 30 ~ 200mA		-0.02		%/mA	3
Current Characteristic of Reference Voltage	$\frac{\Delta V_{REF}}{V_{REF}}/\Delta I_4$	I_4 = 30 ~ 200mA		-0.02		%/mA	2
Temperature Characteristic of Current Coefficient	$\frac{\Delta K}{K}/\Delta T_a$	I_4 = 100mA T_a = -20 ~ +75°C		0.01		%/°C	3
Temperature Characteristic of Reference Voltage	$\frac{\Delta V_{REF}}{V_{REF}}/\Delta T_a$	I_4 = 100mA T_a = -20 ~ +75°C		0.01		%/°C	2

TEST CIRCUIT 1

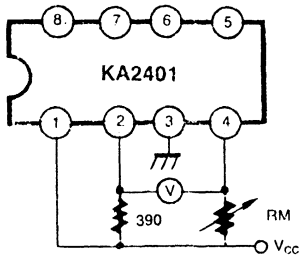


Fig. 2

$$Vref, \frac{\Delta V_{REF}}{V_{REF}}/\Delta Vcc, \frac{\Delta V_{REF}}{V_{REF}}/\Delta I_4, \frac{\Delta V_{REF}}{V_{REF}}/\Delta Ta$$

TEST CIRCUIT 2

Current Coefficient

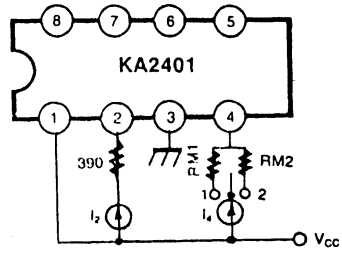


Fig. 3

$$K, \frac{\Delta K}{K}/\Delta Vcc, \quad \frac{\Delta K}{K}/\Delta I_4, \frac{\Delta K}{K}/\Delta Ta$$

$$K = \frac{I_4\,(SW\,2) - I_4\,(SW\,1)}{I_2\,(SW\,2) - I_2\,(SW\,1)}$$

TEST CIRCUIT 3

Saturation Voltage

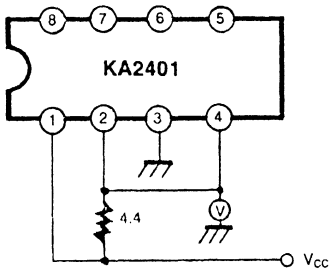


Fig. 4

TEST CIRCUIT 4

Quiescent Circuit Current

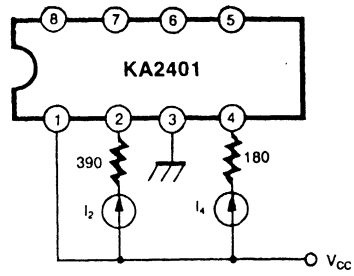
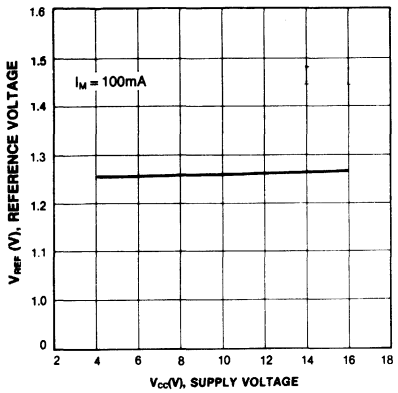
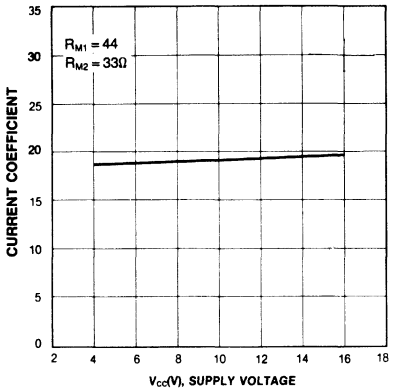


Fig. 5

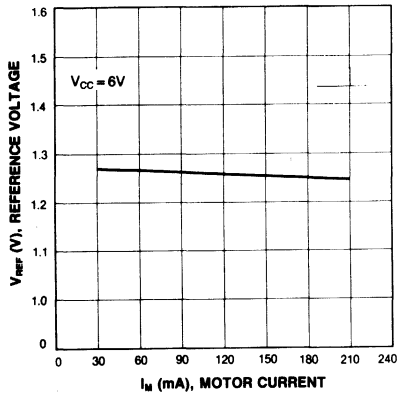
REFERENCE VOLTAGE-SUPPLY VOLTAGE



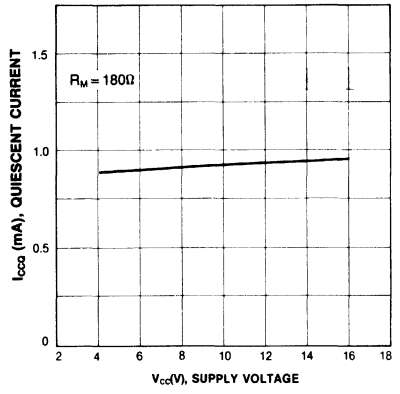
CURRENT COEFFICIENT SUPPLY VOLTAGE



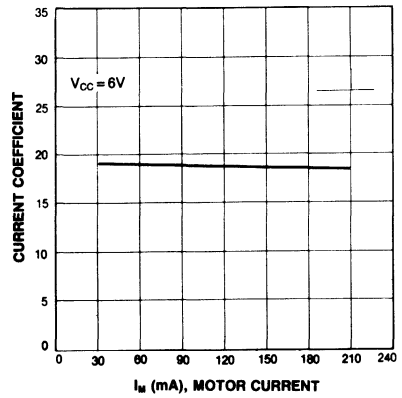
REFERENCE VOLTAGE-MOTOR CURRENT



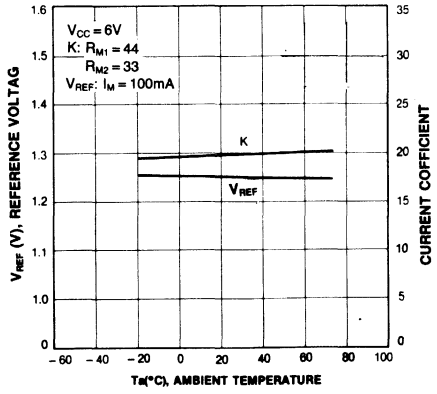
QUIESCENT CURRENT-SUPPLY VOLTAGE

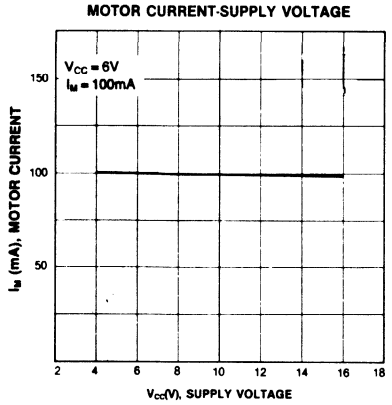


CURRENT COFFICIENT-MOTOR CURRENT



REFERENCE VOLTAGE REFLECTION COEFFICIENT ·AMBIENT TEMPERATURE





APPLICATION CIRCUIT

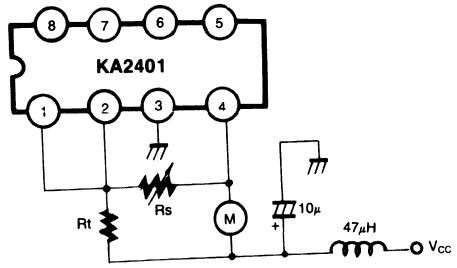
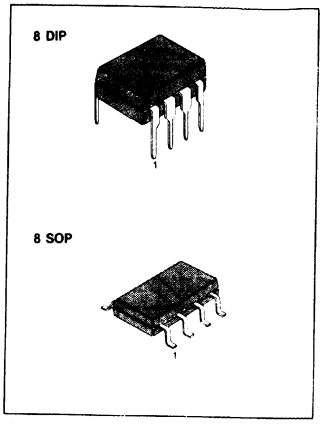


Fig. 6

LOW VOLTAGE DC MOTOR SPEED CONTROLLER



USE

- Speed control or general-purpose low-voltage compact DC motor for microcassette tape recorders, radio cassettes and their equivalents.

FEATURES

- **Operating supply voltage range**
  KA2402: V_{CC} = 1.8V ~ 8V
  KA2402D: V_{CC} = 1.8V ~ 4.5V
- **Capable of making the applicable set compact because of a minimum to adjust speed.**
- **Easy to adjust speed.**
- **Built-in stable low reference power meeting the requirements for 2 speeds.**
- **V_{REF} = 0.2V**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2402	8 DIP	-20°C ~ +80°C
KA2402D	8 SOP	

BLOCK DIAGRAM

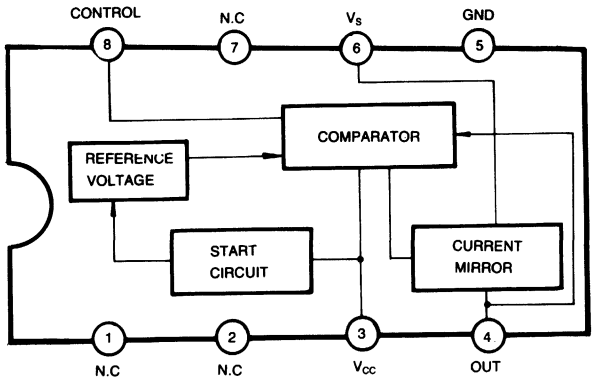


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Maximum Supply Voltage	V_{CC}	10	V
Maximum Motor Current	$I_{M\ (MAX)}$	700	mA
Power Dissipation	P_D	600	mW
Operating Temperature	T_{OPR}	−20 ~ +80	°C
Storage Temperature	T_{STG}	−40 ~ +125	°C

RECOMMENDED OPERATING CONDITIONS (Ta = 25°C)

Characteristic	Symbol	Value		Unit
Supply Voltage	V_{CC}	KA2402	1.8 ~ 8	V
		KA2402D	1.8 ~ 4.5	
Recommended Operating Temperature	T_{OPR}	−20 ~ 60		°C

ELECTRICAL CHARACTERISTICS (Ta = 25°C)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Reference Voltage	V_{REF}	V_{CC} = 3V, I_M = 100mA	0.18	0.2	0.22	V
Circuit Current	I_{CC}	V_{CC} = 3V, I_M = 100mA		2.4	6.0	mA
Current Coefficient	K	V_{CC} = 3V, I_M = 50mA I_M = 100mA	45	50	55	
Saturation Voltage	V_{SAT}	V_{CC} = 3V, I_M = 100mA		0.13	0.3	V
Voltage Characteristic of Reference Voltage	$\frac{\Delta V_{REF}}{V_{REF}} / \Delta V_{CC}$	I_M = 100mA V_{CC} = 1.8 ~ 8V (KA2402) 1.8 ~ 4.5V (KA2402D)		0.1		%/V
Voltage Characteristic of Current Coefficient	$\frac{\Delta K}{K} / \Delta V_{CC}$	I_M = 50, 150mA V_{CC} = 1.8 ~ 8V (KA2402) 1.8 ~ 4.5V (KA2402D)		0.3		%/V
Voltage Characteristic of Reference Voltage	$\frac{\Delta V_{REF}}{V_{REF}} / \Delta I_m$	I_M = 3V I_M = 20 ~ 200mA		0.005		%/mA
Current Characteristic of Current Coefficient	$\frac{\Delta K}{K} / \Delta I_m$	V_{CC} = 3V, I_M = 20, 50mA − 170, 200mA		− 0.07		%/mA
Temperature Characteristic of Reference Voltage	$\frac{\Delta V_{REF}}{V_{REF}} / \Delta T_a$	V_{CC} = 3V, I_M = 100mA T_a = − 20 ~ + 80°C		− 0.008		%/°C
Temperature Characteristic of Current Coefficient	$\frac{\Delta K}{K} / \Delta T_a$	V_{CC} = 3V, I_50m, 150mA ıA T_a = − 20 ~ + 80°C		0.02		%/°C

TEST CIRCUIT

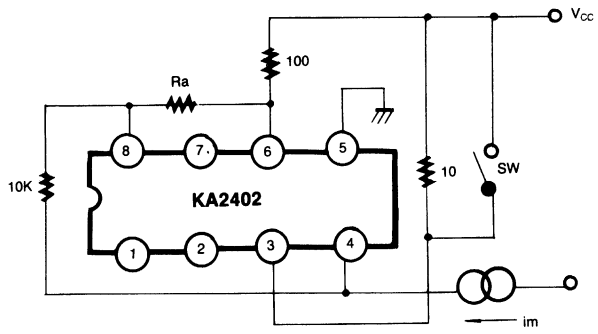


Fig. 2

APPLICATION CIRCUIT

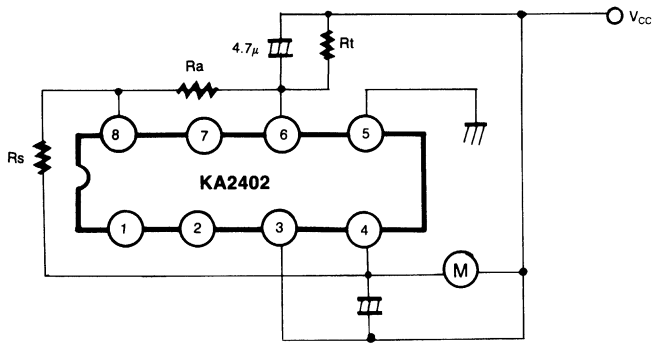
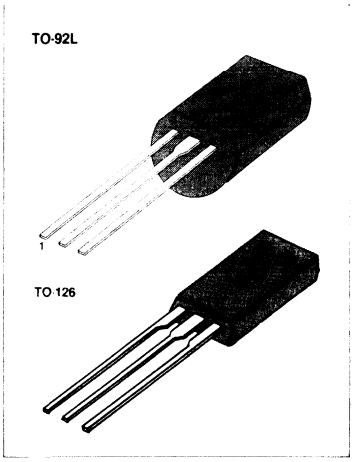


Fig. 3

DC MOTOR SPEED CONTROLLER

The KA2404 is a monolithic integrated circuit designed for DC motor speed controllers.



FEATURES

- **Suitable for DC motor speed controllers of cassette tape recorders and radio cassettes.**
- **Excellent stability of each characteristics against ambient temperature.**
- **High output current.**
- **Low quiescent current (1.3mA: typ).**
- **Low reference voltage.**
- **Wide operating supply voltage range (V_{CC} = 4V ~ 12V)**
- **KA2404A: To-126 PKG type**

EQUIVALENT CIRCUIT BLOCK DIAGRAM

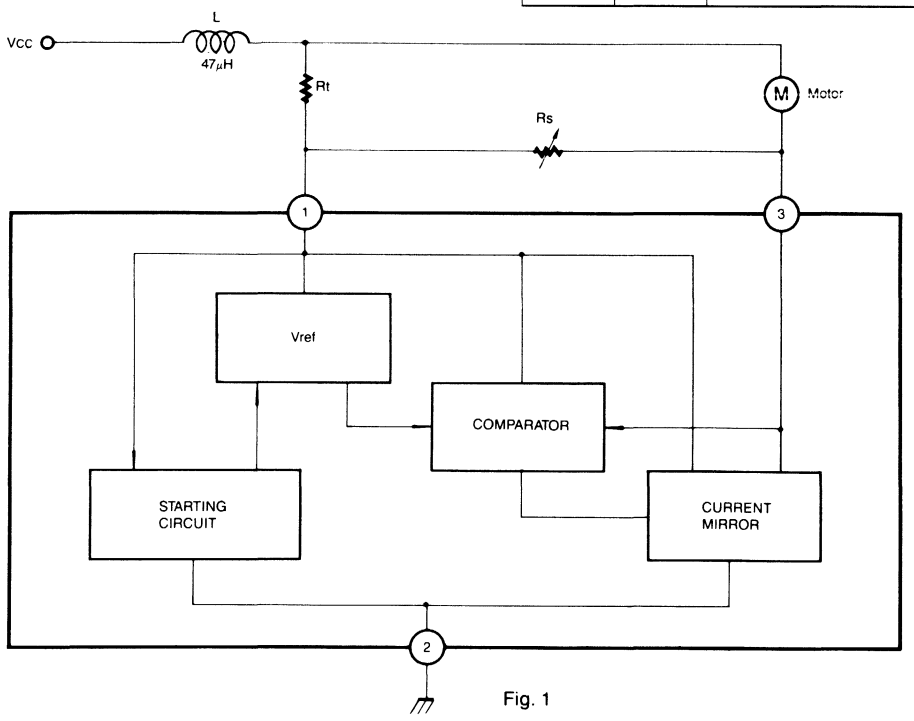


Fig. 1

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2404	TO-92L	-20°C ~ +70°C
KA2404A	TO-126	

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristics	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Circuit Current	I_3	2 (Note 1)	A
Power Dissipation	P_D (TO-92L)	800	mW
(TO-126)	1.3 (Note 2)	W	
Operating Temperature	T_{OPR}	−20 ~ +70	°C
Storage Temperature	T_{STG}	−40 ~ +125	°C

Note 1: 5 > 5 sec
Note 2: Ta = 25°C, with a 100 x 100mm bakelite printed circuit board (35μ Cu leaf)

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 9V, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Fig
Reference Voltage	V_{REF}	I_3 = 10mA	1.10	1.27	1.40	V	2
Quiescent Circuit Current	I_{CCQ}	Rm = 180Ω	0.8	1.3	1.8	mA	4
Current Coefficient	K	Rm_1 = 44Ω Rm_2 = 33Ω	16	18	20		3
Voltage Characteristic of Current Coefficient	$\frac{\Delta K}{K} / \Delta V_{CC}$	I_3 = 100mA V_{CC} = 4 ~ 12V		0.4		%/V	3
Voltage Characteristic of Reference Voltage	$\frac{\Delta V_{REF}}{V_{REF}} / \Delta V_{CC}$	I_3 = 100mA V_{CC} = 4 ~ 12V		0.06		%/V	2
Current Characteristic of Current Coefficient	$\frac{\Delta K}{K} / \Delta I_3$	I_3 = 30 ~ 200mA		−0.02		%/mA	3
Current Characteristic of Reference Voltage	$\frac{\Delta V_{REF}}{V_{REF}} / \Delta I_3$	I_3 = 30 ~ 200mA		−0.02		%/mA	2
Temperature Characteristics of Current Coefficient	$\frac{\Delta K}{K} / \Delta T_a$	I_3 = 100mA T_a = −20 ~ +75°C		0.01		%/°C	3
Temperature Characteristics of Reference Voltage	$\frac{\Delta V_{REF}}{V_{REF}} / \Delta T_a$	I_3 = 100mA T_a = −20 ~ +75°C		0.01		%/°C	2

TEST CIRCUIT 1

Reference Voltage

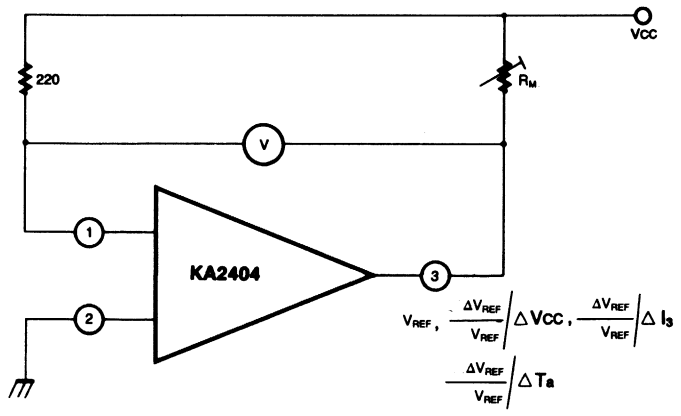


Fig. 2

TEST CIRCUIT 2

Current Coefficient

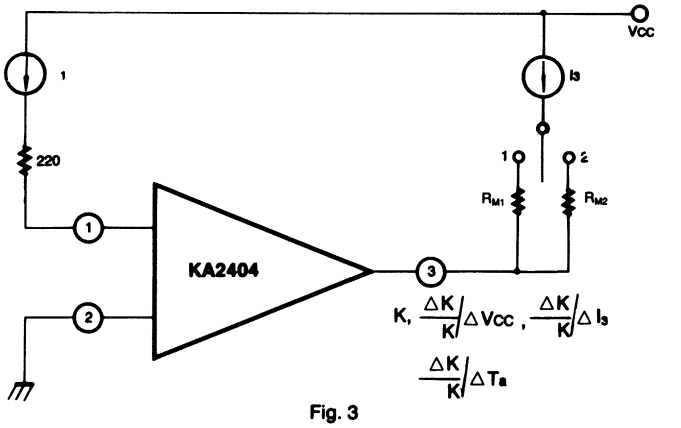


Fig. 3

$$K = \frac{I_3\ (SW\ 2) - (SW\ 1)}{I_1\ (SW\ 2) - (SW\ 1)}$$

TEST CIRCUIT 3

Quiescent Circuit Current

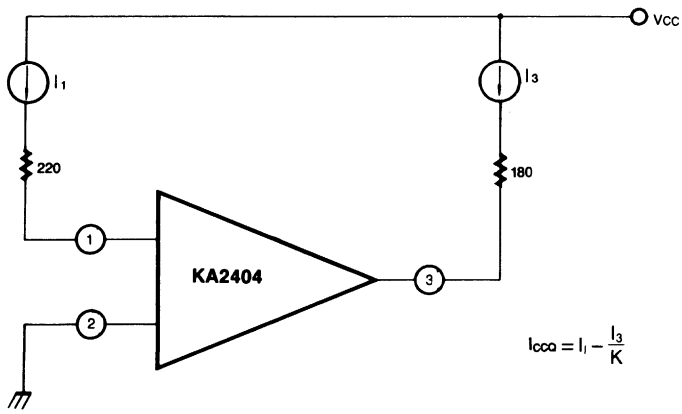
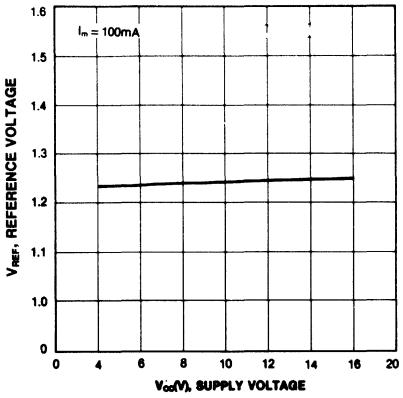
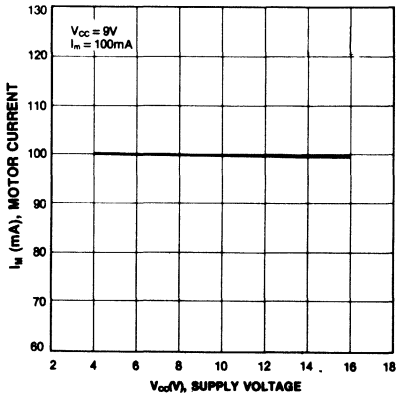


Fig. 4

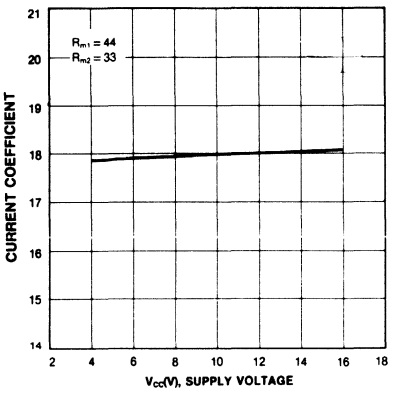
REFERENCE VOLTAGE-SUPPLY VOLTAGE



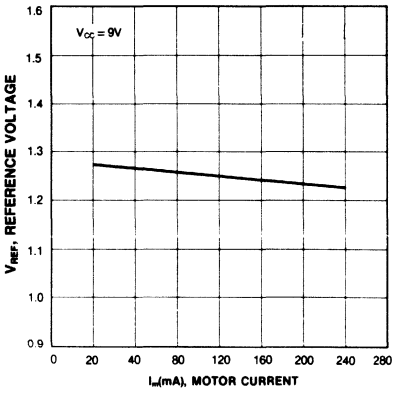
MOTOR CURRENT-SUPPLY VOLTAGE



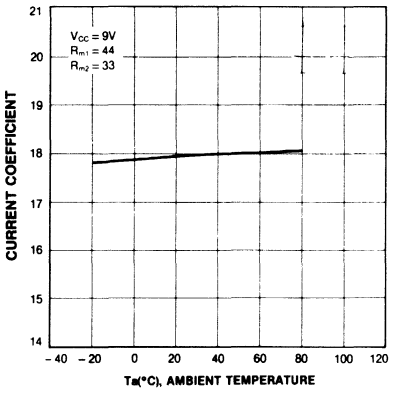
CURRENT COEFFICIENT-SUPPLY VOLTAGE



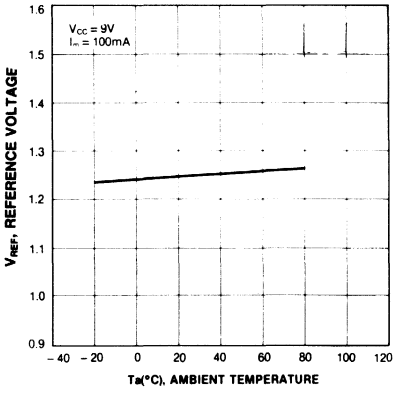
REFERENCE VOLTAGE-MOTOR CURRENT



CURRENT COEFFICIENT-AMBIENT TEMPERATURE

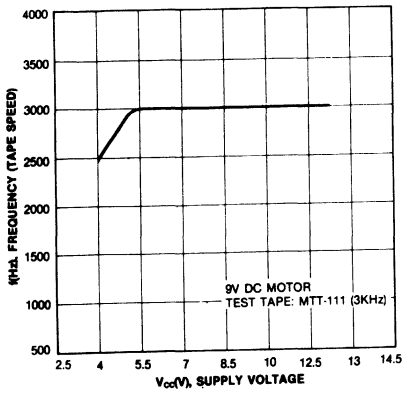


REFERENCE VOLTAGE-AMBIENT TEMPERATURE

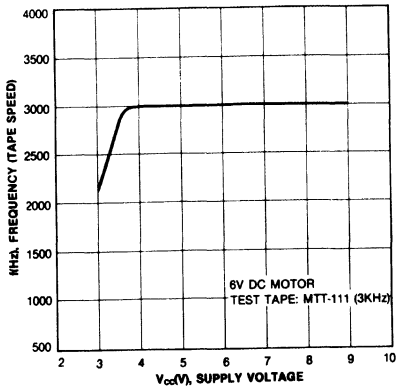


(APPLICATION CHARACTERISTICS)

FREQUENCY(TAPE SPEED)-SUPPLY VOLTAGE



FREQUENCY (TAPE SPEED) SUPPLY VOLTAGE



APPLICATION CIRCUIT

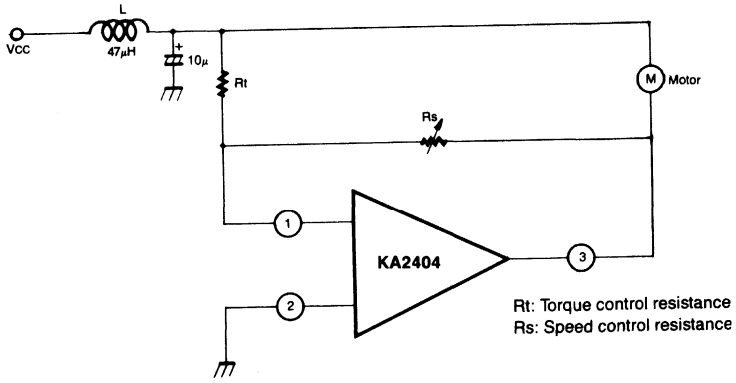
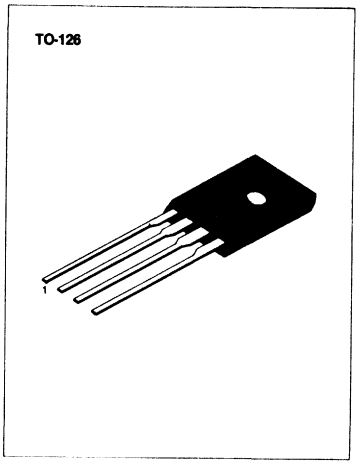


Fig. 5

DC MOTOR SPEED CONTROLLER

The KA2407 is a monolithic integrated circuit designed for DC motor speed controllers.



FEATURES

- **High stable operation over a wide range of supply voltage; V_{CC} = 3.5V ~ 14.4V**
- **Stable low reference voltage (1.0V Typ) for wide motor speed setting**
- **A minimum number of external parts required**
- **Small four-lead plastic package for compact motor**
- **Reverse voltage protection circuit**

APPLICATIONS

- Tape recorders & recorder players
- Home stereos
- Car components

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2407	TO-126	-20°C ~ +70°C

BLOCK DIAGRAM

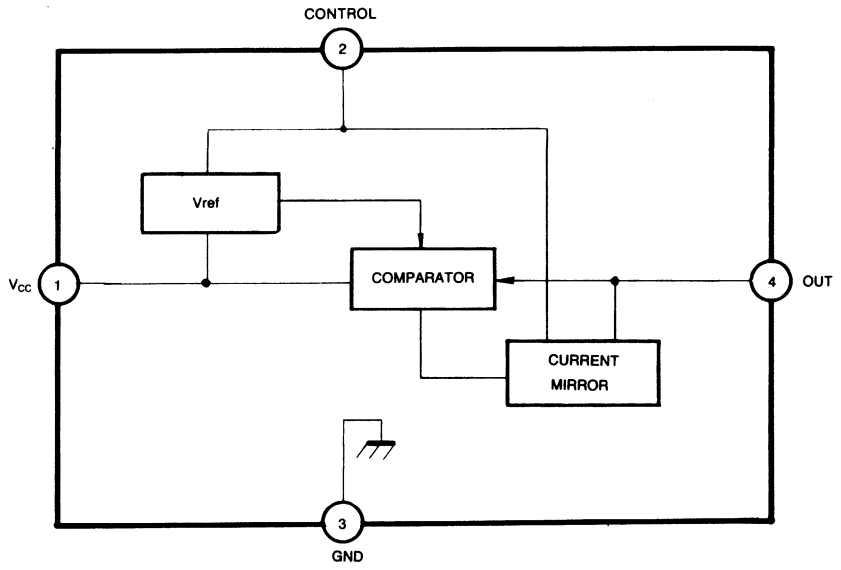


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	14.4	V
Supply Current	I_{CC} (Note 1)	2	A
Power Dissipation	P_D (Note 2)	1.3	W
Operating Temperature	T_{OPR}	−20 ~ +75	°C
Storage Temperature	T_{STG}	−40 ~ +150	°C

(Note 1): $t \leq 5$ sec
(Note 2): Ta = 25°C, With a 100 x 100mm bakelite printed circuit board (35μm Cu leaf)

ELECTRICAL CHARACTERISTICS (Ta = 25°C, V_{CC} = 6V)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Test Circuit
Reference Voltage	V_{REF}	Ra = 1KΩ	0.85	1.0	1.15	V	1
Quiescent Circuit Current	I_{CCQ}			0.8	1.8	mA	3
Current Coefficient	K	ΔI_4 = 40mA	35	40	45		2
Saturation Voltage	V_{SAT}	V_{CC} = 4.2V, Ra = 5Ω		1.15	2	V	1
Voltage Characteristic of Reference Voltage	$\frac{\Delta V_{REF}}{V_{REF}} / \Delta V_{CC}$	V_{CC} = 3.5V ~ 14V, Ra = 1KΩ		−0.1		%/V	1
Voltage Characteristic of Current Coefficient	$\frac{\Delta K}{K} / \Delta V_{CC}$	V_{CC} = 3.5V ~ 14V, ΔI_4 = 40mA		0.1		%/V	2
Current Characteristic of Reference Voltage	$\frac{\Delta V_{REF}}{V_{REF}} / \Delta I_4$	I_4 = 50mA ~ 200mA		−0.02		%/mA	1
Current Characteristic of Current Coefficient	$\frac{\Delta K}{K} / \Delta I_4$	I_4 = 50mA ~ 200mA		−0.01		%/mA	2
Temperature Characteristic of Reference Voltage	$\frac{\Delta V_{REF}}{V_{REF}} / \Delta Ta$	Ta = −20 ~ +75°C, Ra = 1KΩ		0.01		%/°C	1
Temperature Characteristic of Current Coefficient	$\frac{\Delta K}{K} / \Delta Ta$	Ta = −20 ~ +75°C, ΔI_4 = 40mA		0.01		%/°C	2

TEST CIRCUIT 1

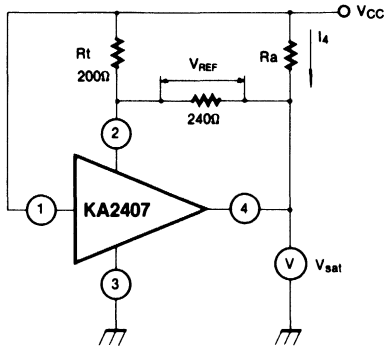


Fig. 2

V_{REF}, V_{SAT}, $\frac{\Delta V_{REF}}{V_{REF}}/V_{CC}$, $\frac{\Delta V_{REF}}{V_{REF}}/I_4$ $\frac{\Delta_{REF}}{V_{REF}}/Ta$,

TEST CIRCUIT 2

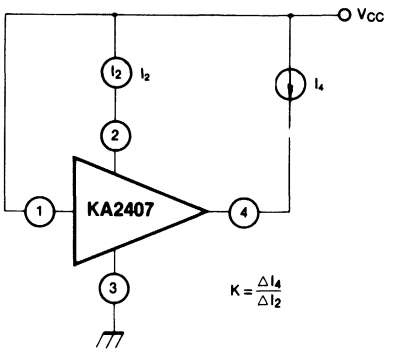


Fig. 3

K, $\frac{\triangle K}{K}/V_{CC}$, $\frac{\triangle K}{K}/I_4$, $\frac{\triangle K}{K}/Ta$

TEST CIRCUIT 3

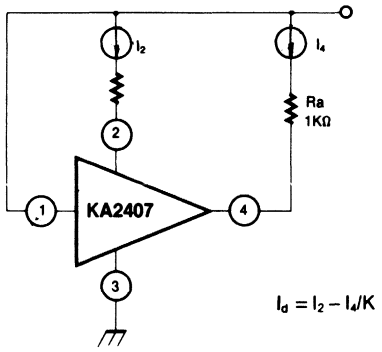
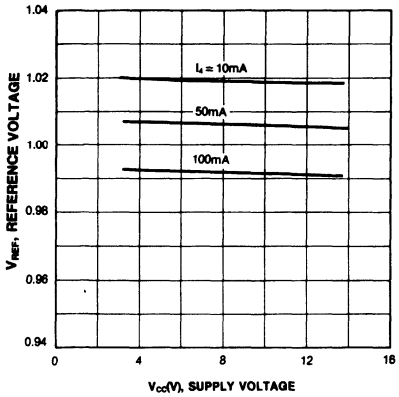
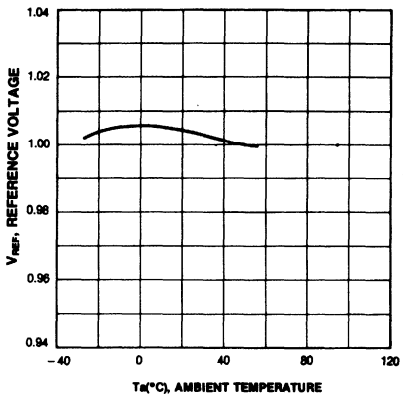


Fig. 4

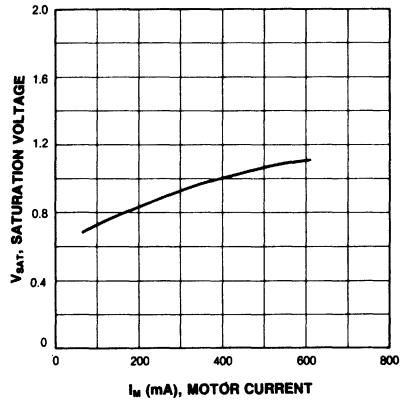
REFERENCE VOLTAGE-SUPPLY VOLTAGE



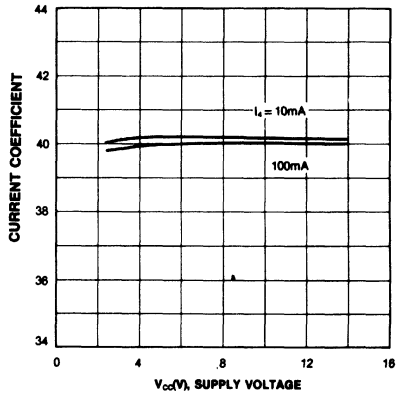
REFERENCE VOLTAGE-AMBIENT TEMPERATURE



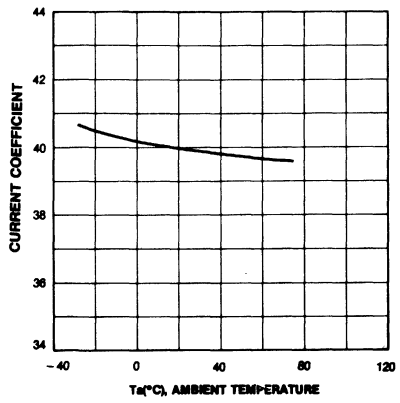
SATURATION VOLTAGE-MOTOR CURRENT



CURRENT COEFFICIENT-SUPPLY VOLTAGE



CURRENT COEFFICIENT-AMBIENT TEMPERATURE



APPLICATION CIRCUIT

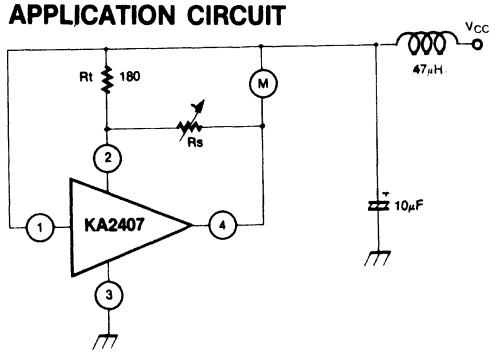
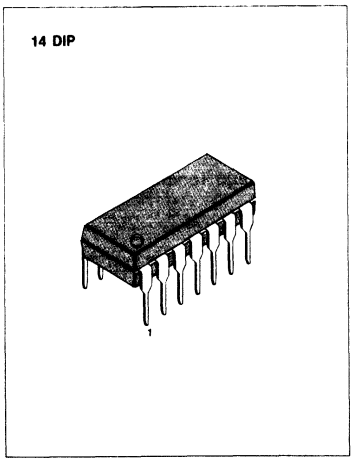


Fig. 5

DUAL EQUALIZER AMPLIFIER WITH ALC

The KA7226 is a monolithic integrated circuit consisting of a dual equalize amplifier with ALC. It is suitable for use in the record/ playback amplifier of stereo radio cassettes.



FEATURES

- **Dual equalizer amplifier with ALC circuit**
- **Built-in buffer amplifier**
- **Not necessary input coupling capacitor**
- **Quick stabilization after power on**
- **High output voltage: V_O = 1.7V (Typ) at THD = 1%**
- **Wide operating supply voltage range: V_{CC} = 3V ~ 16V**

BLOCK DIAGRAM

ORDERING INFORMATION

Device	Package	Operating Temperature
KA7226	14 DIP	- 25°C ~ + 75°C

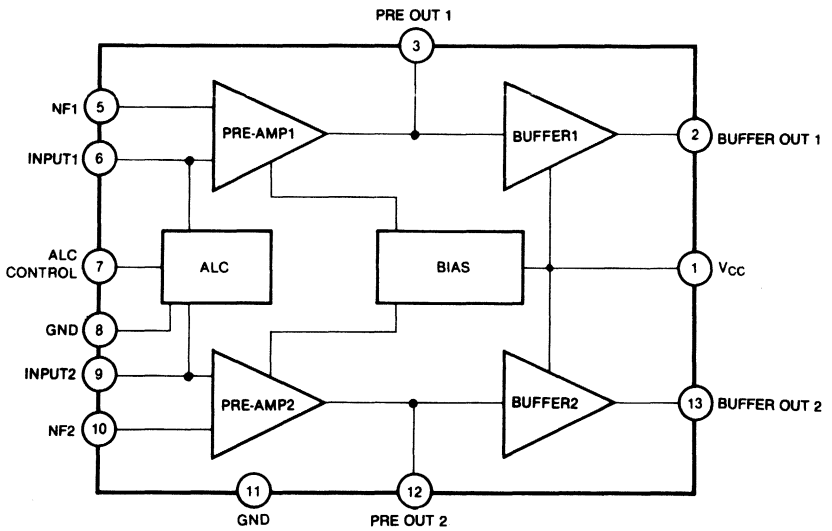


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Power Dissipation	P_D	600	mW
Operating Temperature	T_{OPR}	−25 ~ +75	°C
Storage Temperature	T_{STG}	−40 ~ +125	°C

* : Derated above Ta = 25°C in the propotion of 5mW/°C.

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 5V, f = 1KHz, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CCQ}	V_I = 0	6	10	15	mA
ALC Range	ΔV_{ALC}	V_I = −60dBm	35	40		dB
ALC Voltage	$V_{O\,(ALC)}$	V_I = −20dBm	−3	−1	1	dBm
ALC Distortion	THD_{ALC}	V_I = −20dBm		0.6	2.0	%
ALC Balance	CB_{ALC}	V_I = −20dBm		0	2	dB
Output Voltage	V_O	THD = 1%	1.3	1.7		V
Cross Talk	CT	R_G = 2.2KΩ V_O − 0dBm	40	60		dB
Open Loop Voltage Gain	G_{VO}	V_I = −80dBm	67	75		dB
Equivalent Input Noise Voltage	V_{NI}	R_G = 2.2KΩ,		1.3	2.7	μV

TEST CIRCUIT

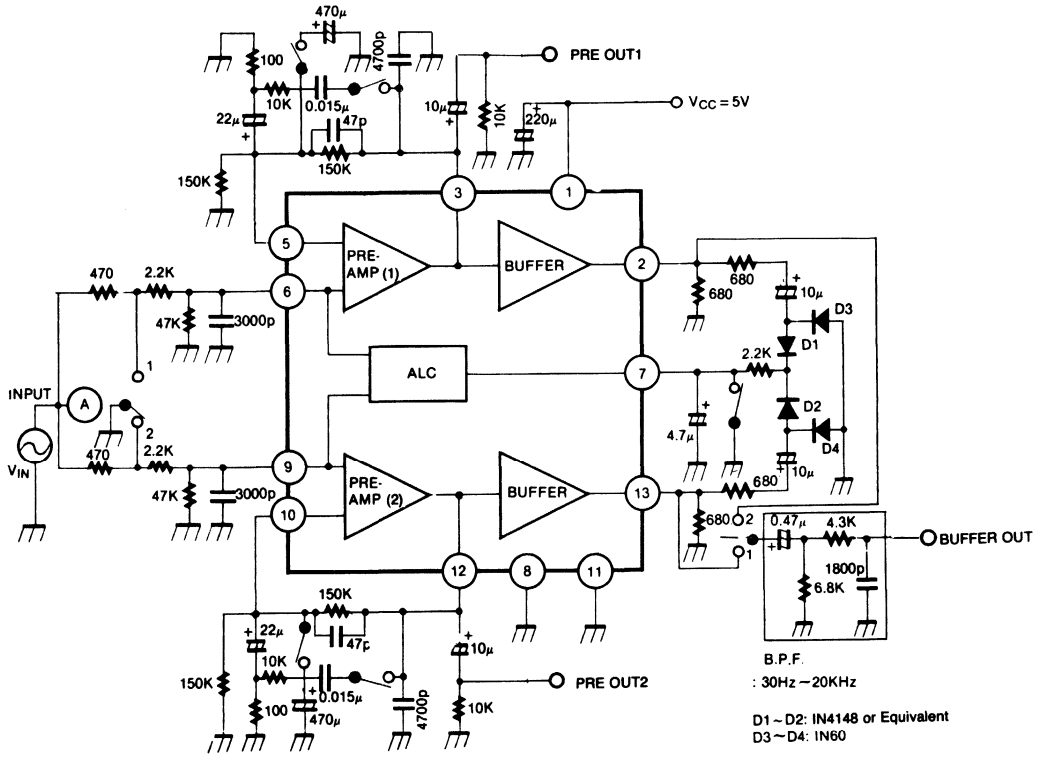
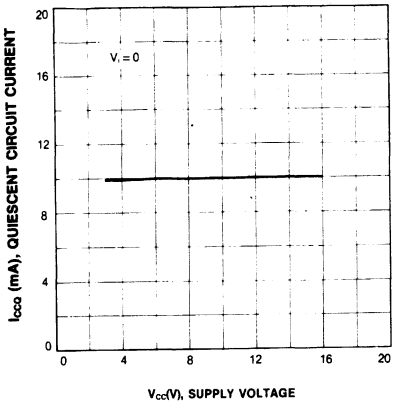
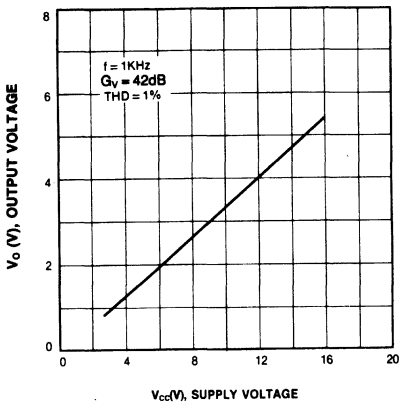


Fig. 2

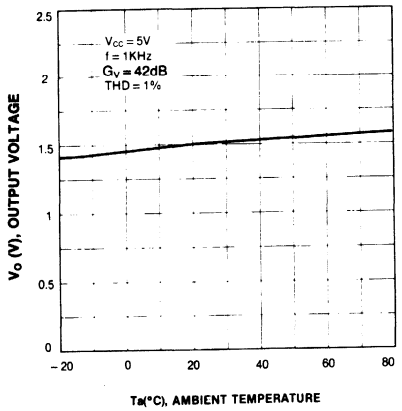
QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE



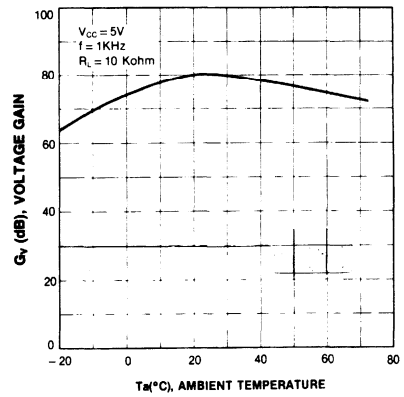
OUTPUT VOLTAGE-SUPPLY VOLTAGE



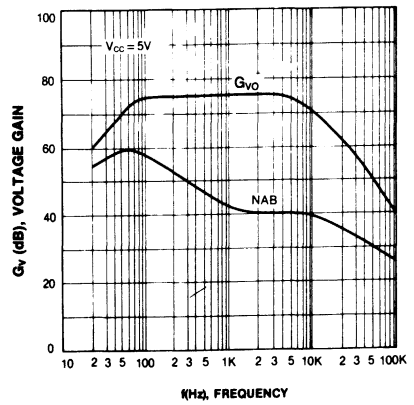
OUTPUT VOLTAGE-AMBIENT TEMPERATURE



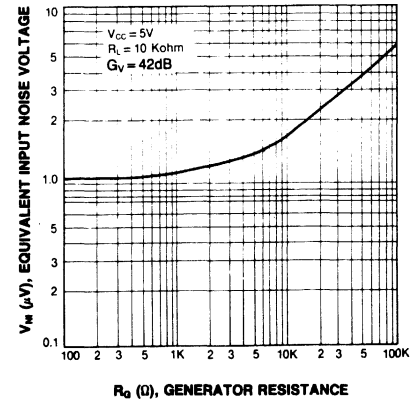
VOLTAGE GAIN-AMBIENT TEMPERATURE



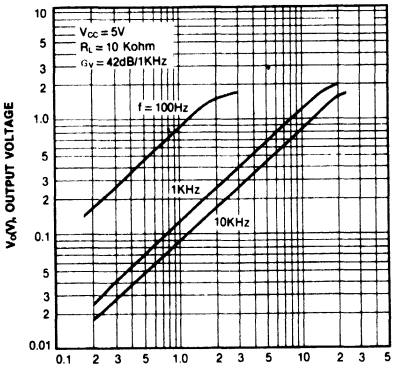
VOLTAGE GAIN-FREQUENCY



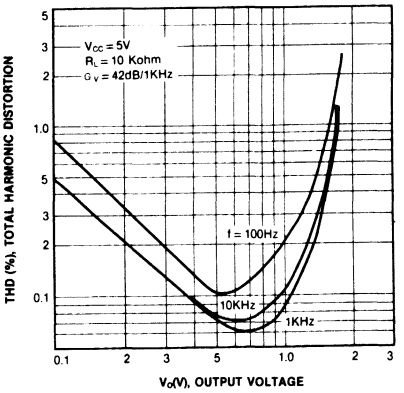
EQUIVALENT INPUT NOISE VOLTAGE
-GENERATOR RESISTANCE



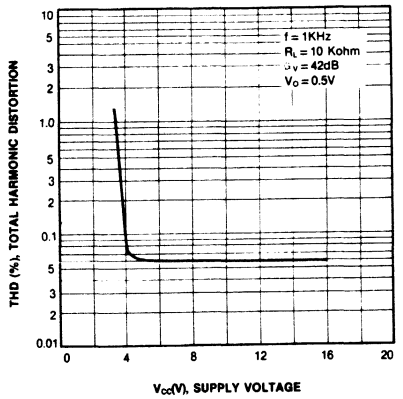
OUTPUT VOLTAGE-INPUT VOLTAGE



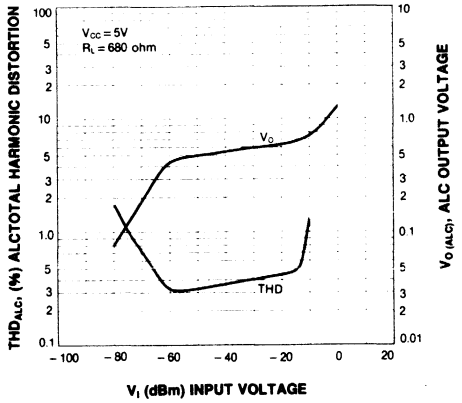
TOTAL HARMONIC DISTORTION-OUTPUT VOLTAGE



TOTAL HARMONIC DISTORTION-SUPPLY VOLTAGE



ALC OUTPUT VOLTAGE ALC TOTAL HARMONIC DISTORTION-INPUT VOLTAGE



APPLICATION CIRCUIT

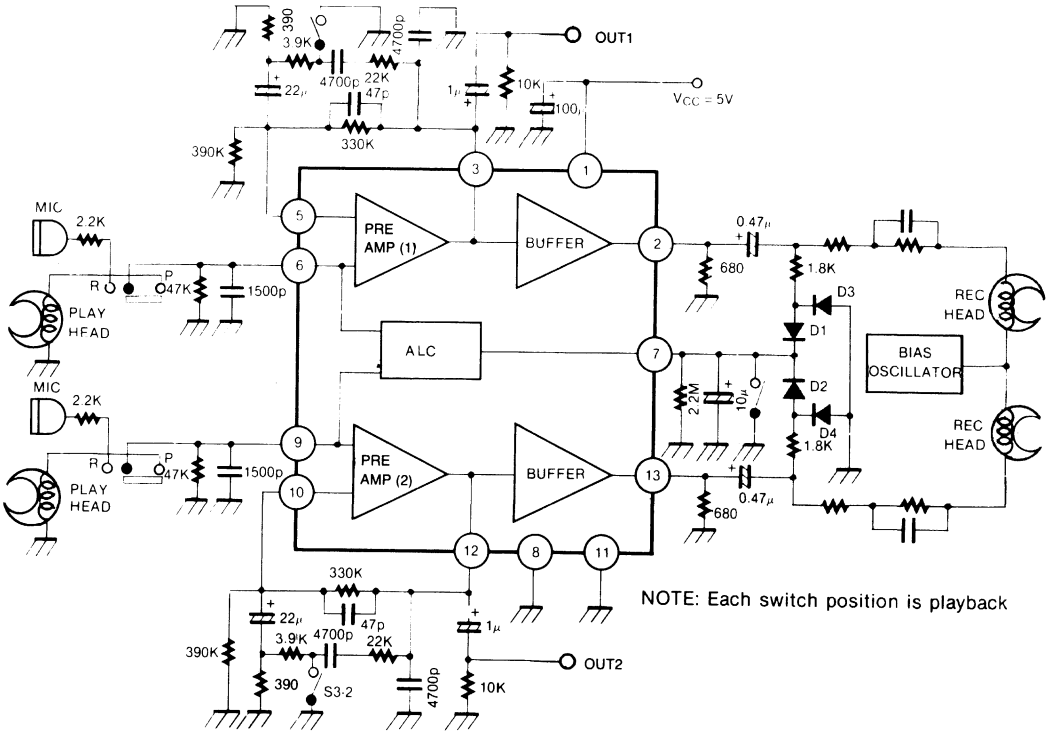
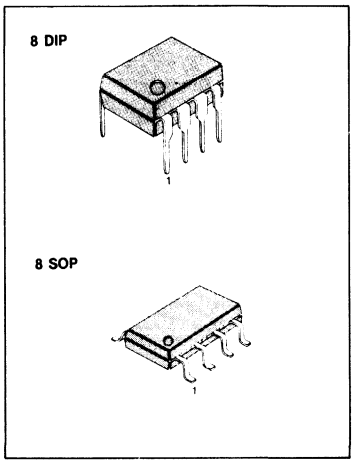


Fig. 3

LOW VOLTAGE AUDIO AMPLIFIER

The KA8602 is a audio power amplifier available for low voltage. This amplifier supplies differential outputs for maximizing output swing at low voltages. The KA8602 doesn't need coupling capacitors to the speaker. The gain of this amp is controlled easily by two external resistors.



FEATURES

- **Wide Supply Voltage: V_{CC} = 2V ~ 16V**
- **Low Quiescent Supply Current (I_{CCQ} = 3mA)**
- **Easy Gain Control**
- **Medium Output Power**
  P_O = 250mW at V_{CC} = 6V, R_L = 32Ω, THD = 10%
- **Minimum External Parts**
- **Load Impedance Range (8Ω ~ 100Ω)**
- **Low Distortion**
- **Mute Function (I_{CC} = 75μA)**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA8602N	8DIP	-20°C ~ +70°C
KA8602D	8SOP	

BLOCK DIAGRAM

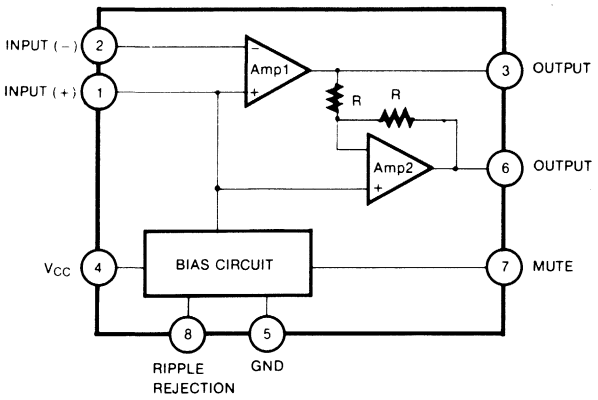
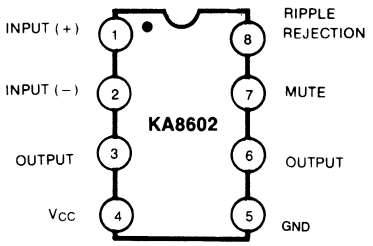


Fig. 1



PIN DESCRIPTION

Pin No.	Symbol	Description
1	Input (+)	Analog Ground for the amplifiers. A 1.0μF capacitor at this pin (with a 5.0μF capacitor at pin 8) provides 52dB (Typ) of power supply rejection. Turn-on time of the circuit is affected by the capacitor on this pin. This pin can be used as an alternate input.
2	Input (−)	Amplifier input. The input capacitor and resistor set low frequency rolloff and input impedance. The feedback resistor is connected to this pin and output.
3	Output	Amplifier 1's output. The DC Level is ≈ $(V_{CC} - 0.7V)/2$
4	V_{CC}	DC supply voltage (+2.0 ~ +16V) is applied to this pin.
5	GND	Ground pin.
6	Output	Amplifier 2's output. This signal is equal in amplitude, but 180° out of phase with that at output pin. The DC level is ≈ $(V_{CC} - 0.7V)/2$.
7	Mute	This pin can be used to power down the IC to conserve power, or for muting, or both. When at a logic "Low" (0 to 0.8 volts), the KA8602 is enabled for normal operation. When at a logic "High" (2.0 to V_{CC} volts), the IC is disabled. If Mute is open, that is equivalent to a logic "Low".
8	Ripple Rejection	A capacitor at this pin increases power supply rejection, and affects turn-on time. This pin can be left open if the capacitor at pin 1 is sufficient.

ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Supply Voltage	V_{CC}	$-1.0 \sim +18$	V
Output Current (output pin)	I_O	± 250	mA
Maximum Voltage (input, RR, Mute pin)	$V_{IM\ (DC)}$	$-1.0 \sim V_{CC}+1.0$	V
Applied Output Voltage (output pin) when disabled	V_O	$-1.0 \sim V_{CC}+1.0$	V
Junction Temperature	T_J	$-55 \sim +140$	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 6 V, Ta = 25°C, unless otherwise noted)

Characteristic		Symbol	Test Conditions		Min	Typ	Max	Unit
DC ELECTRICAL CHARACTERISTICS								
Quiescent Circuit Current (R_L = 0)		I_{CCQ}	V_{CC} = 3.0V, Mute = 0.8V V_{CC} = 16.0V, Mute = 0.8V V_{CC} = 3.0V, Mute = 2.0V			2.7 3.3 65	4.0 5.0 100	mA mA μA
Output Voltage (output Pin)		V_O	R_L = 16Ω R_1 = 75KΩ	V_{CC} = 3.0V V_{CC} = 6.0V V_{CC} = 12.0V	1.0	1.15 2.65 5.65	1.25	V
Output Offset Voltage		V_{OO}	V_{CC} = 6.0V, R_1 = 75KΩ, R_L = 32Ω		−30	0	+30	mV
Output High Voltage		V_{OH}	2.0V ≤ V_{CC} ≤ 16V, I_{out} = −75mA			V_{CC} − 1.0		V
Output Low Voltage		V_{OL}	2.0V ≤ V_{CC} ≤ 16V, I_{out} = 75mA			0.16		V
Input Bias Current (pin 2)		I_M				−100	−200	mA
Equipment Resistance		R_E	pin 1 pin 8		100 18	150 25	220 40	KΩ
Mute	Input Low Voltage	$V_{IL\ (MUTE)}$					0.8	V
	Input High Voltage	$V_{IH\ (MUTE)}$			2.0			V
	Input Resistance	$R_{L\ (MUTE)}$	V_{CC} = Mute = 16V		50	90	175	KΩ
AC ELECTRICAL CHARACTERISTICS								
Open Loop Voltage Gain (Amp 1)		G_{VO}			80			dB
Closed Loop Voltage Gain (Amp 2)		G_{VC}	f = 1.0KHz, R_L = 32Ω		−0.35	0	+0.35	dB
Output Power		P_O	V_{CC} = 3.0V, R_L = 16Ω, THD ≤ 10% V_{CC} = 6.0V, R_L = 32Ω, THD ≤ 10% V_{CC} = 12V, R_L = 100Ω, THD ≤ 10%		55 250 400			mW
Total Harmonic Distortion (f = 1.0 KHz)		THD	V_{CC} = 6.0V, R_L = 32Ω, P_O = 125mW V_{CC} ≤ 3.0V, R_L = 8Ω, P_O = 20mW V_{CC} ≤ 12V, R_L = 32Ω, P_O = 200mW			0.5 0.5 0.6	1.0	%
Gain Bandwidth Product		GBW				1.5		MHz
Power Supply Rejection Ratio (V_{CC} = 6.0V, ΔV_{CC} = 3.0V)		PSRR	C_1 = ∞, C_2 = 0.01μF C_1 = 0.1μF, C_2 = 0, f = 1.0KHz C_1 = 1.0μF, C_2 = 5.0μF, f = 1.0KHz		50	 12 52		dB
Muting		MUTE	Mute = 2.0V, 1.0KHz ≤ f ≤ 20KHz			>70		dB

APPLICATION CIRCUIT

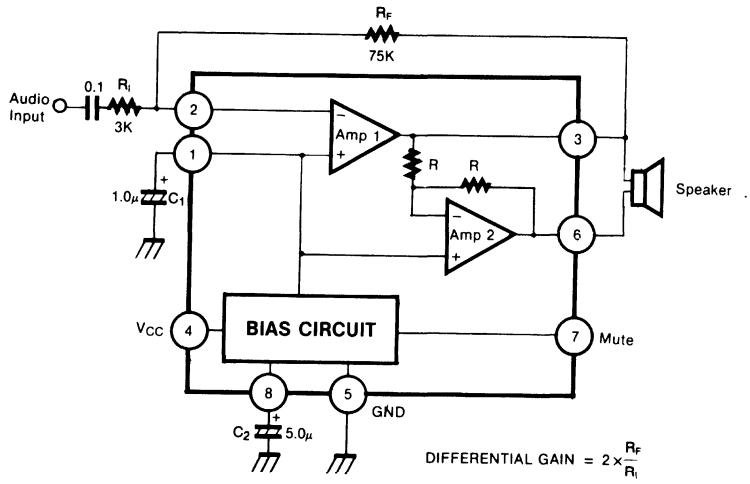
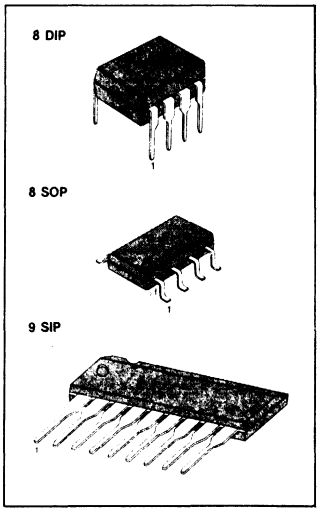


Fig. 2

LOW VOLTAGE AUDIO POWER AMPLIFIER

The KA386/S/D is a power amplifier designed for use in low voltage consumer applications. The gain is internally set to 20 to keep the external part count low, but the addition of an external resistor and capacitor between Pins 1 and 8 will increase the gain to any value up to 200.



FEATURES

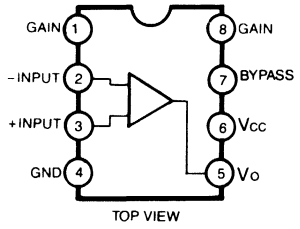
- **Battery operation.**
- **Minimum external parts.**
- **Wide supply voltage range: 4V ~ 12V (KA386)**
  4V ~ 9V (KA386S/D)
- **Low quiescent current drain (4mA.)**
- **Voltage gains : 20 ~ 200.**
- **Ground referenced input.**
- **Self-centering output quiescent voltage.**
- **Low distortion.**
- **3 kinds of package types**
  KA386 (8 Dip), KA386S (9 Sip), KA386D (8 Sop)

ORDERING INFORMATION

Device	Package	Operating Temperature
KA386	8 DIP	-20°C ~ +70°C
KA386S	9 SIP	
KA386D	8 SOP	

BLOCK DIAGRAM

(KA386/D)



(KA386S)

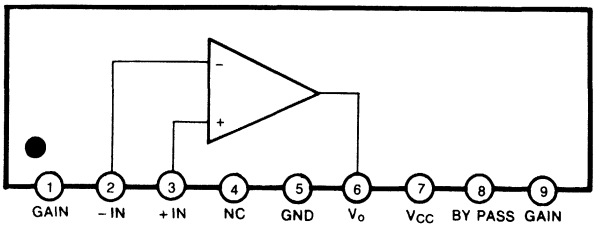


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic		Symbol	Value	Unit
Supply Voltage		V_{CC}	15	V
Power Dissipation	KA386	P_D	660	mW
	KA386S		500	
	KA386D		300	
Input Voltage		V_I	± 0.4	V
Operating Temperature		T_{OPR}	− 20 ~ + 70	°C
Storage Temperature		T_{STG}	− 40 ~ + 125	°C

ELECTRICAL CHARACTERISTICS

(T_a = 25°C, V_{CC} = 6V, R_L = 8Ω, f = 1KHz, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescient Circuit Current	I_{CCQ}	V_I = 0		4	8	mA
Output Power	P_o	V_{CC} = 6V, THD = 10%	250	325		mW
		V_{CC} = 9V, THD = 10%	500	700		mW
Voltage Gain	G_V	Pins 1 and 8 Open		26		dB
		10μF from Pin 1 to 8		46		
Bandwidth	BW	Pins 1 and 8 Open		300		KHz
		10μF from Pin 1 to 8		60		
Total Harmonic Distortion (D-Type)	THD	P_o = 125mW, Pins 1 and 8 Open		0.2		%
Input Resistance	R_I			50		KΩ
Input Bias Current	I_{BIAS}	Pins 1 and 8 Open		250		nA

APPLICATION CIRCUIT

Amplifier with Gain=50 (34 dB)

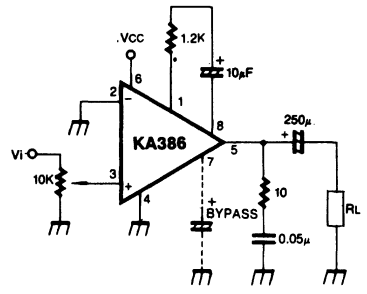
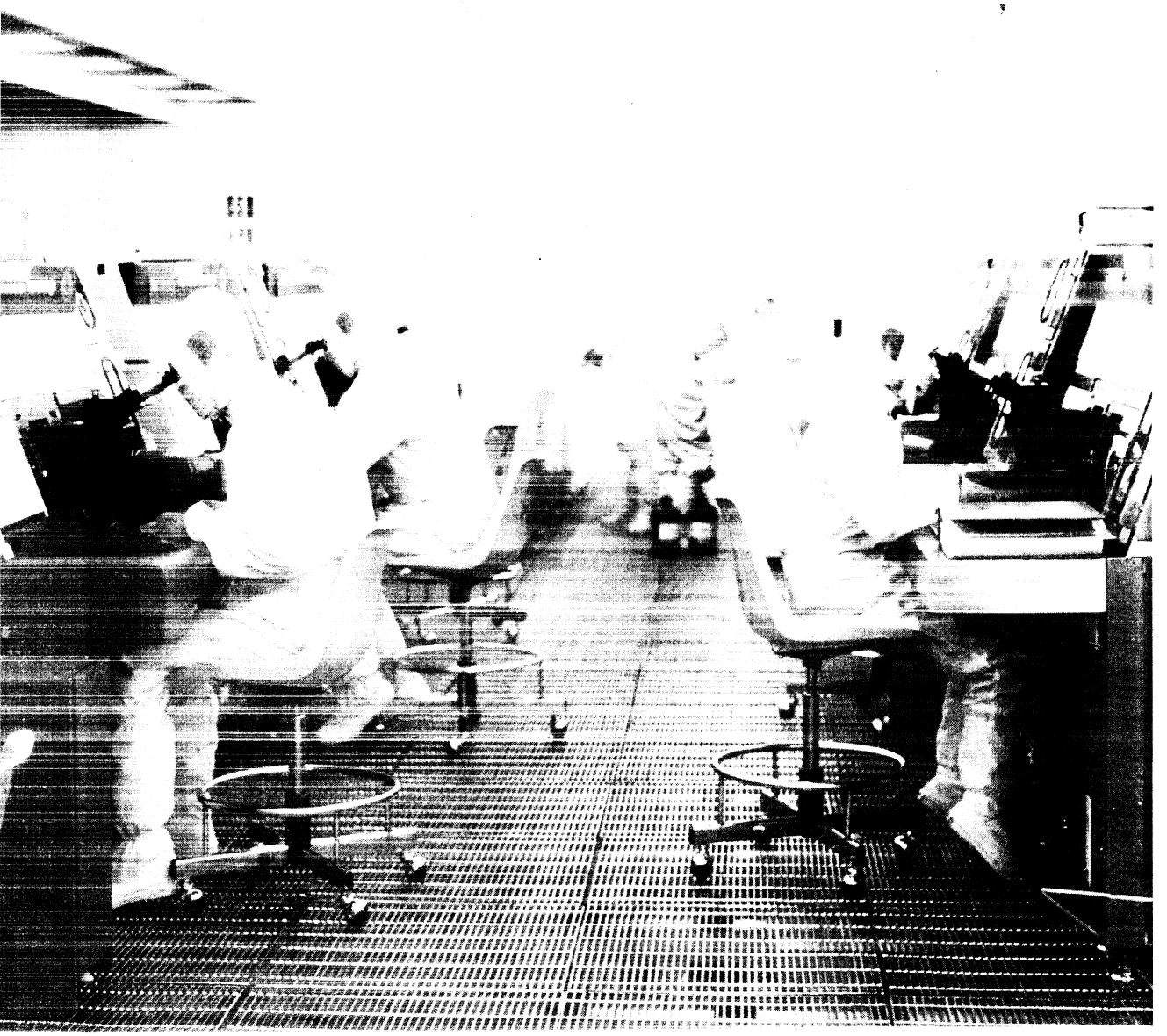


Fig. 2

CDP ICs 4

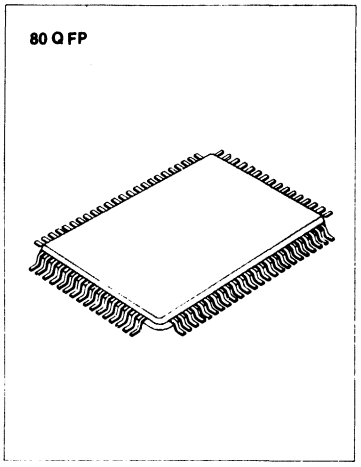


CDP APPLICATION

Device	Function	Package	Page
KS5990	Digital Signal Processor	80 QFP	335
KS5991	Digital Signal Processor	80 QFP	364
KA8309B	Servo Signal Processor	48 QFP	393
KA9201	RF Amp for CDP	30 SOP/30 SDIP/32 QFP	407
KS9210	Digital Signal Processor	80 QFP	418
KS9211	Digital Signal Processor	80 QFP	446
KA9221	Servo Signal Processor	48 QFP	475
KA9256	Dual Power Operational Amplifier	10 SIP H/S	491
KA9257	Dual Power Operational Amplifier	12 SIP H/S	493
KA9270	Audio Filter for CDP	20 DIP/SOP	497
KDA0316	16-bit D/A Converter for CDP	20 DIP/20 SOP	504
KS56C820	4-bit Microcontroller	80 QFP	510

DIGITAL SIGNAL PROCESSOR

The KS5990 is a CMOS integrated circuit designed for compact disc player applications. It consists of 16KSRAM, digital filter, and digital signal processing circuits.



FEATURES

- All digital signals for regeneration are processed using one chip.
- Internal aperture compensation digital filter
- EFM-PLL circuit for bit clock regeneration
- EFM data demodulation
- Frame synchronous signal detection, protection
- Compensation using mean value and prior value retention
- Subcode signal demodulation subcode Q detection
- CLV servo for spindle motor
- 8-bit tracking counter
- CPU interface with serial bus
- Subcode Q register
- Built-in 17th digital filter
- Built-in 16KSRAM
- 80 Quad flat package type

ORDERING INFORMATION

Device	Package	Operating Temperature
KS5990	80 QFP	−20°C ~ +75°C

BLOCK DIAGRAM

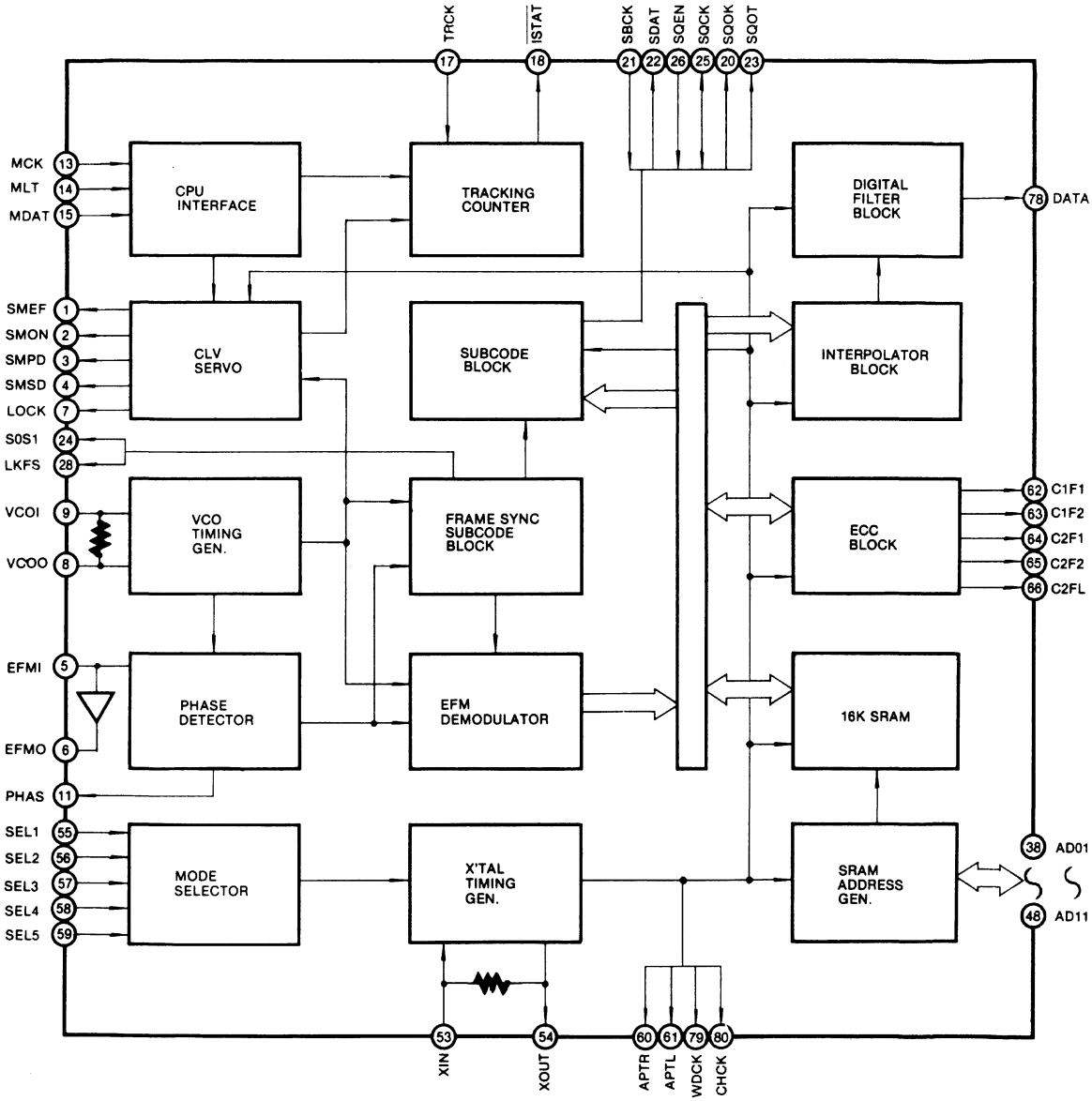


Fig. 1

PIN CONFIGURATION

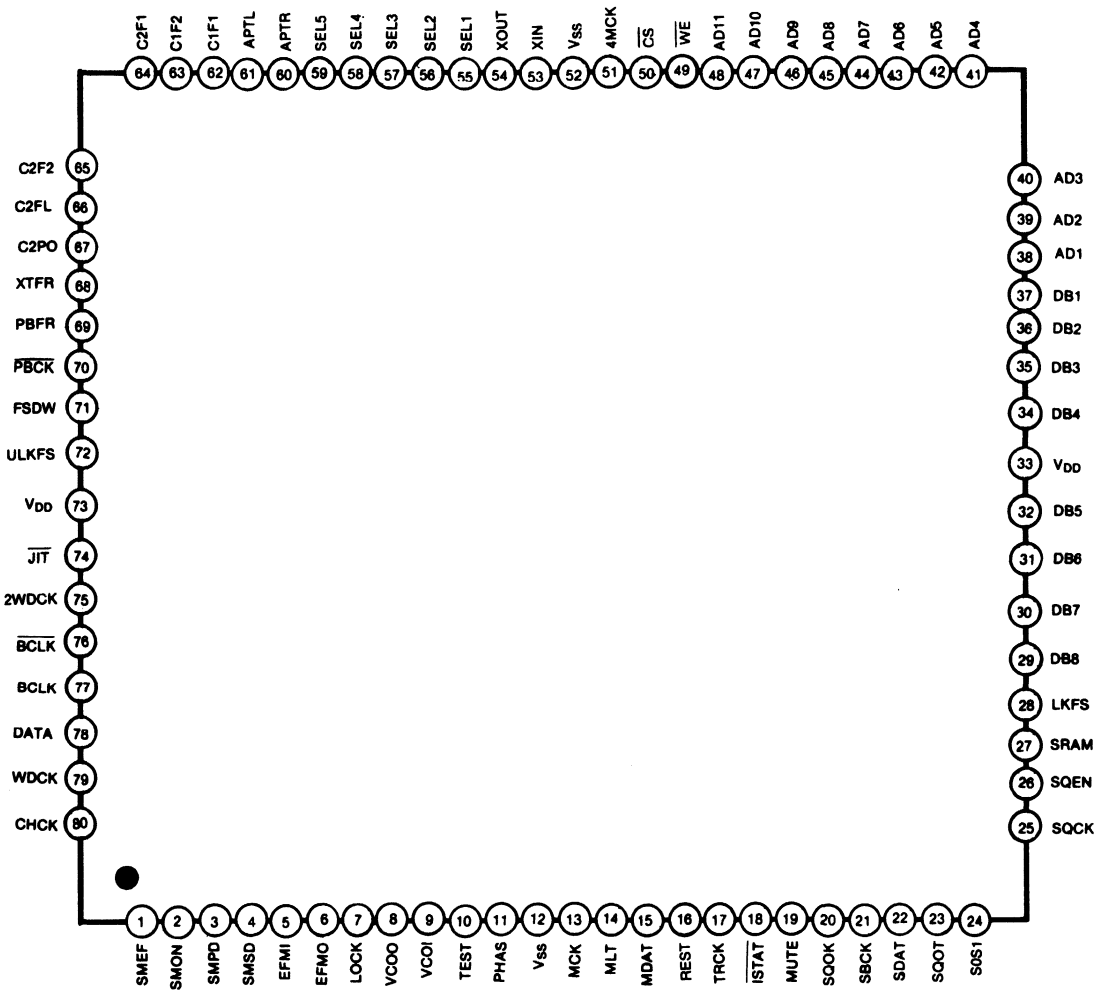


Fig. 2

PIN DESCRIPTION

Pin No	Symbol	I/O	Description
1	SMEF	O	Pin 1 output is switched constant when output filter of the spindle motor is energized.
2	SMON	O	ON/OFF control for spindle motor.
3	SMPD	O	Spindle motor drive. Provides rough control during CLV-S mode and phase control during CLV-P mode.
4	SMSD	O	Spindle motor drive. Controls speed during CLV-P mode.
5	EFMZ	I	EFM signal from RF amplifier.
6	EFMO	O	Controls slice level of the EFM signal.
7	LOCK	O	The output of pin 7 reflects the status of the GFS signal which is sampled at PBFR/16. When the GFS signals is "H", but, when the signal has remained "L" for at least 8 samples, the output of pin 7 is "L".
8	VCOO	O	VCO output. The frequency is f = 8.6436MHz, when locked by the DBFR signal.
9	VCOI	I	VCO input.
10	TEST	I	(0V).
11	PHAS	O	The output of Pin 11 provides phase comparison of EFM signal and VCO/2.
12	V_{SS}	—	GND (0V).
13	MCK	I	Pin 13 provides serial transmission clock from the CPU. Data is latched on the leading edge of the clock.
14	MLT	I	Pin 14 provides latch input from the CPU. 8-bit shift register data (serial data received from the CPU) is latched in each of the registers.
15	MDAT	I	Serial data from the CPU.
16	REST	I	System reset ("L").
17	TRCK	I	Tracking pulse input.
18	ISTAT	O	Output reflecting internal condition as designated by address.
19	MUTE	I	Muting input. MUTE is "L" when ATTM of internal register A is "L" (normal condition). MUTE is "H" when meting condition is set.
20	SQOK	O	Output the results CRC check of subcode Q.
21	SBCK	I	Clock input for subcode serial output.
22	SDAT	O	Serial output of subcode.
23	SQDT	O	Output of subcode Q.
24	S0S1	O	Output of subcode sync S0 + S1.
25	SQCK	I/O	Clock for reading subcode Q.
26	SQEN	I	Input for selecting SQCK (L; SQCK is output, H; SQCK is input)
27	SRAM	I	SRAM is "H" in Nomal, SRAM is "L" when system is testing.
28	LKFS	O	Display output for frame sync lock status.

PIN DESCRIPTION (Continued)

Pin No	Symbol	I/O	Description
29	DB8	I/O	Data pin for external RAM. DATA8 (MSB) in test mode. Hi-Z in normal
30	DB7	I/O	Data pin for external RAM. DATA7 in test mode. Hi-Z in normal
31	DB6	I/O	Data pin for external RAM. DATA6 in test mode. Hi-Z in normal
32	DB5	I/O	Data pin for external RAM. DATA5 in test mode. Hi-Z in normal
33	V_{DD}	—	Power supply (+5V).
34	DB4	I/O	Data pin for external RAM. DATA4 in test mode. Hi-Z in normal
35	DB3	I/O	Data pin for external RAM. DATA3 in test mode. Hi-Z in normal
36	DB2	I/O	Data pin for external RAM. DATA2 in test mode. Hi-Z in normal
37	DB1	I/O	Data pin for external RAM. DATA1 (LSB) in test mode. Hi-Z in normal
38	AD01	O	(LSB)
39	AD02	O	In normal mode (TEST = 'L', SRAM = 'H'), these pins are High impedance (Hi-Z) In test mode (TEST = 'H', SRAM = 'L'), these pins are Output address of external RAM
40	AD03	O	
41	AD04	O	
42	AD05	O	
43	AD06	O	
44	AD07	O	
45	AD08	O	
46	AD09	O	
47	AD10	O	
48	AD11	O	(MSB)
49	$\overline{WE}$	I/O	In normal mode, this is WE output. In test mode, write enable input.
50	$\overline{CE}$	I/O	In normal mode, this is CE output. In test mode, chip enable input.
51	4MCK	O	Divider output for crystal. f = 4.2336MHz
52	V_{SS}	—	GND (0V)
53	XIN	I	Input to crystal oscillator circuit. Depending on the mode, the frequency is either f = 8.4672 r 16.9344MHz.
54	XOUT	O	Output from crystal oscillator circuit. Depending on the mode, the frequency is either f = 8.4672 or 16.9344MHz.
55	SEL1	I	Mode selection input 1.
56	SEL2	I	Mode selection input 2.
57	SEL3	I	Mode selection input 3.
58	SEL4	I	Mode selection input 4. Code switch input for audio data output. 2's complement output when "L", and offset binary output when "H"
59	SEL5	I	Mode selection input 5. Code switch input for audio data output. Serial output when "L", parallel output when "H".

PIN DESCRIPTION (Continued)

Pin No	Symbol	I/O	Description
60	APTR	O	Output for aperture compensation. "H" when R-ch.
61	APTL	O	Output for aperture compensation. "H" when L-ch.
62	C1F1	O	Monitor output reporting status of error correction for C1 decoder. When SEL5 = 'L', DA01 (LSB of parallel audio data) is output when SEL5 = 'H'.
63	C1F2	O	Monitor output reporting status of error correction for C1 decoder when SEL5 = 'L', DA02 is output when SEL5 = 'H'.
64	C2F1	O	Monitor output reporting status of error correction for C2 decoder when SEL5 = 'L', DA03 is output when SEL5 = 'H'.
65	C2F2	O	Monitor output reporting status of error correction for C2 decoder when SEL5 = 'L', DA04 is output when SEL5 = 'H'.
66	C2FL	O	Output of status condition when SEL5 = 'L'. C2FL is set 'H' when the C2 sequence, being corrected becomes impossible to correct. DA05 is output when SEL5 = 'H'.
67	C2PO	O	Display output of the C2 pointer when SEL5 = 'L'. DA06 is output when SEL5 = 'H'.
68	XTFR	O	When SEL5 = 'L', output of read frame dock, which is 7.35KHz of the crystal system. DA07 is output when SEL5 = 'H'.
69	PBFR	O	When SEL5 = 'I', output of write frame clock, which is 7.35KHz when locked by the crystal system. DA08 is output when SEL5 = 'H'.
70	$\overline{\text{PBCK}}$	O	When SEL5 = 'L', output of VCO/2 (f = 4.3218MHz when locked by the EFM signal). DA09 is output when SEL5 = 'H'.
71	FSDW	O	When SEL5 = 'L', output for unprotected frame sync patterns. DA10 is output when SEL5 = 'H'.
72	ULKFS	O	Output for display of status of frame sync protection when SEL5 = 'L', DA11 is ouput when SEL5 = 'H'.
73	V_{DD}	—	Power supply (+5V).
74	$\overline{\text{JIT}}$	O	When SEL5 = 'L', output for display of either RAM overflow or underflow for +4 frame jitter absorption. DA12 is output when SEL5 = 'H'.
75	ZWDCK	O	When SEL5 = 'L', output for strobe signal (352.8KHz when DF is ON, 176.4KHz when DF is OFF). DA13 is output when SEL5 = 'H'.
76	$\overline{\text{BLCK}}$	O	When SEL5 = 'L', inverse output of BLCK. DA14 is output when SEL5 = 'H'.
77	BLCK	O	When SEL5 = 'L', bit clock output (4.2336MHz when DF is ON, 2.1168MHz when DF is OFF) DA15 is output when SEL5 = 'H'.
78	DATA	O	Serial data output of audio signal when SEL5 = 'L'. DA16 is output when SEL5 = 'H'.
79	WDCK	O	Strobe signal output. Output is 176.4KHz when DF is on. Output is 88.2KHz when DF is off.
80	CHCK	O	Strobe signal output. Output is 88.2KHz when DF is on. Output is 44.1KHz when DF is off.

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{DD}	−0.3 ~ +7	V
Input Voltage	V_I	−0.3 ~ +7	V
Output Voltage	V_O	−0.3 ~ +7	V
Operating Temperature	T_{OPR}	−20 ~ +75	°C
Storage Temperature	T_{STG}	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(V_{DD} = 5V ± 10%, V_{SS} = 0V, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Input High Voltage	V_{IH1}	Note 1	0.7 V_{DD}		V_{DD}	V
Input Low Voltage	V_{IL1}	Note 1			0.3 V_{DD}	V
Input High Voltage	V_{IH2}	Note 2	0.8 V_{DD}			V
Input Low Voltage	V_{IL2}	Note 2			0.2 V_{DD}	V
Output High Voltage	V_{OH}	I_{OH} = −1mA	V_{DD} − 0.5		V_{DD}	V
Output Low Voltage	V_{OL}	I_{OL} = 1mA	0		0.4	V
Input Leakage Current	I_{LKG}	V_{IN} = 0 ~ 5.5V	−5		+5	μA
Three-State Pin Output Leakage Current	I_{LKG}	V_{OUT} = 0 ~ 5.5V	−5		+5	μA
SRAM Input Leakage Current	I_{LKG}	V_{IN} = 0 ~ 5.5V	−5		+200	μA

Note 1. Related pins—EFMI. RESET. TEST. MUTE. SEL 2 ~ 5. MLT. MDAT. SQEN. SQCK.
Note 2. Related pins—TRCK. MCK. SRAM.

2. AC Characteristics

A. XIN Pin, VCOI Pin

(1) When pulse applied to XIN and VCO, V_{DD} = 5V ± 10%, V_{SS} = 0V, and Ta = 25°C, unless otherwise specified.

Characteristic	Symbol	Min	Typ	Max	Unit
"H" Level Pulse Width	t_{WHX}	20			ns
"L" Level Pulse Width	t_{WLX}	20			ns
Pulse Frequency	t_{CK}	55			ns
Input "H" Level	V_{IH}	V_{DD} − 1.0			V
Input "L" Level	V_{IL}			0.8	V
Rising Time Breaking Time	t_R			15	ns

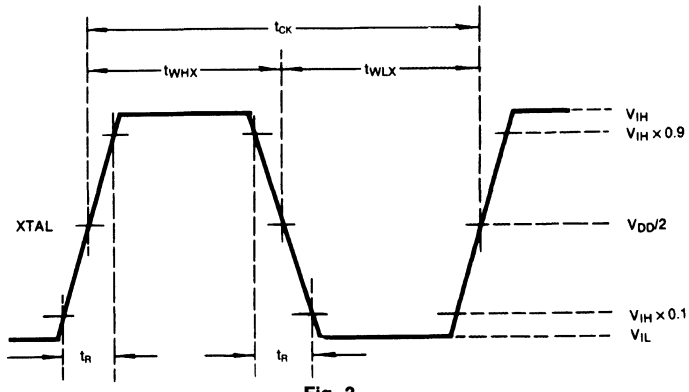


Fig. 3

B. Pins MCK, DATA, MLT, TRCK, SQCK

($V_{DD} = 5.0V \pm 10\%$, $V_{SS} = 0V$, $T_{OPR} = -20 \sim +75°C$)

Characteristic	Symbol	Min	Typ	Max	Unit
Clock Frequency	f_{CK}			1	MHz
Clock Pulse Width	t_{WCK}	300			ns
Setup Time	t_{SU}	300			ns
Hold Time	t_H	300			ns
Delay Time	t_D	300			ns
Latch Pulse Width	t_W	300			ns
CNIN SQCK Frequency	f_{CK2}			1	MHz
CNIN SQCK Pulse Width	t_{WCK2}	300			ns

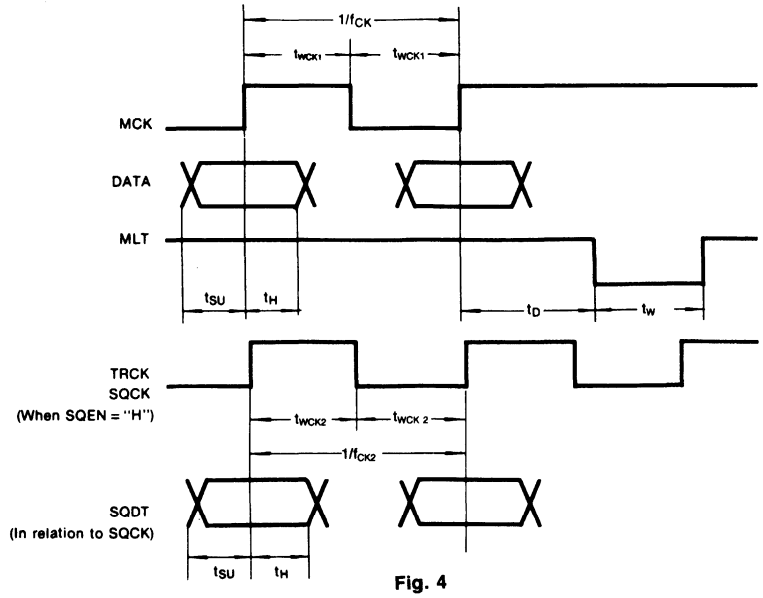


Fig. 4

C. DAC Interface (V_{DD} = 5V ± 10%, V_{SS} = 0V, T_{OPR} = −20 ~ +75°C, C_L = 50pF)

Item	Symbol	DF is OFF			When DF ON			Unit
		Min	Typ	Max	Min	Typ	Max	
Clock Pulse Width	t_{WCK}		236			118		ns
Clock Skew (Fast)	t_{FCK}			40			40	ns
Data Skew (Fast)	$t_{F(SK)}$			0			0	ns
Data Skew (Delay)	$t_{D(SK)}$			80			80	ns

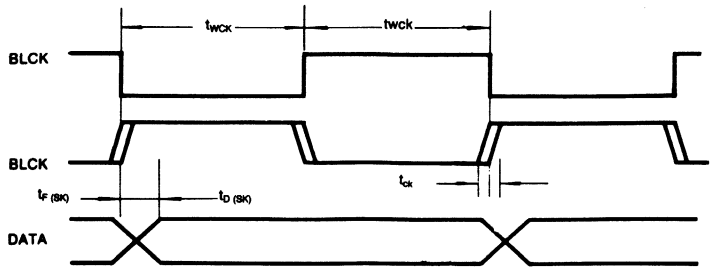


Fig. 5

*Note: CHCK, WDCK, APTR, APTL
DA01 through DA16 during parallel DA conversion or C1F1, C1F2, C2F1, C2F2, C2FL, C2PO, XTFR, 2WDCK, DATA during serial conversion.

APPLICATION INFORMATION
FUNCTION DESCRIPTION

MODE SELECTOR

To control several blocks in KS5991, there are 5 selecting pin signals. Table 1. shows selected mode by these signals.

Input Pins					Function*				
SEL1	SEL2	SEL3	SEL4	SEL5	XIN	DF	P/S	OB/2'S	CD ROM/Audio
0	1	0	0	0	16M	ON	S	2'S	Audio
0	1	0	1	1	16M	ON	P	OB	Audio
0	1	1	0	0	16M	OFF	S	2'S	Audio
0	1	1	1	1	16M	OFF	P	OB	Audio
1	0	0	0	0	8M	ON	S	2'S	Audio
1	0	0	1	1	8M	ON	P	OB	Audio
1	0	1	0	0	8M	OFF	S	2'S	Audio
1	0	1	1	1	8M	OFF	P	OB	Audio
1	1	1	1	0	8M	OFF	S	2'S	CD ROM

Table 1. Mode Selection

* Note: • 8M/16M: Selection of either the XIN or XOUT clocks will provide either a 8.4672MHz or 16.9344MHz signals.
  • DF: Digital Filter
  • P/S: Parallel mode/serial mode
  • OB/2'S: Offset

- Clock selection
  Selectioin of an 16.9344MHz or 8.4672MHz oscillator clock is possible at pins XIN and XOUT. However only 16.9344MHz clocks are provided for digital out usage.

- Digital filter selection
  When the digital filter function is switched to ON, all signals on the DAC interface are handled at twice the normal speed.

- Parallel/Serial output selection
  When the output is parallel, 16-bit parallel data is output from pins DA01 through DA16.
  When the output is serial, the following signals are output at pin DA01 through DA16.

DATA (DA16)	Serial data output (MSB or LSB first output)
BLCK (DA15)	Internal system clock (with DF ON 4.2336MHz and with DF OFF 2.1168MHz)
$\overline{\text{BLCK}}$ (DA14)	Bit clock (BLCK inversion signal)
2WDCK (DA13)	4X multiplied CHLK signal
$\overline{\text{JIT}}$ (DA12)	Jitter Margin Overflow/Underflow signal
ULKFS (DA11)	Display output of frame sync protection status
FSDW (DA10)	Unguarded (unprotected) frame sync signal
PBCK (DA09)	Signal at 1/2 V_{CO} pin cycle times. When locked 4.3218MHz
PBFR (DA08)	Write Frame Clock signal. When locked 7.35KHz.
XTFR (DA07)	Read Frame Clock signal. Crystal system 7.35KHz.
C2PO (DA06)	C2 Pointer signal
C2FL (DA05)	Correction mode output, C2FL = C2F1, C2F2
C2F2 (DA04) C2F1 (DA03)	Monitor Output of Error Correction Mode for C2 Decode
C1F2 (DA02) C1F1 (DA01)	Monitor Output of Error Correction Mode for C1 Decode

- OFFSET Binary/2's Complement Selection
  When pin SEL4 is at "H" output occurs at OFFSET BINARY; when it is at "L" output occurs at 2's complement.
- CD-ROM/AUDIO Selection
  When SEL1 = SEL2 = SEL3 = "H",CD-ROM is selected. Then the C2 pointer is output with each byte (8 bits) and neither the mean value interpolation nor the preceding value hold are exercised. That is, if an error occurs in the upper 8 bits of a 16-bit data, only the C2 pointer related to those upper 8 bits switches to "H" while the lower 8 bits are handled as correct data.

Microcomputer Interface

Data from the microcomputer are inputed through MDAT pins by MCK which is the clock signal of the microcomputer and the pulse signal through MLT pin is for inputed data load one of 6 kinds of control registers.

Fig. 6 Shows the timing diagram of data input from microcomputer.

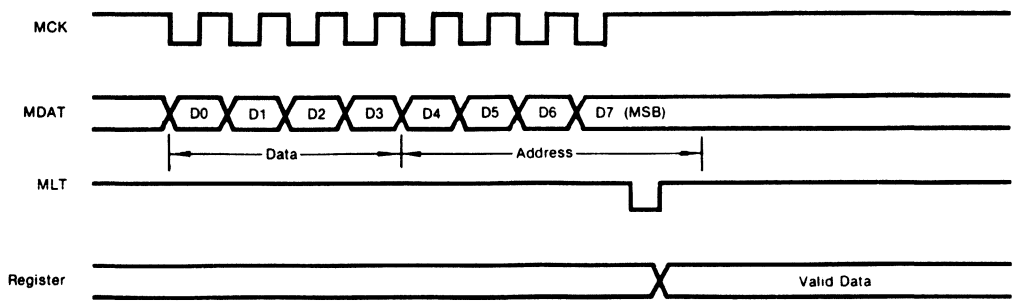


Fig. 6 Data Input Timing Diagram

According to the address of MDAT, control register is selected as below table 2.

Control Register	Comment	Address D7 - D4	Data				$\overline{\text{ISTAT}}$ Pin
			D3	D2	D1	D0	
CNTL-Z	Data Control	1 0 0 1	ZCMT	HIPD	NCLV	CRCD	Hi-Z
CNTL-S	Frame Sync Protection Attenuation Control	1 0 1 0	FSEM	FSEL	WSEL	ATTM	Hi-Z
CNTL-L	Tracking Counter Lower 4 Bit	1 0 1 1	TRC3	TRC2	TRC1	TRC0	$\overline{\text{Complete}}$
CNTL-U	Tracking Counter Upper 4 Bit	1 1 0 0	TRC7	TRC6	TRC5	TRC4	$\overline{\text{COUNT}}$
CNTL-W	CLV Control	1 1 0 1	COM	WB	WP	GAIN	Hi-Z
CNTL-C	CLV Mode	1 1 1 0	CLV Mode				$\overline{\text{PW}\geq 64}$

Table 2. Data of Selected Control Register

According to D0 through D1 DAA,
The function of each control register is described below.

1) CNTL-Z Register

This is a control register for the zero cross mute of audio data, PHAS, the control signal of phase servo and CRCF data.

		Data = 0	Data = 1
ZCMT	D3	Zero cross mute "OFF"	Zero cross mute "ON"
HIPD	D2	Phase normally active	Phase convert "L" to "Hi-Z" by LKFS
NCLV	D1	Phase servo driven by frame sync	Phase servo is controlled by base counter
CRCQ	D0	SQDT output without SQOK	SQDT = CRCF during the rising time of S0S1

2) CNTL-S Control Register

This is a control register for the frame sync. Protection and attenuation.

FSEM	FSEL	Frame
0	0	2
0	1	4
1	0	8
1	1	13

WSEL	Clock
0	±3
1	±7

ATTM	MUTE	dB
0	0	0
0	1	–
1	0	–12
1	1	–12

3) CNTL-L, U Control Register

When the numbers of tract to be counted are inputed from a microcomputer, data load these registers.
(See tracking counter)

4) CNTL-W Control Register

This is a control register for CLV-Servo.

		Data = 0	Data = 1	Comments
COM	D3	XTFR/4 & PBFR/4	XTFR/4 & PBFR/4	Phase comparative frequency during PHASE-mode
WB	D2	XTFR/32	XTFR/16	Bottom hold period during SPEED and HSPEED-mode
WP	D1	XTFR/4	XTFR/2	Peak hold period during SPEED-mode
GAIN	D0	– 12dB	0dB	SMPD gain during SPEED & HSPEED-mode

5) CNTL-C Control Register

This is a control register for CLV-Servo.

Mode	D7 ~ D4	D3 ~ D0	SMDP	SMSD	SMEF	SMON
Forward	1 1 1 0	1 0 0 0	H	Hi-Z	L	H
Reverse		1 0 1 0	L	Hi-Z	L	H
SPEED		1 1 1 0	SPEED mode	Hi-Z	L	H
HSPEED		1 1 0 0	HSPEED mode	Hi-Z	L	H
PHASE		1 1 1 1	PHASE mode	PHASE mode	Hi-Z	H
XPHSP		0 1 1 0	SPEED, PHASE mode	Hi-Z or PHASE mode	L or Hi-Z	H
VPHSP		0 1 0 1	SPEED PHASE mode	Hi-Z or PHASE mode	L or Hi-Z	H
STOP		0 0 0 0	L	Hi-Z	L	L

TRACKING COUNTER

This counter is used to improve track-jumping characteristics. The number of tracks that are to be jumped are loaded into either register CNTL-L or CNTL-U. After either register CNTL-L or CNTL-U have been loaded and at the rising **edge of the next MLT, TRCK pulse count begins. If register CNTL-L = register = CNTL-U = 0, then n = 256n is load**ed into the register, and when the address is set in CNTL-L, the signal ($\overline{\text{COMPLETE}}$) is output from pin SENS at high level until the "n"th pulse and then at low level for succeeding pulses. When the address is set in CNTL-U, the signal ($\overline{\text{COUNT}}$) TRCK/2n is output. Fig. 7 shows the timing of the tracking counter.

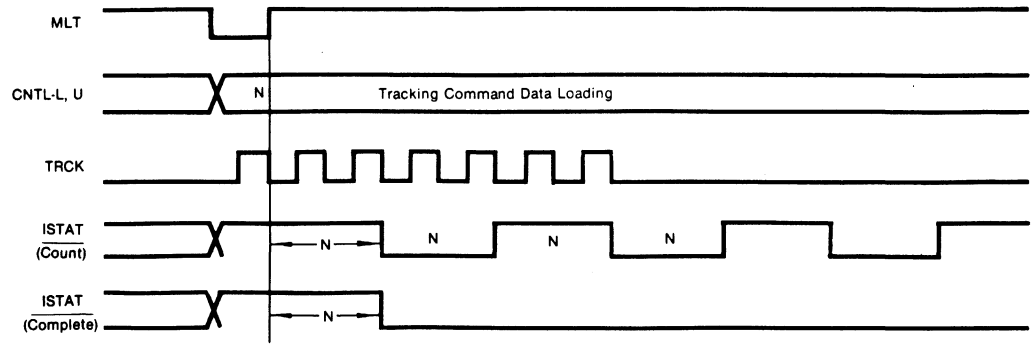


Fig. 7 Tracking Count Timing Chart

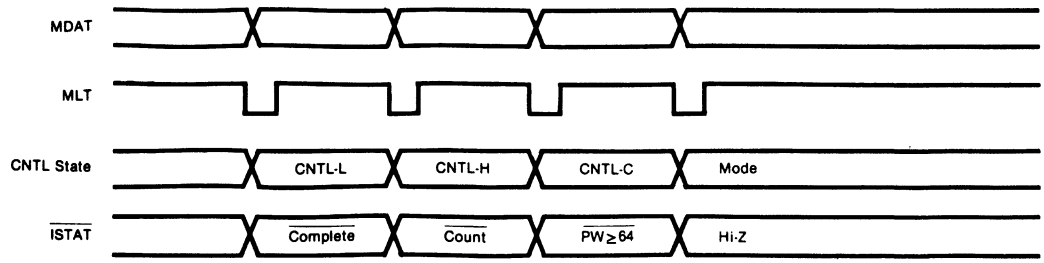
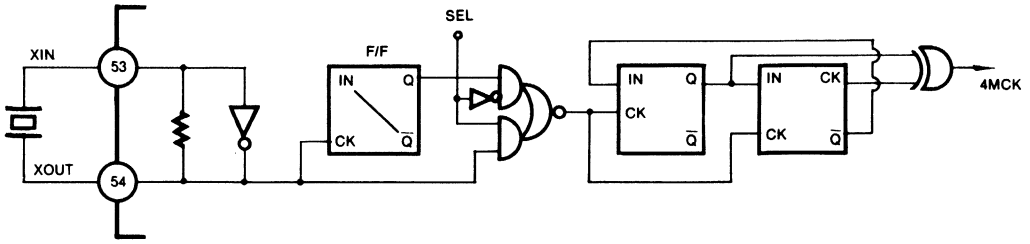


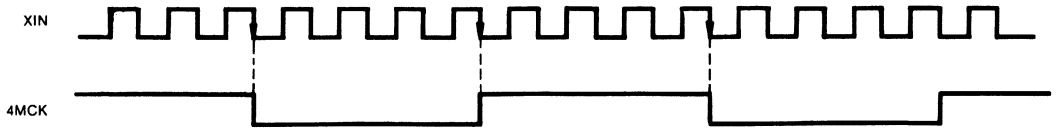
Fig. 8 $\overline{\text{ISTAT}}$ Output Signal by CNTL Register

X'TAL OSCILLATION

1) Block Diagram



2) Timing Chart (SEL = 0) in Use f = 16.9344MHz X'tal OSC.



3) Timing Chart (SEL = 1) in use f = 8.4672MHz X'tal OSC.

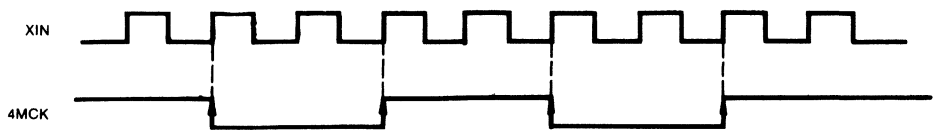


Fig. 9

DIGITAL FILTER

KS5990 is built-in 17th FIR Digital Filter.
The digital filter consists of RAM, multiplier, serial to parallel and parallel to serial converter and controller.

1) Block Diagram

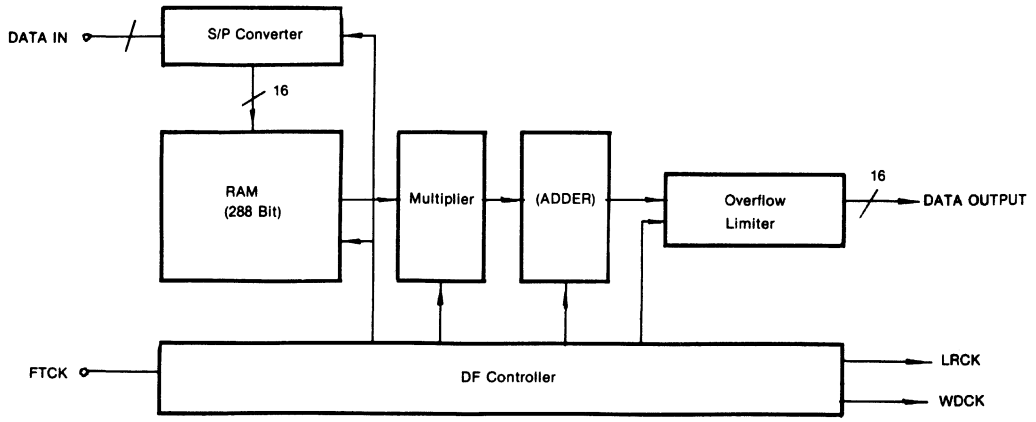


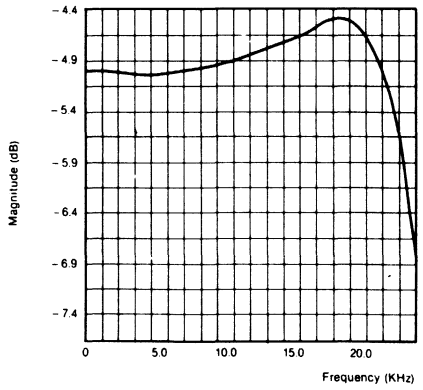
Fig. 10

2) Specification

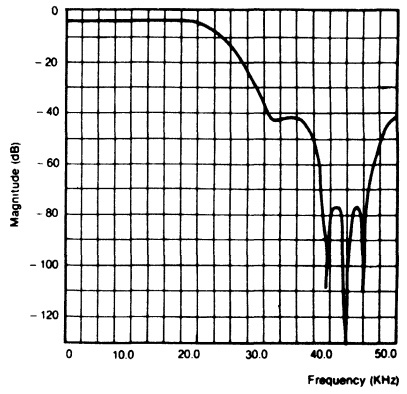
	DC through 18KHz ripple 20KHz of attenuation against 1KHz	±0.07dB max 0.65dB max
	44.1±1KHz attenuation against 1KHz 44.1±5KHz attenuation against 1KHz 44.1±10KHz attenuation against 1KHz 44.1±20KHz attenuation against 1KHz −30dB frequency range against 1KHz −60dB frequency range against 1KHz	87dB min 58dB min 44dB min 10dB min 44.1±14KHz 44.1±4KHz

3) Frequency Characteristic

A. Ripple Characteristic Graph



B. Low Pass Filter Frequency Characteristic Graph



EFM BLOCK

The EFM Block is made up of an EFM Demodulator which demodulates the EFM data inputted from a recorded disc, EFM Phase Detector, Frame Sync Detector/Protector/Inserter, Subcode Sync Detector, and Controller for the EFM Block.

1) EFM Phase Detector

As the EFM signal inputted from the disc contains a 2.16 MHz component, a 4.32 MHz bit clock is generated to detec the phase of the signal. The PBCK outputs the result to the PHAS terminal after detecting the phase on the edge of the EFM signal. The relationship between the EFM signal and the PBCK is explained in the following Timing Chart.

A. In normal operation

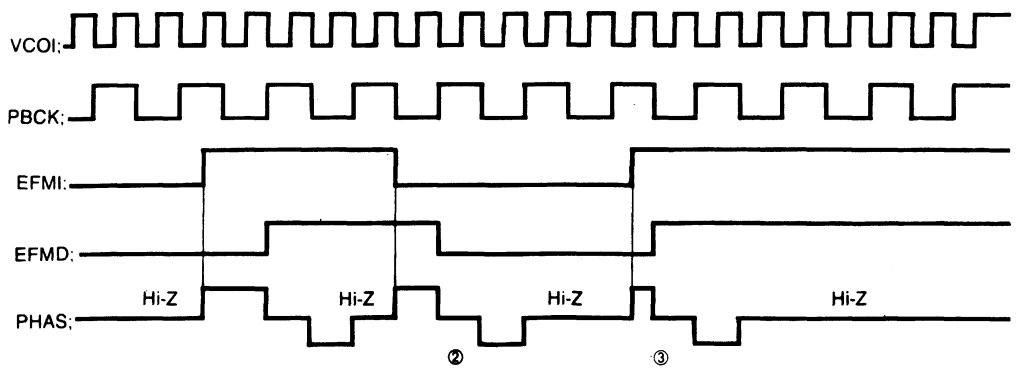


Fig. 11 EFM Phase Detection Timing Chart

Case ① : When the EFM signal is slower than the VCO
Case ②: When the EFM signal is locked up the VCO
Case ③: When the EFM signal is faster than the VCO

B. In abnormal operation

When the HIPD of CNTL-Z is chosen as 'L' from M-COM, the detector of the EFM phase operates as in Fig. 11 When the HIPD is 'H' and the time 'L' of LKFS is below 3.5T, against a PBFS period T, it outpputs Hi-Z to the PHAS terminal as long as "L". When it is above 3.5T, it outputs Hi-Z as long as 3.5T.

2) EFM (Eight to Fourteen) Demodulator

The modulated 14 bit Data is inputted from a disc, then it is inputted into a NRZ-I circuit. As the EFM Data passes by the NRZ-I circuit which converts 14 bit data into 8 bit data, it gets demodulated as 8 bit data. There are two kinds of demodulated data: subcode and PCM data. The subcode data is inputted into the subcode Block, and the PCM Data is written into 16KSRAM by, with both CE and WE signals.

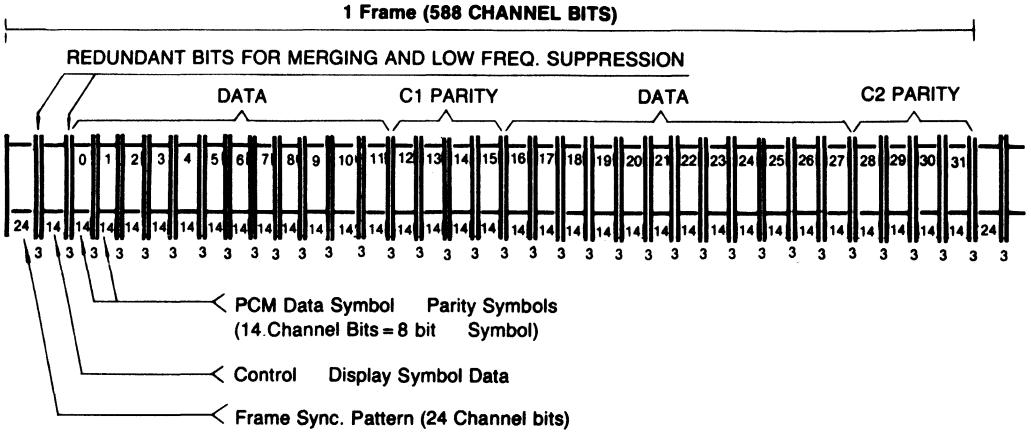
3) Frame Sync Detector/Inserter/Protector

A. Frame Sync Detector

CDP data are composed of units of a frame. A frame is made up of Frame Sync, Subcode Data, PCM Data, and Redundancy Data. A Frame sync is detected per frame against this format.

B. Frame Sync Protector/Inserter

There are cases in which the Frame Sync is left out or detected from the data beside the frame sync because of the effects of an error on the disk or Jitter. In this case the frame sync needs to be protected and inserted. To protect the frame sync, a window is made by the use of a WSEL signal of CNTL-S Reg. The frame sync which comes into the window is true data, and the frame sync deviating from the window is disregarded.



(Frame Format)

The width of the window is determined by the WSEL signal from the CNTL-S Reg. (cf. CNTL-S) being inserted in the frame When the frame sync reaches the number of a frame designated by the FSEM and FSEL, using the CNTL-S Reg, ULKFS becomes 'L' and the frame sync protection window is disregarded. In this case, an outputted frame sync is unconditionally accepted. After the frame sync is received, the ULKFS signal becomes 'H' and accepts a frame sync detected inside the window.

LKFS	ULKFS	Explanation
I	I	When a play back frame sync coincides with a generated frame sync.
O	I	① When a PBFR sync is detected in the window chosen by WSEL even if a play back frame sync does not coincide with a generated frame sync ② In the case of sync insertion, when PBFR sync does not coincide with a XTER sync and a frame sync within the window chosen by WSEL is not detected.
O	O	①After inserting a sync as many as times the number of frames decided by the FSEM and FSEL by the CNTL-S Reg., because Frame Sync is not detected within a window. ②When PBFR sync is not continuously detected after situation ① happens.

SUBCODE BLOCK

The 14 bit subcode sync signal S0, S1 is outputted to the Subcode Sync Block. In a frame delay after the output of S0, S1 is outputted. In this case, the signal of S0 + S1 is outputted through the S0S1 terminal, and the signal of S0·S1 is outputted through the SDAT terminal, when the signal S0S1 becomes 'H'. After the 14 bit Subcode Data inputted to the EFMI terminal has the EFM demodulated, an 8-bit P, Q, R, S, T, U, V, W subcode datum is outputted to SDAT by SBCK clock after it syncronizes with the signal PBFR. Only Q data are chosen among the 8 subcode data, and it is loaded on to 80 shift registers. The CRC-checked results of the loaded data is synchronized with the S0S1 rising edge, and is outputted to the SQCK terminal.
If the result of CRC checking is an error, 'L' is outputted to the SQCK terminal. If it is true, 'H' is outputted to the SQOK terminal. If the CRCD of CNTL-Z mode is 'H', the result of CRC checking is outputted to the SQDT terminal from the S0S1 section 'H' to the period of the SQCK falling edge.
The timing chart of a subcode block is as follows:

1) In SQEN = 'L': SDAT, SQDT, S0S1, SQOK, VCOI Timing Relation

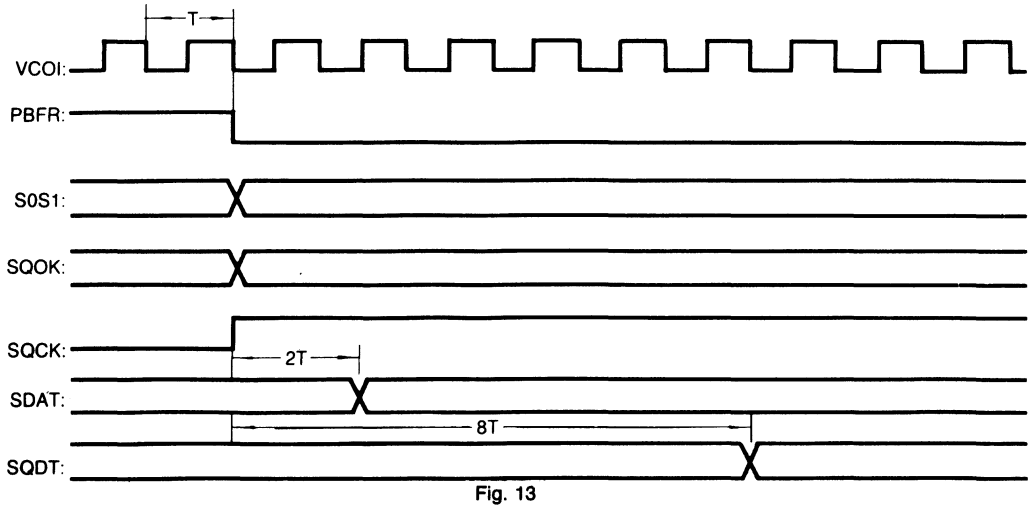


Fig. 13

2) In SQEN = 'L': SQOK, SQDT, S0S1, Timing Chart

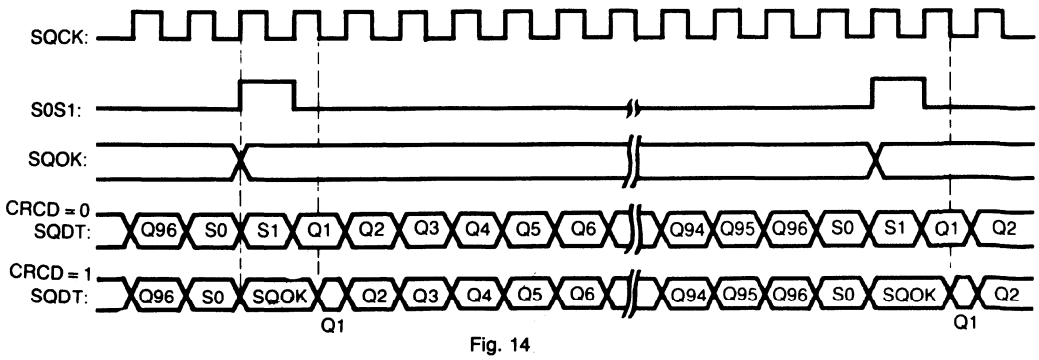
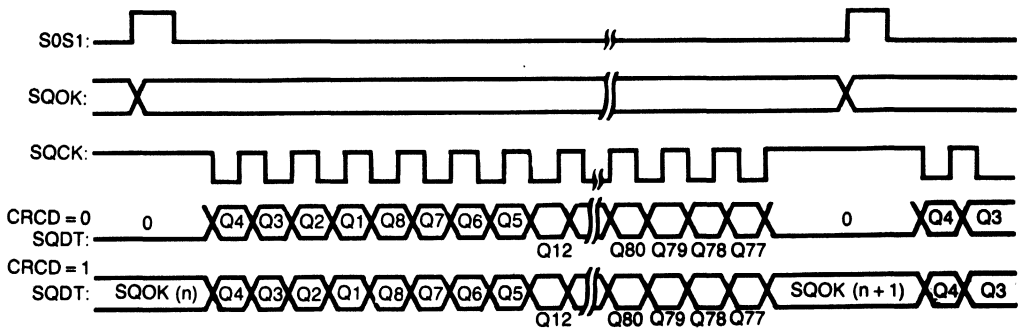


Fig. 14

3) In SQEN = 'H': SQOK, SQDT, S0S1, SQCK Timing Chart



Comment: When a SQOK of subcode Q Data is 'H', subcode data is outputted to SQDT according to SQCK. When SQOK is 'L', 'L' is outputted to the SQDT terminal.

Fig. 15

4) VCO1, SDAT, SBCK Timing Chart

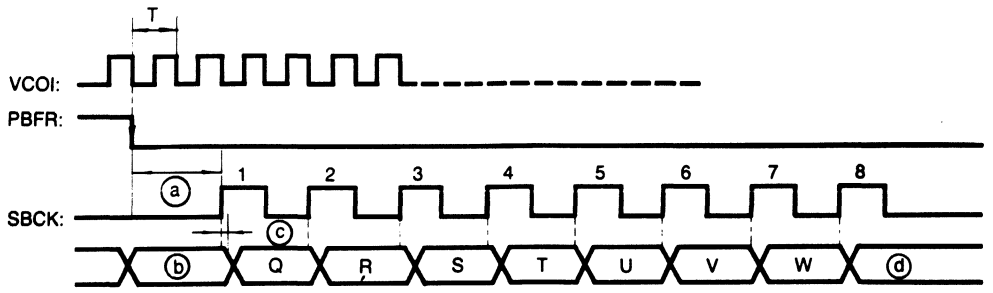


Fig. 16

ⓐ : SBCK is set to "L" for about 10μS after PBFR becomes a falling edge.

ⓑ : When S0S1 is 'L', a subcode P is outputted. When S0S1 is 'H', S0S1 is outputted.

ⓒ : When a cycle of VCO1 is 'T', the width of ⓒ is 4T ~ 6T.

ⓓ : When the pulse inputted to the SBCK terminal is above 7, subcode data P, Q, R, S, T, U, V, W data are repeated.

ECC (Error-Correction Code) Block

The function of ECC Block is to recover damaged data to some extent when data on a disk is damaged. By using CIRC (Crossed-Interleave Reed-Solomon Code), C1 (32, 28) and C2 (28, 24) errors are corrected. ECC is performed with an 8-bit as a symbol unit. In correcting C1, a C1 Pointer is generated, and in correcting C2, a C2 pointer is generated. C1, C2 Pointers send error information or the data to which ECC is given. After correcting C2, against uncorrectable data, Error Data is sent by outputing a C2 Flag.
The signal C2FL is AND signal of C2F1 and C2F2. By using this information, Data is treated in the interpolator block.

C1F1	C1F2	C1, C2 Error	C2F1	C2F2	C2FL
0	0	No Error	0	0	0
0	1	Single Error	0	1	0
1	0	Double Error	1	0	0
1	1	Irretrievable Error	1	1	1

Fig. 17

C1F1, C1F2 — Output the state of an error correction by C1 Decoder

C2F1, C2F2 — Output the state of an error correction by C2 Decoder

C2FL — Becomes 'L' when an error correction by C2 Decoder is possible and an 'H' error correction is impossible.

16K SRAM BLOCK

After EFM demodulation of EFM modulated data inputted from disc, when the data is written into RAM is outputted to Read/Write and D/A Converters in ECC Processing for reading a SRAM Address Generator and a 16K SRAM is installed. SRAM terminal must be 'H' in a 16K SRAM application.

1) Address Generation Priority Control

Writing in EFM demodulation, reading the data with R/W, and a D/A Converter in the ECC process are sometimes required at the same time.
When 3 signals are demanded at the same time, priority of the data process needs to be controlled. Priority is D/A Converter Read demand > EFM Write demand > ECC R/W demand.

2) EFM Demodulation Data Write Demand

EFM demodulated data must be written to SRAM. Priority is controlled when the write demand signal is transmitted to the SRAM Address Generator, and the Enable signal is transmitted to the EFM Block. The generated address is transmitted to the SRAM Interface circuit.
A generated address is data in which deinterleave is considered, and a frame 32 address is generated.

A. In the use of 16K SRAM (in EFM & ECC Write): SRAM terminal 'H'

DB1 ~ DB8 and AD1 ~ AD11 terminals are in a state of Hi-Z. $\overline{CE}$ and $\overline{WE}$ are 'Don't Care.'

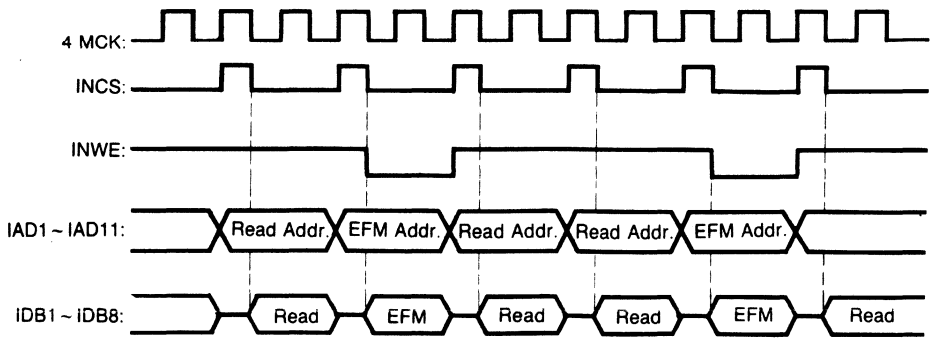
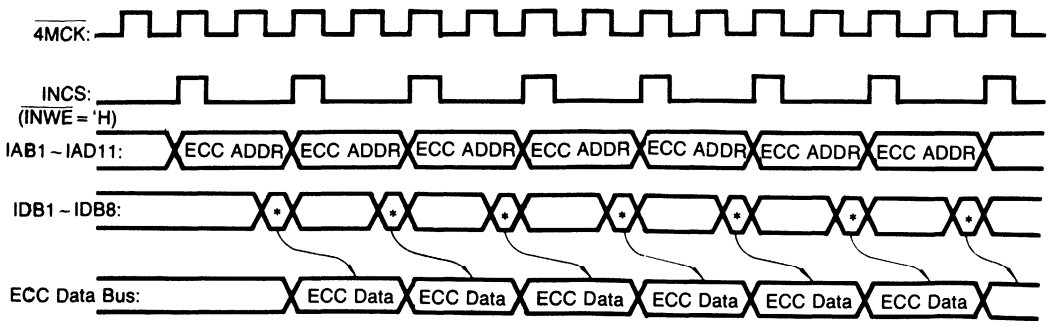


Fig. 18

3) R/W Demand of ECC Data

For C1 and C2, ECC treatment is 129 times of the Address demand signals generated, due to an R/W operation, and must be given to 64 PCM data and 65 Pointers during a frame.
The write of FCC processing is the same as 2) an EFM Write operation.
In reading, it is as follows:

A. In the use of 16K SRAM Reading Timing (SRAM: H)



*: Valid ECC Data

Fig. 19

4) D/A Converter Read Demand

Since each 6 sampling data on the left and right channel and 12 C2 Pointer data must be read for a frame, 36 read enable demand signals are caused. The timing chart for a D/A Converter Read is the same as the R/W demand block of ECC data. As a result, the number of the maximum R/W operation action demanded for a frame is 179.

5) Address Generated Block

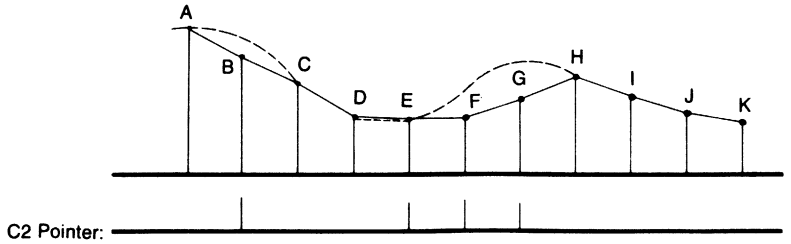
The interleaving data in encoding is deinterleaved in decoding. The data of 108 frames is needed to get 8 frames of PCM data in a CDP format. To get data suitable for a CDP format, 2 counters are needed. A write base counter is used to write. EFM demodulation data are hindered in storing data in SRAM due to disk shaking, the instability of a servo system, etc.

6) Jitter Margin

EFM demodulation data are hindered in storing data in SRAM due to disk shaking, the instability of a servo system, etc. Now that the data that must be kept is limited by the size of SRAM in view of time, data is destroyed if the value of the read/write base counter has a difference above ± 5 frames. Loading into the value of the write base counter with enforcement, the value of read the base counter has a jitter margin below ± 4 frames when there is a difference of over ± 5 frames in the read/write base counter value.
A read base counter value is loaded into a write base counter with enforcement when data on the left and right channels are all muting, or when NCLV is 'H' and CLV-Servo is stop, forward or reverse. When the difference between the read/write base counter is above ± 4 frame, a 'H' signal is outputted to the JIT terminal for a period.

INTERLEAVE, MUTE BLOCK

When a burst error occurs on a disk, sometimes the data can't be corrected even if a ECC process is conducted. An interpolator block revises data by using a C2 Pointer outputted through the ECC Block. PCM data inputted to a data bus are inputted to the left and right channels, respectively, in the order of 8-bit C2 Pointer, Lower 8-bit, and Upper 8-bit. A pre-hold method is taken when a DA Flag is 'H' continuously. In case of the occurrence of a single error, a mean value interploating method is carried out with the range of the PCM Data before and after an error happens. When a check against a checked cycle is 'L', R-CH Data is outputted. L-CH Data is outputted when the check is 'H'. For the timing chart of an interpolator block see figure 6.



$B = \frac{A+C}{2}$: Mean value interpolation

F = E = D : Pre-hold interpolation

G = F + H : Mean value interpolation

Fig. 20

2) Mute and Attenuation

By using a Mute terminal and the ATTM signal of the CNTL-S Reg., AUDIO data is muted or reduced. There are two kinds of mute: zero-cross muting and muting.

A. Zero-Cross Muting
Audio data is muted when a mute terminal is 'H' and when 6 bits in a high position of Audio Data are all 'H' or 'L'.

B. Muting
Audio data is muting when ZCMT of the CNTL-Z Reg. is 'L' and when a mute terminal is 'H'.

C. Attenuation
By means of the ATTM signal of the CNTL-S Reg. and the signal of the Mute terminal, an audio signal attenuation occurs as the following.

ATTM	MUTE	Degree of Attenuation
0	0	0 dB
0	1	$-\infty$ dB
1	0	– 12 dB
1	1	– 12 dB

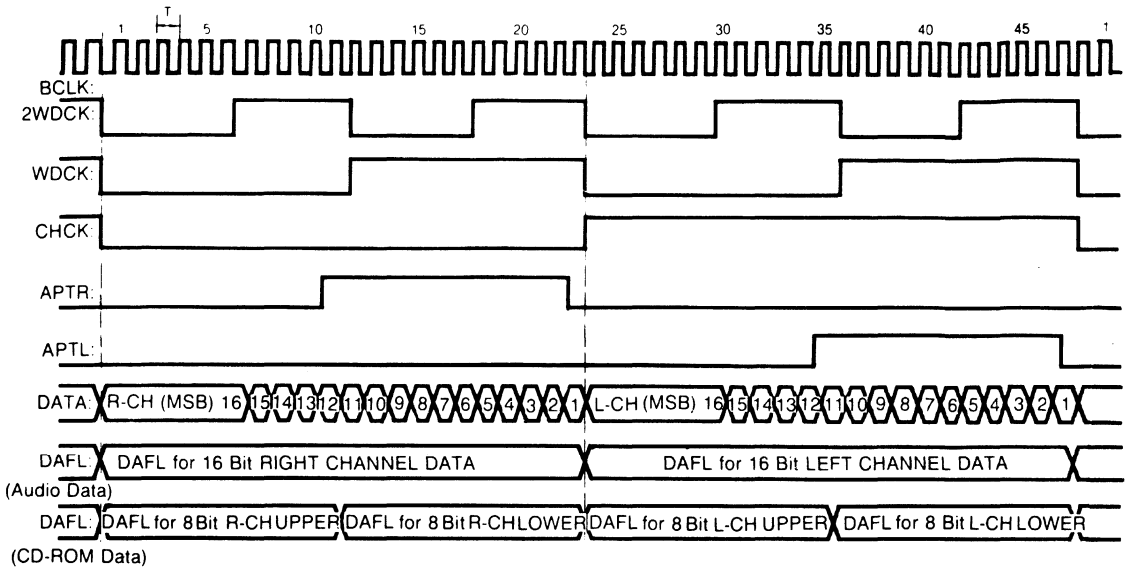


Fig. 21. When Sel. 5 is 'L', and DF is off, the Timing Chart of PCM Data

CLV SERVO

CNTL-C Reg. is selected to control CLV Servo by the Data inputted from μ-COM. In CNTL-C Reg, the data from μ-com appoints CLV servo action mode and controls the spindle motor.

1) Forward

The states of output terminal, related to the mode that rotates a spindle motor forward, are SMDP = 'H', SMSD = Hi-Z, SMEF = 'L' and SMON = 'H', respectively.

2) Reverse

The modes to rotate a spindle motor reversly are SMDP = 'L', SMSD = 'Hi-Z', SMEF = 'L', and SMOD = 'H'.

3) SPEED-Mode

The SPEED-Mode is the mode for the rough control of a spindle motor when a track is jumps or a EFM phase is unlocked. If a cycle of VCO is 'T', the pulse width of a frame sync is '22T'. Sometimes an EFM signal is above 22T, due to noises on a disc, etc. A correct frame sync cannot be detected when the signal is not removed. In this case, the pulse width of an EFM signal is detected at a cycle of XTFR/2 or XTFR/4, which are peak hold clocks. The pulse width an of EFM signal is detected at a cycle of XTFR/16 or XTFR/32, which are bottom hold clocks. The value detected is used for a frame synchronization signal. When the frame synchronization signal is smaller than 21T, the SMPD terminal outputs 'L'. When it is 22T, Hi-Z is outputted. 'H' is outputted when it is above 23T.
When the GAIN signal of CNTL-W Reg. is 'L', the SMDP terminal is outputted after being attenuated at – 12dB. When the signal is 'H', the terminal is outputted without any attenuation. <cf. figure 22>
In SMSD, SMEF, and SMON terminals Hi-Z, 'L', and 'H' are outputted.

4) HSPEED-Mode

The rough servo mode, which moves 20,000 tracks in high speed, acts between the inside of the CD and the outside of the CD. In the domain of a mirror of the track without, a pit EFM and the signal of 20KHz overlap. In this case, since in a speed-mode the peak range of a longer mirror signal than the original frame sync is detected, a servo operation becomes unstable. In HSPEED-mode, a peak hold uses a 8.4672/256 MHz signal, and a bottom hold removes a mirror component and stabilizes the high speed servo operation by using an XTFR/16 or XTFR/32 period signal.
In SMSD, SMEF, and SMON terminals, Hi-Z, 'L', and 'H' are outputted.

5) PHASE-Mode

A PHASE Mode is the mode that control an EFM Phase. When NCLV of CNTL-Z is 'L', it detects a phase difference between PBFR/4 and XTFR/4, and when NCLV is 'H', it detects the phase difference between Read base Counter/4, and write base Counter/4, and then outputs to the SMPD terminal. See figure 8.
If the VCO/2 signal cycle is put as 'T' and the PBFR, during a 'H' period, as a V_{pb}, it outputs 'H' to a SMSD terminal from the falling edge of PBFR for $(W_{pb}\text{-}278T) \times 32$, and later outputs 'L' to the falling edge of PBFR. Refer to figure 24

6) XPHSP-Mode

A XPHSP mode is the mode used in normal operation. It samples a LKFS signal made in the frame sync block at a cycle of PBFR/16. After sampling 'H', DHASE mode is carried out. When 'L' is sampled continuously 8 times, it goes over to speed-mode. CNTL-W Reg. decides the choice of the peak hold of the speed-mode, the bottom hold cycle of SPEED-and HSPEED-Mode, and the choice of a gain.

7) VPHSP-Mode

A VPHSP-Mode is the mode used for rough servo control. It uses VCO instead of X'tal in the EFM pattern test. When the range of VCO center changes, VCO is easily loaded because the rotation of a spindle motor changes in the same direction.

8) STOP

Stop is the mode used to stop a spindle motor.
SMDP = 'L', SMSD = Hi-Z, SMEF = 'L', SMON = 'L'

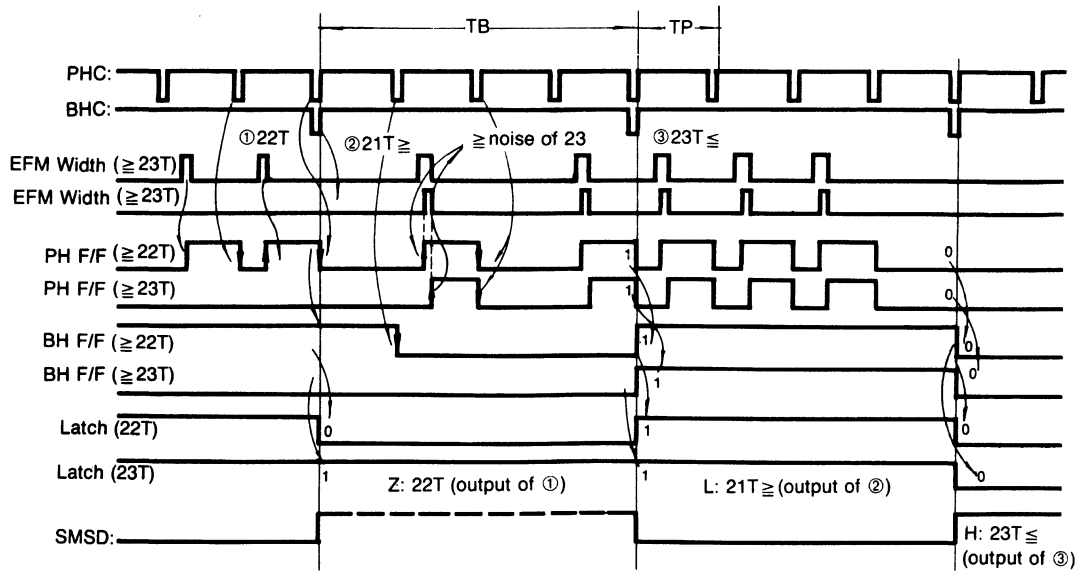


Fig. 22 When gain is 'H' in a speed-mode Timing Chart of SMSD output

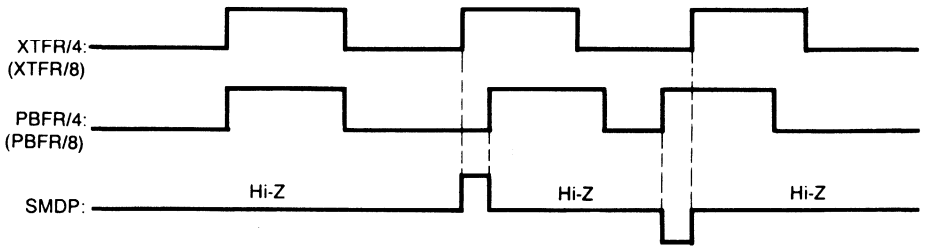
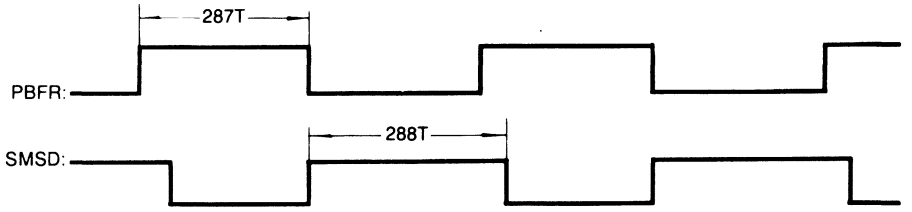
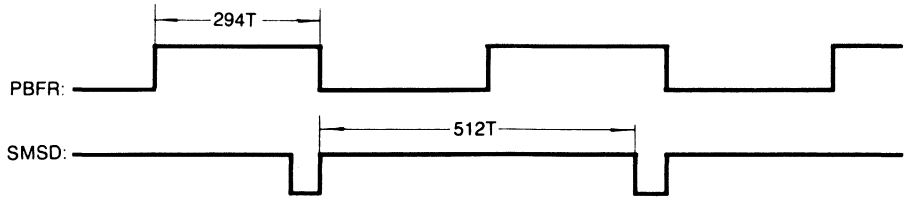


Fig. 23 Output Timing Chart of a SMDP terminal



(a) When PBFR is 287T, Timing Chart of SMSD output

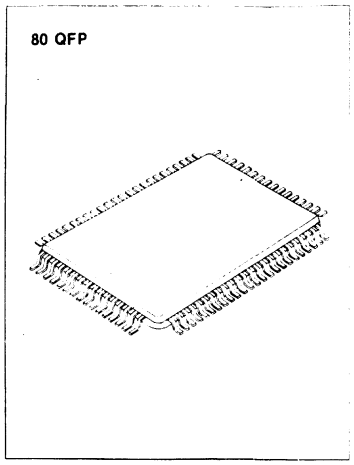


(b) When PBFR is 294T, Timing Chart of SMSD output

Fig. 24 In a PHASE Mode Timing Chart of SMSD output (T: VCO/2)

DIGITAL SIGNAL PROCESSOR

The KS5991 is a CMOS integrated circuit designed for compact disc player application. It consists, of 16KSRAM, digital filter and digital signal processing circuits, and is suitable for headphone stereo CDP.



FEATURES

- **All digital signals for regeneration are processed using one chip.**
- **Internal aperture compensation digital filter**
- **EFM-PLL circuit for bit clock regeneration**
- **EFM data demodulation**
- **Frame synchronous signal detection and protection**
- **Compensation using mean value and prior value retention**
- **Subcode signal demodulation subcode Q detection**
- **CLV servo for spindle motor**
- **8-bit tracking counter**
- **CPU interface with serial bus**
- **Subcode Q register**
- **Built-in 17th digital filter**
- **Built-in 16KSRAM**
- **80-Quad, flat package type**
- **Operating supply voltage: V_{DD} = 3.0V ~ 4.0V**

ORDERING INFORMATION

Device	Package	Operating Temperature
KS5991	80 QFP	−20°C ~ +75°C

BLOCK DIAGRAM

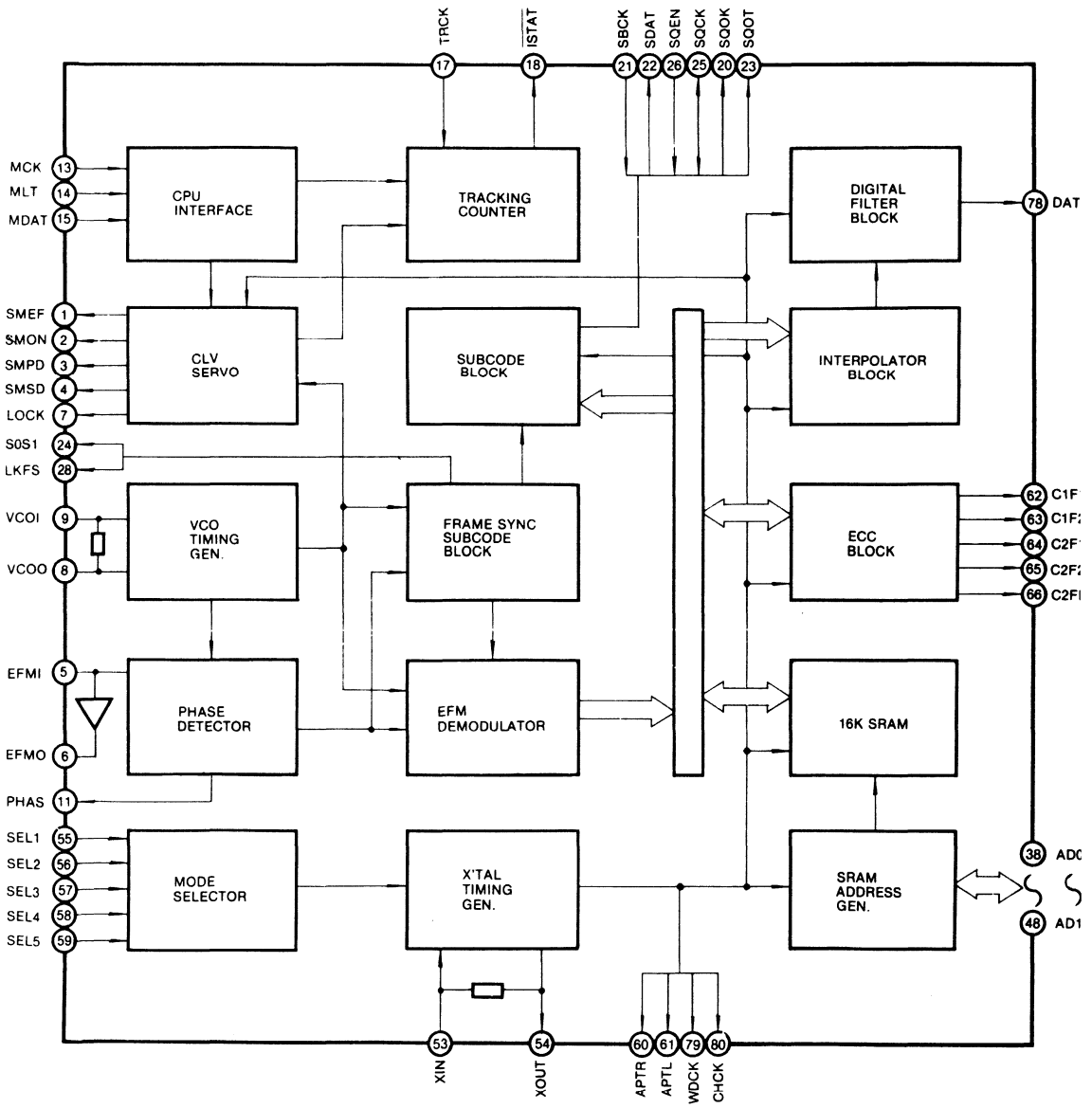


Fig. 1

PIN CONFIGURATION

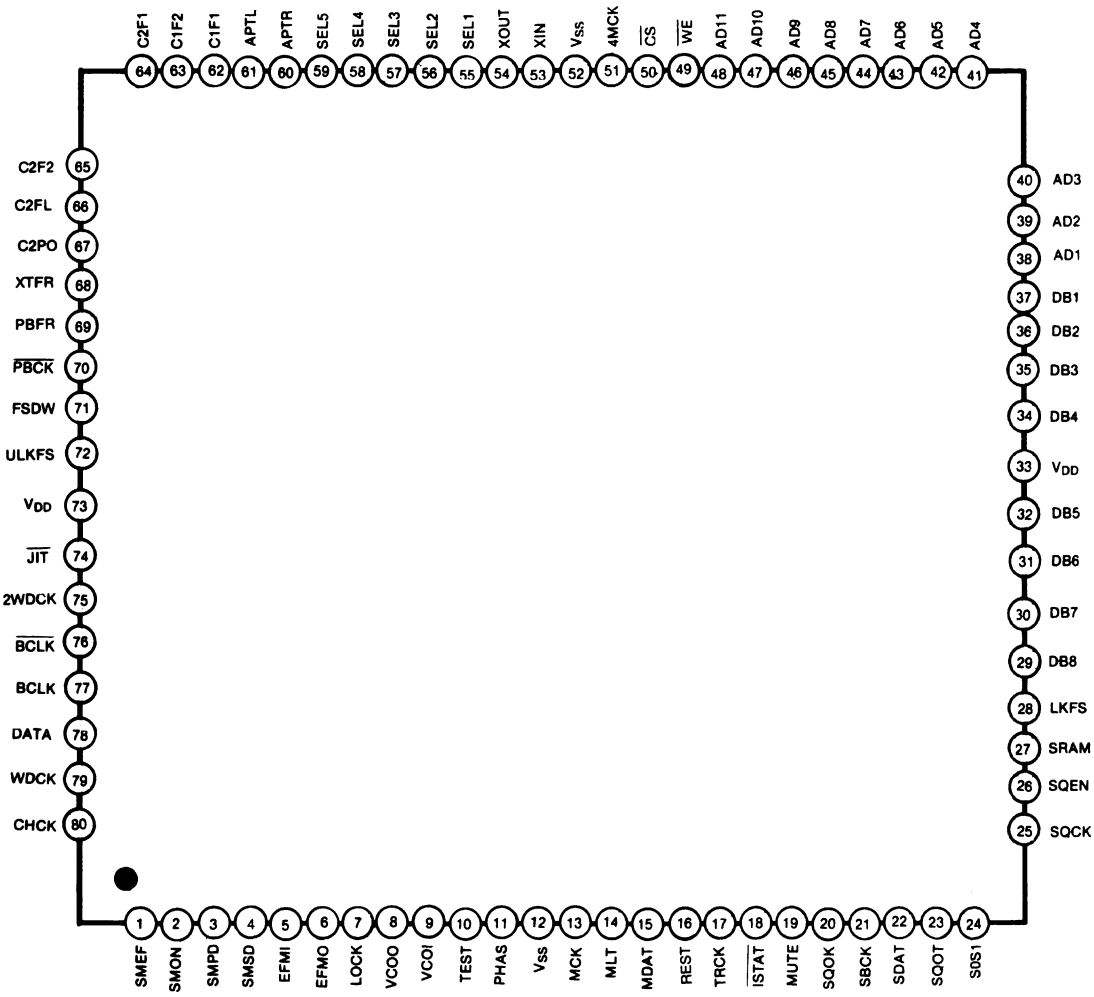


Fig. 2

PIN DESCRIPTION

Pin No	Symbol	I/O	Description
1	SMEF	O	Pin 1 output is switched constant when the output filter of the spindle motor is energized.
2	SMON	O	ON/OFF control for spindle motor.
3	SMPD	O	Spindle motor drive. Provides rough control during CLV-S mode and phase control during CLV-P mode.
4	SMSD	O	Spindle motor drive. Controls speed during CLV-P mode.
5	EFMZ	I	EFM signal from RF amplifier.
6	EFMO	O	Controls slice level of the EFM signal.
7	LOCK	O	The output of pin 7 reflects the status of the GFS signal which is sampled at PBFR/16. when the GFS signals are "H", but, has remained "L" for at least 8 samples, the output of pin 7 is "L".
8	VCOO	O	VCO output. The frequency is f = 8.6436MHz, when locked by the DBFR signal.
9	VCOI	I	VCO input.
10	TEST	I	(0V).
11	PHAS	O	The output of Pin 11 provides phase comparison of the EFM signal and VCO/2.
12	V_{SS}	—	GND (0V).
13	MCK	I	Pin 13 provides the serial transmission clock from the CPU. Data is latched on the leading edge of the clock.
14	MLT	I	Pin 14 provides latch input from the CPU, and 8-bit shift register data (serial data received from the CPU) is latched in each of the registers.
15	MDAT	I	Serial data from the CPU.
16	REST	I	System reset ("L").
17	TRCK	I	Tracking pulse input.
18	ISTAT	O	Output reflecting the internal condition, as designated by the address.
19	MUTE	I	Muting input. MUTE is "L" when ATTM of internal register A is "L" (normal condition). MUTE is "H" when the muting condition is set.
20	SQOK	O	Outputs the results the CRC check of the subcode Q.
21	SBCK	I	Clock input for subcode serial output.
22	SDAT	O	Serial output of subcode.
23	SQDT	O	Output of subcode Q.
24	S0S1	O	Output of subcode sync S0 + S1.
25	SQCK	I/O	Clock for reading subcode Q.
26	SQEN	I	Input for selecting SQCK (L SQCK is output, H SQCK is input)
27	SRAM	I	SRAM is "H" in Normal, SRAM is "L" when system is testing.
28	LKFS	O	Display output for frame sync lock status.

PIN DESCRIPTION (Continued)

Pin No	Symbol	I/O	Description
29	DB8	I/O	Data pin for external RAM. DATA8 (MSB) in test mode. Hi-Z in normal
30	DB7	I/O	Data pin for external RAM. DATA7 in test mode. Hi-Z in normal
31	DB6	I/O	Data pin for external RAM. DATA6 in test mode. Hi-Z in normal
32	DB5	I/O	Data pin for external RAM. DATA5 in test mode. Hi-Z in normal
33	V_{DD}	—	Power supply (+5V).
34	DB4	I/O	Data pin for external RAM. DATA4 in test mode. Hi-Z in normal
35	DB3	I/O	Data pin for external RAM. DATA3 in test mode. Hi-Z in normal
36	DB2	I/O	Data pin for external RAM. DATA2 in test mode. Hi-Z in normal
37	DB1	I/O	Data pin for external RAM. DATA1 (LSB) in test mode. Hi-Z in normal
38	AD01	I/O	(LSB)
39	AD02	I/O	In normal mode (TEST = 'L', SRAM = 'H'), these pins are High impedance (Hi-Z) In test mode (TEST = 'H', SRAM = 'L'), these pins are Output address of external RAM
40	AD03	I/O	
41	AD04	I/O	
42	AD05	I/O	
43	AD06	I/O	
44	AD07	I/O	
45	AD08	I/O	
46	AD09	I/O	
47	AD10	I/O	
48	AD11	I/O	(MSB)
49	WE	I/O	In normal mode, this is WE output. In test mode, write enable input.
50	CE	I/O	In normal mode, this is CE output. In test mode, chip enable input.
51	4MCK	O	Divider output for crystal. f = 4.2336MHz
52	V_{SS}	—	GND (0V)
53	XIN	I	Input to crystal oscillator circuit. Depending on the mode, the frequency is either f = 8.4672 r 16.9344MHz.
54	XOUT	O	Output from crystal oscillator circuit. Depending on the mode, the frequency is either f = 8.4672 or 16.9344MHz.
55	SEL1	I	Mode selection input 1.
56	SEL2	I	Mode selection input 2.
57	SEL3	I	Mode selection input 3.
58	SEL4	I	Mode selection input 4. Code switch input for audio data output. 2's complement output when "L", and offset binary output when "H".
59	SEL5	I	Mode selection input 5. Code switch input for audio data output. Serial output when "L" and parallel output when "H".

PIN DESCRIPTION (Continued)

Pin No	Symbol	I/O	Description
60	APTR	O	Output for aperture compensation. "H" when R-ch.
61	APTL	O	Output for aperture compensation. "H" when L-ch.
62	C1F1	O	Monitor output reporting status of error correction for C1 decoder. When SEL5 = 'L', DA01 (LSB of parallel audio data) is output when SEL5 = 'H'.
63	C1F2	O	Monitor output reporting status of error correction for C1 decoder when SEL5 = 'L', DA02 is output when SEL5 = 'H'.
64	C2F1	O	Monitor output reporting status of error correction for C2 decoder when SEL5 = 'L', and DA03 is output when SEL5 = 'H'.
65	C2F2	O	Monitor output reporting status of error correction for C2 decoder when SEL5 = 'L', DA04 is output when SEL5 = 'H'.
66	C2FL	O	When SEL5 = 'L', output of status condition. C2FL is set 'H' when the C2 sequence, being corrected becomes impossible to correct. DA05 is output when SEL5 = 'H'.
67	C2PO	O	Display output of the C2 pointer when SEL5 = 'L', DA06 is output when SEL5 = 'H'.
68	XTFR	O	When SEL5 = 'L', output of read frame dock, which is 7.35KHz of the crystal system. DA07 is output when SEL5 = 'H'.
69	PBFR	O	When SEL5 = 'L', output of write frame clock, which is 7.35KHz when locked by the crystal system. DA08 is output when SEL5 = 'H'.
70	$\overline{\text{PBCK}}$	O	When SEL5 = 'L', output of VCO/2 (f = 4.3218MHz when locked by the EFM signal). DA09 is output when SEL5 = 'H'.
71	FSDW	O	When SEL5 = 'L', output for unprotected frame sync patterns. DA10 is output when SEL5 = 'H'.
72	ULKFS	O	Output for display of status of frame sync protection when SEL5 = 'L', DA11 is ouput when SEL5 = 'H'.
73	V_{DD}	—	Power supply (+5V).
74	$\overline{\text{JIT}}$	O	When SEL5 = 'L', output for display of either RAM overflow or underflow for +4 frame jitter absorption. DA12 is output when SEL5 = 'H'.
75	ZWDCK	O	When SEL5 = 'L', output for strobe signal (352.8KHz when DF is ON, 176.4KHz when DF is OFF). DA13 is output when SEL5 = 'H'.
76	$\overline{\text{BLCK}}$	O	When SEL5 = 'L', inverse output of BLCK. DA14 is output when SEL5 = 'H'.
77	BLCK	O	When SEL5 = 'L', bit clock output (4.2336MHz when DF is ON; 2.1168MHz when DF is OFF). DA15 is output when SEL5 = 'H'.
78	DATA	O	Serial data output of audio signal when SEL5 = 'L'. DA16 is output when SEL5 = 'H'.
79	WDCK	O	Strobe signal output. Output is 176.4KHz when DF is on. Output is 88.2KHz when DF is off.
80	CHCK	O	Strobe signal output. Output is 88.2KHz when DF is on. Output is 44.1KHz when DF is off.

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristics	Symbol	Value	Unit
Supply Voltage	V_{DD}	−0.3 ~ +7.0	V
Input Voltage	V_I	−0.3 ~ +7.0	V
Output Voltage	V_O	−0.3 ~ +7.0	V
Operating Temperature	T_{OPR}	−20 ~ +75	°C
Storage Temperature	T_{STG}	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(V_{DD} = 3.4V ± 10%, V_{SS} = 0V, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Input High Voltage	V_{IH1}	Note 1	0.7 V_{DD}		V_{DD}	V
Input Low Voltage	V_{IL1}	Note 1			0.3 V_{DD}	V
Input High Voltage	V_{IH2}	Note 2	0.8 V_{DD}			V
Input Low Voltage	V_{IL2}	Note 2			0.2 V_{DD}	V
Output High Voltage	V_{OH}	I_{OH} = −1mA	V_{DD} − 0.5		V_{DD}	V
Output Low Voltage	V_{OL}	I_{OL} = 1mA	0		0.4	V
Input Leakage Current	I_{LKG1}	V_{IN} = 0 ~ 5.5V	−5		+5	μA
Three-State Pin Output Leakage Current	I_{LKG2}	V_{OUT} = 0 ~ 5.5V	−5		+5	μA
SRAM Input Leakage Current	I_{LKG3}	V_{IN} = 0 ~ 5.5V	−5		+200	μA

Note 1. Related pins—EFMI, XRST, TEST, MUTE, SEL1 ~ 5, MLT, MDAT, SBCK, SQEN, SQCK
Note 2. Related pins—CNIN, MCK.

2. AC Characteristics

A. XIN Pin, VCOI Pin

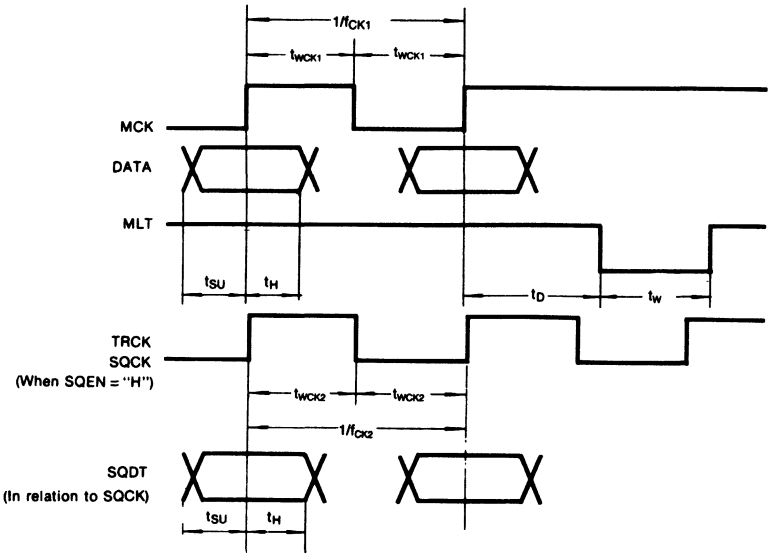
(1) When pulse is applied to XIN and VCO, $V_{DD} = 3.4V \pm 10\%$, $V_{SS} = 0V$, and $Ta = 25°C$, unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
"H" Level Pulse Width	t_{WHX}	20			ns
"L" Level Pulse Width	t_{WLX}	20			ns
Pulse Frequency	t_{CK}	55			ns
Input "H" Level	V_{IH}	$V_{DD} - 1.0$			V
Input "L" Level	V_{IL}			0.8	V
Rising Time Breaking Time	t_R			15	ns

B. Pins MCK, DATA, MLT, TRCK, SQCK

($V_{DD} = 3.4V \pm 10\%$, $V_{SS} = 0V$, $T_{OPR} = -20$ to $+75°C$)

Item	Symbol	Min	Typ	Max	Unit
Clock Frequency	f_{CK1}			1	MHz
Clock Pulse Width	f_{WCK1}	300			ns
Setup Time	t_{SU}	300			ns
Hold Time	t_H	300			ns
Delay Time	t_D	300			ns
Latch Pulse Width	t_W	300			ns
CNIN SQCK Frequency	f_{CK2}			1	MHz
CNIN SQCK Pulse Width	t_{WCK2}	300			ns



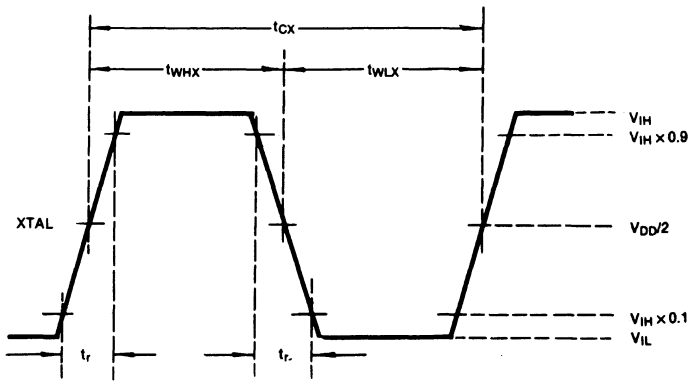
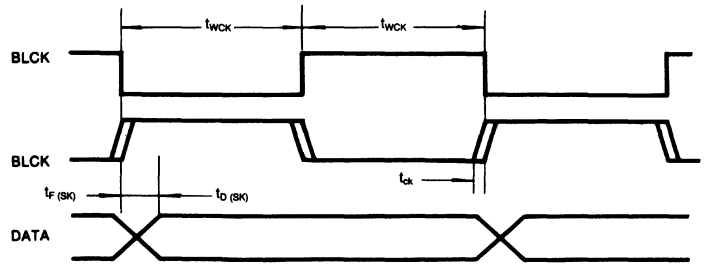


Fig. 3

C. DAC Interface (V_{DD} = 3.4V ± 10%, V_{SS} = 0V, T_{OPR} = −20 ~ 75°C, C_L = 50pF)

Item	Symbol	DF is OFF			When DF ON			Unit
		Min	Typ	Max	Min	Typ	Max	
Clock Pulse Width	t_{WCK}		236			118		ns
Clock Skew (Fast)	t_{FCK}			40			40	ns
Data Skew (Fast)	$t_{F(SK)}$			0			0	ns
Data Skew (Delay)	$t_{D(SK)}$			80			80	ns



*Note: CHCK, WDCK, APTR, APTL
DA01 through DA16 during parallel DA conversion or C1F1, C1F2, C2F1, C2F2, C2FL, C2PO, XTFR, 2WDCK, DATA during serial conversion.

Fig. 4

APPLICATION INFORMATION
FUNCTION DESCRIPTION

MODE SELECTOR

To control several blocks in KS5991, there are 5 selecting pin signals. Table 1. Shows selected mode by these signals.

Input Pins					Function*				
SEL1	SEL2	SEL3	SEL4	SEL5	XIN	DF	P/S	OB/2'S	CD ROM/Audio
0	1	0	0	0	16M	ON	S	2'S	Audio
0	1	0	1	1	16M	ON	P	OB	Audio
0	1	1	0	0	16M	OFF	S	2'S	Audio
0	1	1	1	1	16M	OFF	P	OB	Audio
1	0	0	0	0	8M	ON	S	2'S	Audio
1	0	0	1	1	8M	ON	P	OB	Audio
1	0	1	0	0	8M	OFF	S	2'S	Audio
1	0	1	1	1	8M	OFF	P	OB	Audio
1	1	1	1	0	8M	OFF	S	2'S	CD ROM

Table 1. Mode Selection

* Note: • 8M/16M: Selection of either the XIN or XOUT clocks will provide either a 8.4672MHz or 16.9344MHz signal.
  • DF: Digital Filter
  • P/S: Parallel mode/serial mode
  • OB/2'S: Offset

- Clock selection
  Selectioin of an 16.9344MHz or 8.4672MHz oscillator clock is possible at pins XIN and XOUT. However only 16.9344MHz clocks are provided for digital out usage.

- Digital filter selection
  When the digital filter function is switched to ON, all signals on the DAC interface are handled at twice the normal speed.

- Parallel/Serial output selection
  When the output is parallel, 16-bit parallel data is output from pins DA01 through DA16.
  When the output is serial, the following signals are output at pin DA01 through DA16.

DATA (DA16)	Serial data output (MSB or LSB first output)
BLCK (DA15)	Internal system clock (with DF ON, 4.2336MHz, and with DF OFF, 2.1168MHz)
$\overline{\text{BLCK}}$ (DA14)	Bit clock (BLCK inversion signal)
2WDCK (DA13)	4X multiplied CHLK signal
$\overline{\text{JIT}}$ (DA12)	Jitter Margin Overflow/Underflow signal
ULKFS (DA11)	Display output of frame sync protection status
FSDW (DA10)	Unguarded (unprotected) frame sync signal
PBCK (DA09)	Signal at 1/2 V_{CO} pin cycle times. When locked 4.3218MHz.
PBFR (DA08)	Write Frame Clock signal. When locked 7.35KHz.
XTFR (DA07)	Read Frame Clock signal. Crystal system 7.35KHz.
C2PO (DA06)	C2 Pointer signal
C2FL (DA05)	Correction mode output, C2FL = C2F1, C2F2
C2F2 (DA04) C2F1 (DA03)	Monitor Output of Error Correction Mode for C2 Decode
C1F2 (DA02) C1F1 (DA01)	Monitor Output of Error Correction Mode for C1 Decode

- OFFSET Binary/2's Complement Selection
  When pin SEL4 is at "H" output occurs at OFFSET BINARY; when it is at "L", output occurs at 2's complement.
- CD-ROM/AUDIO Selection
  When SEL1 = SEL2 = SEL3 = "H", CD-ROM is selected. Then the C2 pointer is output with each byte (8 bits), and neither the mean value interpolation nor the preceding value hold are exercised. That is, if an error occurs in the upper 8 bits of a 16-bit data, only the C2 pointer related to those upper 8 bits switches to "H" while the lower 8 bits are handled as correct data.

Microcomputer Interface

Data from the microcomputers are inputed through the MDAT pin by MCK which is the clock signal of the microcomputers, and the pulse signal through the MLT pin is for inputed data loaded in one of 6 kinds of control registers.

Fig. 5 Shows the timing diagram of data input from microcomputers

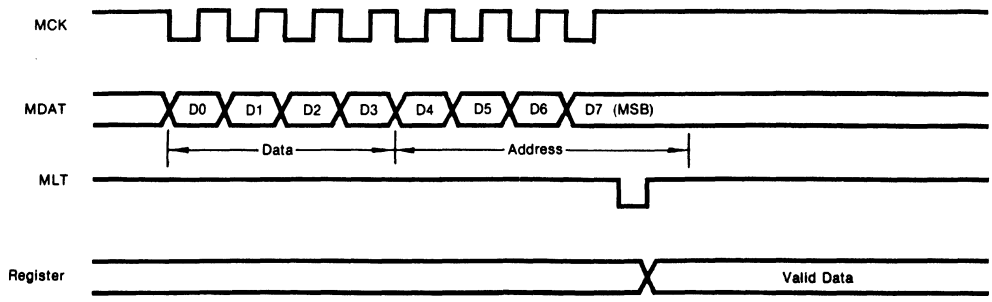


Fig. 5 Data Input Timing Diagram

According to the address of MDAT, the control register is selected as below table 2 below.

Control Register	Comment	Address D7~D4	Data				ISTAT Pin
			D3	D2	D1	D0	
CNTL-Z	Data Control	1 0 0 1	ZCMT	HIPD	NCLV	CRCD	Hi-Z
CNTL-S	Frame Sync Protection Attenuation Control	1 0 1 0	FSEM	FSEL	WSEL	ATTM	Hi-Z
CNTL-L	Tracking Counter Lower 4 Bit	1 0 1 1	TRC3	TRC2	TRC1	TRC0	$\overline{\text{Complete}}$
CNTL-U	Tracking Counter Upper 4 Bit	1 1 0 0	TRC7	TRC6	TRC5	TRC4	$\overline{\text{COUNT}}$
CNTL-W	CLV Control	1 1 0 1	COM	WB	WP	GAIN	Hi-Z
CNTL-C	CLV Mode	1 1 1 0	CLV Mode				$\overline{\text{PW}\geq 64}$

Table 2. Data of Selected Control Register

From to D0 through D7, the function of each control register is descriped below.

1) CNTL-Z Register

This is a control register for the zero cross mute of audio data, PHAS, the control signal of phase servo and CRCF data.

		Data = 0	Data = 1
ZCMT	D3	Zero cross mute "OFF"	Zero cross mute "ON"
HIPD	D2	Phase normally active	Phase convert "L" to "Hi-Z" by LKFS
NCLV	D1	Phase servo driven by frame sync	Phase servo be controlled by base counter
CRCQ	D0	SQDT output without SQOK	SQDT = CRCF during the rising time of S0S1

2) CNTL-S Control Register

This is a control register for the frame sync. protection and attenuation.

FSEM	FSEL	Frame
0	0	2
0	1	4
1	0	8
1	1	13

WSEL	Clock
0	±3
1	±7

ATTM	MUTE	dB
0	0	0
0	1	–
1	0	–12
1	1	–12

3) CNTL-L, U Control Register

When the numbers of tracts to be counted are input from a microcomputer, data is loaded in these registers. (See tracking counter)

4) CNTL-W Control Register

This is a control register for CLV-Servo

		Data = 0	Data = 1	Comments
COM	D3	XTFR/4 & PBFR/4	XTFR/4 & PBFR/4	Phase comparative frequency during PHASE-mode
WB	D2	XTFR/32	XTFR/16	Bottom hold period during SPEED and HSPEED-mode
WP	D1	XTFR/4	XTFR/2	Peak hold period during SPEED-mode
GAIN	D0	– 12dB	0dB	SMPD gain during SPEED & HSPEED-mode

5) CNTL-C Control Register

This is a control register for CLV-Servo

Mode	D7 ~ D4	D3 ~ D0	SMDP	SMSD	SMEF	SMON
Forward	1 1 1 0	1 0 0 0	H	Hi-Z	L	H
Reverse		1 0 1 0	L	Hi-Z	L	H
SPEED		1 1 1 0	SPEED mode	Hi-Z	L	H
HSPEED		1 1 0 0	HSPEED mode	Hi-Z	L	H
PHASE		1 1 1 1	PHASE mode	PHASE mode	Hi-Z	H
XPHSP		0 1 1 0	SPEED, PHASE mode	Hi-Z or PHASE mode	L or Hi-Z	H
VPHSP		0 1 0 1	SPEED PHASE mode	Hi-Z or PHASE mode	L or Hi-Z	H
STOP		0 0 0 0	L	Hi-Z	L	L

TRACKING COUNTER

This counter is used to improve track-jumping characteristics. The number of tracks that are to be jumped are loaded into either register CNTL-L or CNTL-U. After either register CNTL-L or CNTL-U has been loaded, and at the rising edge of the next MLT, the TRCK pulse counte begins. When n (if register CNTL-L = register = CNTL-U = 0, then n = 256) is loaded into the register, and when the address is set in CNTL-L, the signal ($\overline{\text{COMPLETE}}$) is output from pin SENS at high level until the "n"th pulse, and then at low level for succeeding pulses. When the address is set in CNTL-U, the signal ($\overline{\text{COUNT}}$) TRCK/2n is output. Fig. 6 shows the timing of the tracking counter.

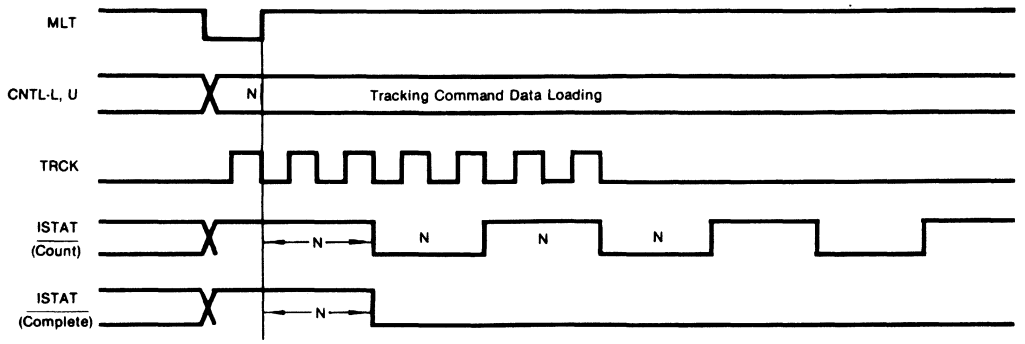


Fig. 6 Tracking Count Timing Chart

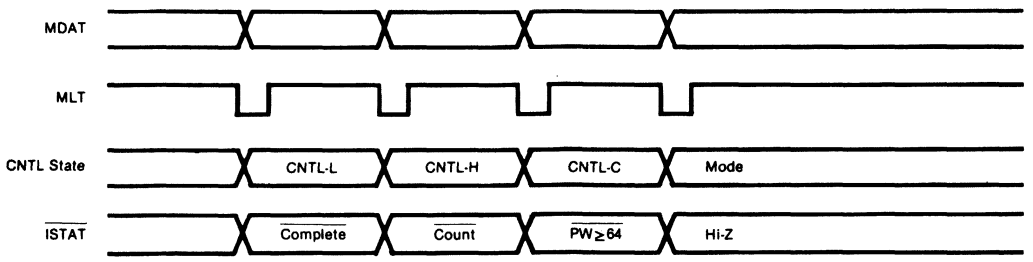


Fig. 7 $\overline{\text{ISTAT}}$ Output Signal by CNTL Register

X'TAL OSCILLATION

1) Block Diagram

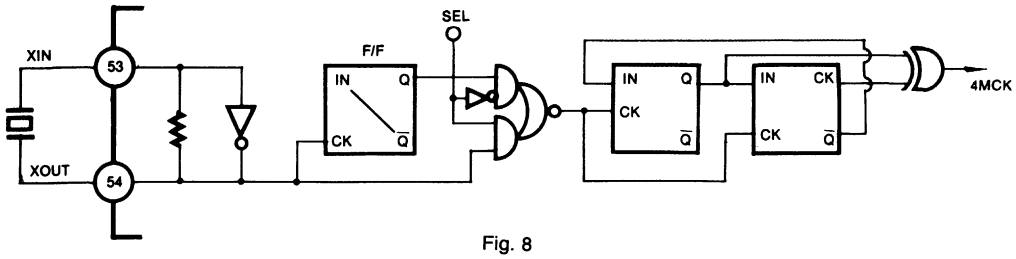
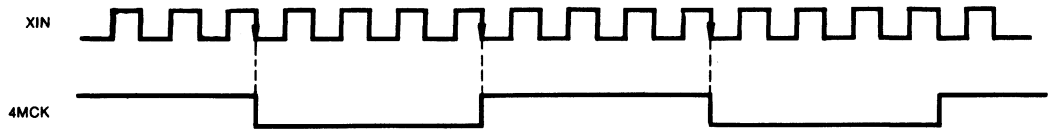
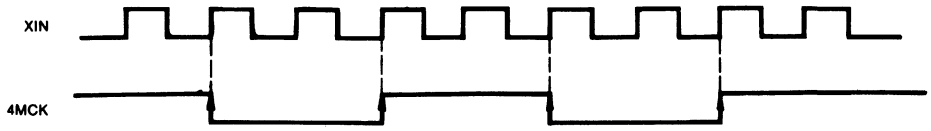


Fig. 8

2) Timing Chart (SEL = 0) in Use f = 16.9344MHz X'tal OSC.



3) Timing Chart (SEL = 1) in use f = 8.4672MHz X'tal OSC.



DIGITAL FILTER

KS5991 has a built-in, 17th FIR Digital Filter.
The digital filter consists of RAM, multiplier, serial to parallel, and parallel to serial converter and controller.

1) Block Diagram

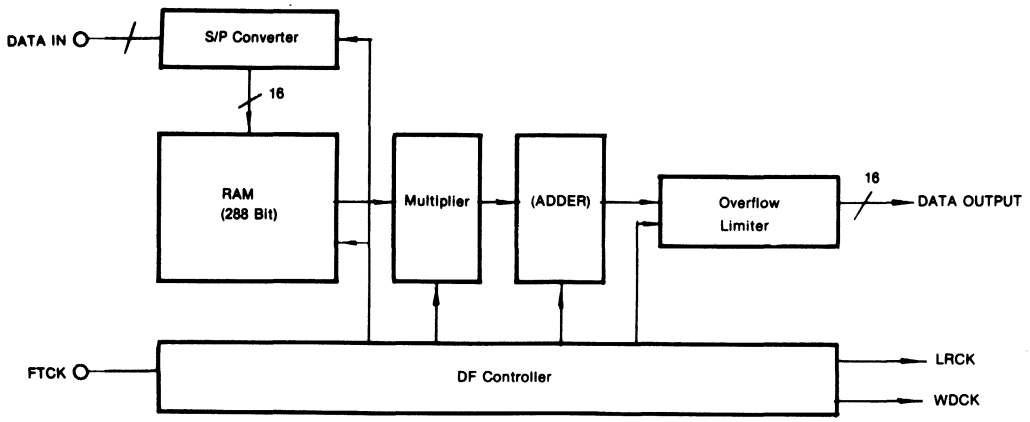


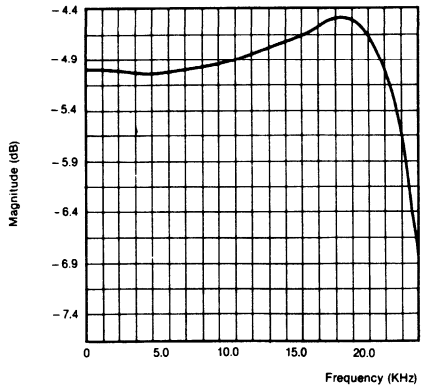
Fig. 9

2) Specification

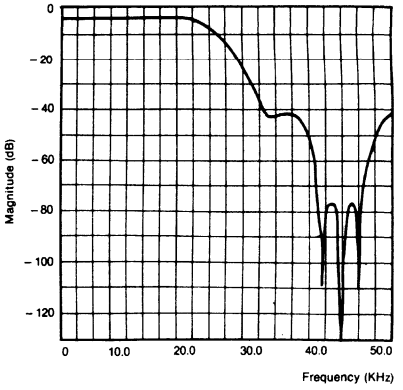
	DC through 18KHz ripple 20KHz of attenuation against 1KHz	±0.07dB max 0.65dB max
	44.1±1KHz attenuation against 1KHz 44.1±5KHz attenuation against 1KHz 44.1±10KHz attenuation against 1KHz 44.1±20KHz attenuation against 1KHz −30dB frequency range against 1KHz −60dB frequency range against 1KHz	87dB min 58dB min 44dB min 10dB min 44.1±14KHz 44.1±4KHz

3) Frequency Characteristic

A. Ripple Characteristic Graph



B. Low Pass Filter Frequency Characteristic Graph



EFM BLOCK

The EFM Block is made up of an EFM Demodulator which demodulates the EFM data inputted from a recorded disc, EFM Phase Detector, Frame Sync Detector/Protector/Inserter, Subcode Sync Detector, and the Controller for the EFM Block.

1) EFM Phase Detector

As the EFM signal inputted from the disc contains a 2.16 MHz component, a 4.32 MHz bit clock is generated to detect the phase of the signal. The PBCK outputs the result to the PHAS terminal after detecting the phase on the edge of the EFM signal. The relationship between the EFM signal and the PBCK is explained in the following Timing Chart.

A. In normal operation

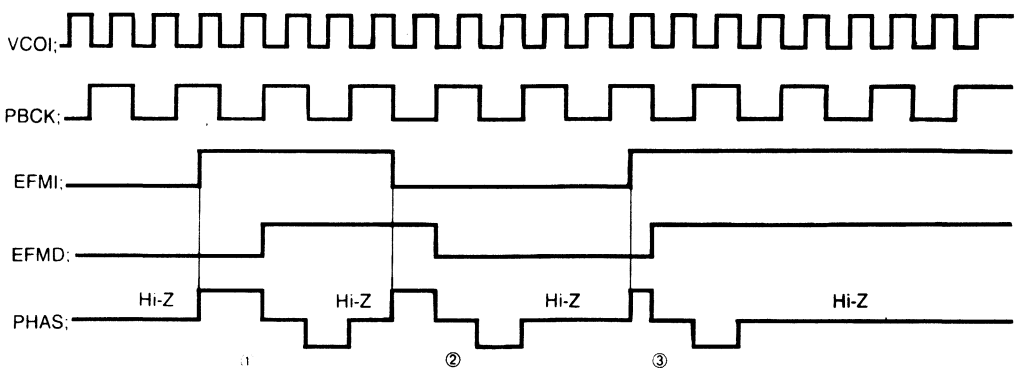


Fig. 10 EFM Phase Detection Timing Chart

Case ① : When the EFM signal is slower than the VCO
Case ②: When the EFM signal is locked up the VCO
Case ③: When the EFM signal is faster than the VCO

B. In abnormal operation

When the HIPD of CNTL-Z is chosen as 'L' from M-COM, the detector of the EFM phase operates as in Fig. 5. When the HIPD is 'H' and the time 'L' of LKFS is below 3.5T during a PBFS period T, it outputs Hi-Z to the PHAS terminal as an "L". When it is above 3.5T, it outputs Hi-Z a 3.5T.

2) EFM (Eight to Fourteen) Demodulator

The modulated 14 bit Data is inputted from a disc, and then it is inputted into a NRZ-I circuit. As the EFM Data passes by the NRZ-I circuit, which converts 14-bit data into 8 bit data, it gets demodulated to 8-bit data. There are two kinds of demodulated data: subcode and PCM data. The subcode data is inputted into the subcode Block, and the PCM Data is written into 16KSRAM by the CE signal and the WE signal.

3) Frame Sync Detector/Inserter/Protector

A. Frame Sync Detector

CDP data are composed of the units of a frame. A frame is made up of Frame Sync, Subcode Data, PCM Data, and Redundancy Data. A Frame sync is detected each frame using this format.

B. Frame Sync Protector/Inserter

There are cases in which the Frame Sync is left out or detected from data besides the frame sync because of the effects of an error on the disk or Jitter. In this case the frame sync needs to be protected and inserted. To protect the frame sync, a window is made by the use of a WSEL signal of the CNTL-S Reg. The frame sync which comes into the window is true data, and the frame sync deviating from the window is disregarded.

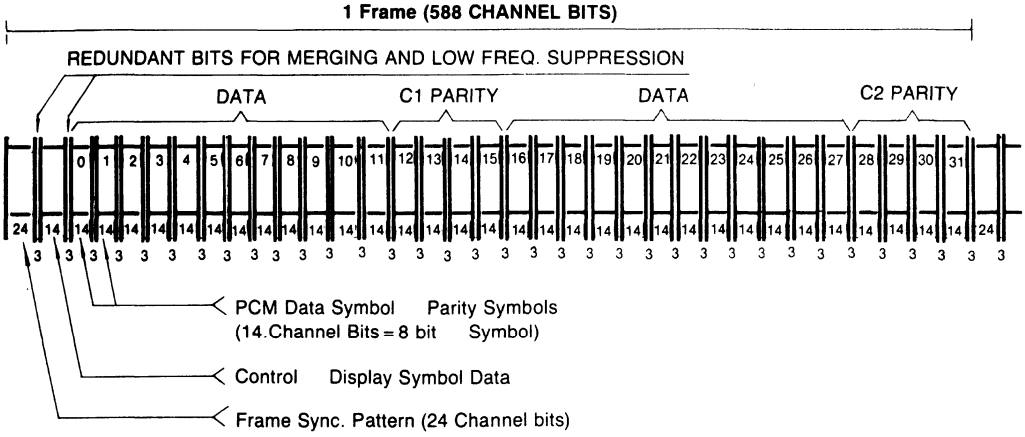


Fig. 11 (Frame Format)

The width of the window is determined by the WSEL signal from the CNTL-S Reg. (cf. CNTL-S) being inserted in the frame sync continuously. If the frame sync is not detected inside a frame sync protection window, insert a frame sync. When the frame sync reaches the number of a frame designated by the FSEM and FSEL of the CNTL-S Reg, ULKFS becomes 'L', and the frame sync protection window is disregarded. In this case, an outputted frame sync is unconditionally accepted. After the frame sync is received, the ULKFS signal becomes 'H' and accepts a frame sync detected inside the window.

LKFS	ULKFS	Explanation
I	I	When a play back frame sync coincides with a generated frame sync.
O	I	① When a PBFR sync is detected in the window chosen by WSEL even if a play back frame sync does not coincide with a generated frame sync ② In the case of sync insertion, because a PBFR sync does not coincide with a XTER sync, and a frame sync in the window chosen by WSEL is not detected.
O	O	① After inserting as many sync's as the number of frames decided by the FSEM and FSEL by the CNTL-S Reg. and because a Frame Sync is not detected within a window. ② When PBFR sync is not continuously detected after situation ① happens.

SUBCODE BLOCK

The 14-bit subcode sync signal S0, S1 is detected in the Subcode Sync Block, in a frame delay, after the output of S0, S1 is outputted. In this case, the signal of S0 + S1 is outputted through the S0S1 terminal, and the signal of S0·S1 is outputted through the SDAT terminal, when the signal S0S1 becomes 'H'. After the 14-bit Subcode Data inputted to the EFMI terminal get EFM Demodulated, 8-bit P, Q, R, S, T, U, V, W subcode data are outputted to SDAT by SBCK clock after it syncronizes with the signal PBFR. Only Q data are chosen among the 8 subcode data, and it is loaded into 80 shift registers. The CRC-checked results of the loaded data is synchronized with the S0S1 rising edge, and is outputted to the SQCK terminal.
If the result of the CRC check is an error, 'L' is outputted to the SQCK terminal. If it is true, 'H' is outputted to the SQOK terminal. If the CRCD of CNTL-Z mode is 'H', the result of the CRC check is outputted to the SQDT terminal from the Section 'H' of the S0S1 section 'H' during the SQCK falling edge.
The timing chart of a subcode block is as follows:

1) In SQEN = 'L': SDAT, SQDT, S0S1, SQOK, VCOI Timing Relation

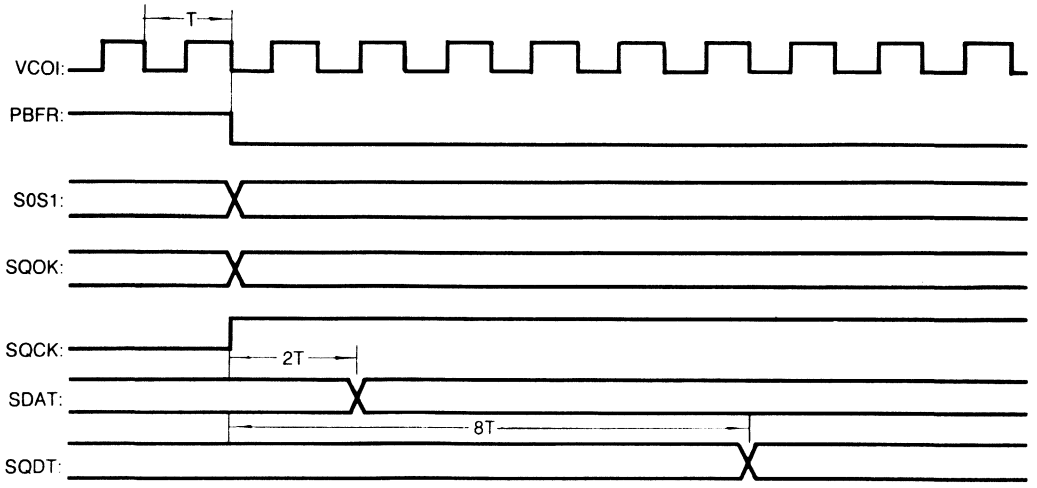


Fig. 12

2) In SQEN = 'L': SQOK, SQDT, S0S1, Timing Chart

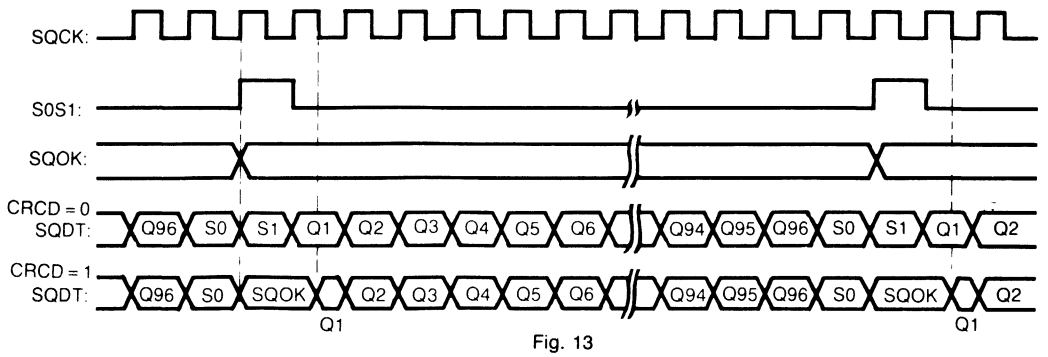
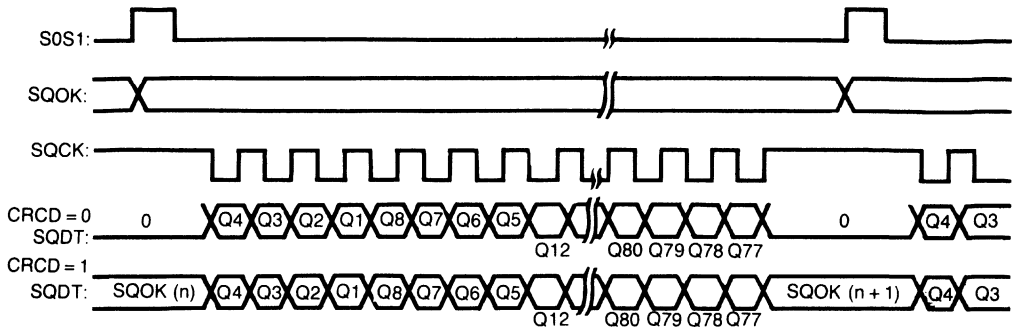


Fig. 13

3) In SQEN = 'H': SQOK, SQDT, S0S1, SQCK Timing Chart



Comment: When a SQOK of subcode Q Data is 'H', subcode data is outputted to SQDT according to SQCK. When SQOK is 'L', 'L' is outputted to the SQDT terminal.

Fig. 14

4) VCO1, SDAT, SBCK Timing Chart

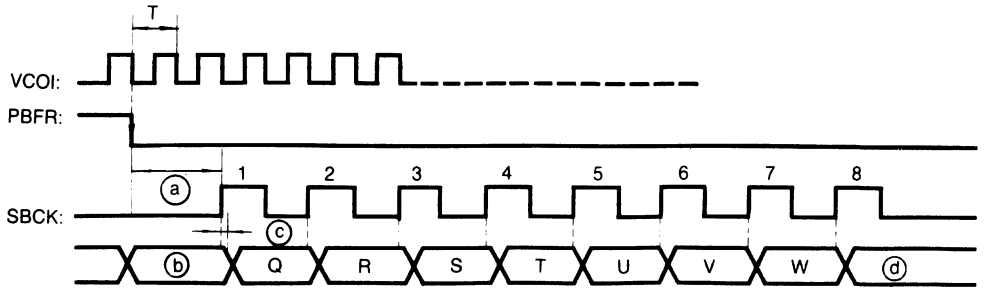


Fig. 15

ⓐ : SBCK is set to "L" for about 10μS after PBFR becomes a falling edge.

ⓑ : When S0S1 is 'L', a subcode P is outputted. When S0S1 is 'H', S0S1 is outputted.

ⓒ : When a cycle of VCO1 is 'T', the width of ⓒ is 4T ~ 6T.

ⓓ : When the pulse inputted into the SBCK terminal is above 7, subcode data P, Q, R, S, T, U, V, W is repeated.

ECC (Error-Correction Code) Block

The function of ECC Block is to recover damaged, data to some extent, when data on the disk is damaged. By using CIRC (Crossed-Interleave Reed-Solomon Code), C1 (32, 28) and C2 (28, 24) errors are corrected. ECC is performed with an 8-bit as a symbol unit. In correcting C1, a C1 Pointer is generated, and in correcting C2, a C2 pointer is generated. C1, C2 Pointers send error information or the data to which ECC is given. After correcting C2, Data, Error Data is sent by outputing a C2 Flag.
The signal C2FL is an AND signal of C2F1 and C2F2. By using this information, Data is treated in the interpolator block.

C1F1	C1F2	C1, C2 Error	C2F1	C2F2	C2FL
0	0	No Error	0	0	0
0	1	Single Error	0	1	0
1	0	Double Error	1	0	0
1	1	Irretrievable Error	1	1	1

C1F1, C1F2 — Output the state of an error correction by C1 Decoder

C2F1, C2F2 — Output the state of an error correction by C2 Decoder

C2FL — Becomes 'L' when an error correction by C2 Decoder is possible and an 'H' when error correction is impossible.

16K SRAM BLOCK

After EFM demodulation of EFM modulated data is inputted from a disc, and the Data is written into RAM or data is outputted to Read/Write and D/A Converters in the ECC Processing for reading, the SRAM Address Generator and a 16K SRAM are installed.
SRAM terminal must be 'H' in a 16K SRAM application.

1) Address Generation Priority Control

Writing in EFM demodulation, reading the data with R/W, D/A Converters in the ECC process, are sometimes are required at the same time.
When 3 signals are demanded at the same time, priority of the data process needs to be controlled. Priority is D/A Converter Read demand > EFM Write demand > ECC R/W demand.

2) EFM Demodulation Data Write Demand

EFM demodulated data must be written to SRAM. Priority is controlled when the write demand signal is transmitted to the SRAM Address Generator, and the Enable signal is transmitted to the EFM Block. The generated address is transmitted to the SRAM Interface circuit.
A generated address is data in which deinterleave is considered, and a frame of 32 addresses is generated.

A. In the use of 16K SRAM (in EFM & ECC Write): SRAM terminal 'H'
DB1 ~ DB8 and AD1 ~ AD11 terminals are in a state of Hi-Z. $\overline{CE}$ and $\overline{WE}$ are 'Don't Care.'

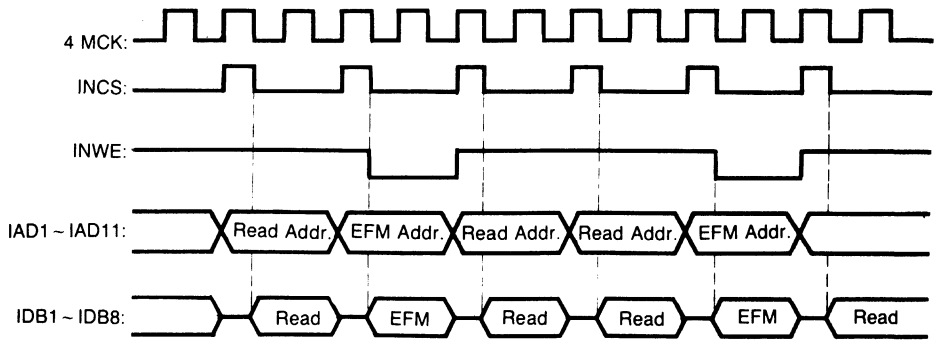
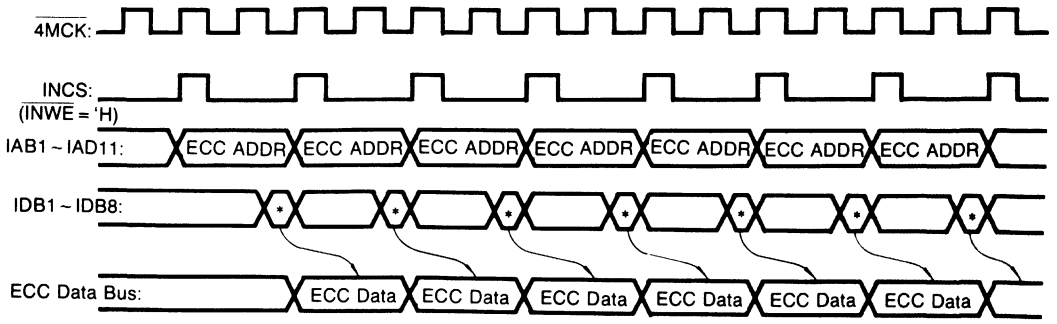


Fig. 16

3) R/W Demand of ECC Data

For C1 and C2, ECC treatment, 129 Address demand signals generated due to an R/W operation must be given to 64 PCM data and 65 Pointers during a frame.
The write of FCC processing is the same as 2) an EFM Write operation.
In reading, it is as follows:

A. In the use of 16K SRAM Reading Timing (SRAM: H)



*: Valid ECC Data

Fig. 17

4) D/A Converter Read Demand

Since each 6 sampling data on the left and right channel and 12 C2 Pointer data must be read for a frame, 36 read enable demand signals are caused. The timing chart for a D/A Converter Read is the same as the R/W demand block of ECC data. As a result, the number of the maximum R/W operation actions demanded for a frame is 179.

5) Address Generated Block

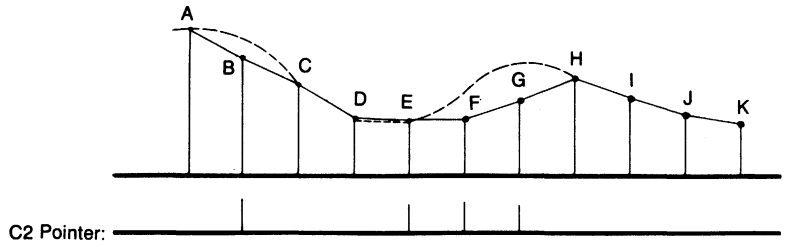
The interleaving data in encoding is deinterleaved in decoding. The data of 108 frames is needed to get 8 frames of PCM data in a CDP format. To get data suitable for a CDP format, 2 counters are needed. A write base counter is used to write. EFM demodulation data are hindered in storing data in SRAM due to disk shaking, the instability of a servo system, etc.

6) Jitter Margin

EFM demodulation data are hindered in storing data in SRAM due to disk shaking, the instability of a servo system, etc. Now that the data that must be kept is limited by the size of SRAM in view of time, data is destroyed if the value of the read/write base counter has a difference above ± 5 frames. Being loading into the value of a write base counter with enforcement, the value of a read the base counter has a jitter margin below ± 4 frames when there is a difference of over ± 5 frames in the read/write base counter value.
A read base counter value is loaded into a write base counter with enforcement when data on the left and right channels are all muting, or when NCLV is 'H' and CLV-Servo is stop, forward, and reverse. When the difference between the read/write base counter is above ± 4 frame, a 'H' signal is outputted to the JIT terminal for a period.

INTERLEAVE, MUTE BLOCK

When a burst error occurs on a disk, sometimes the data can't be corrected even if a ECC process is conducted. An interpolator block revises data by using C2 Pointer outputted through the ECC Block. PCM data inputted to a data bus are inputted to the left and right channels, respectively, in the order of an 8-bit C2 Pointer. Lower 8-bit, and Upper 8-bit. A pre-hold method is taken when a DA Flag is 'H' continuously. In case of the occurrence of a single error, a mean value interploating method is carried out with the range of the PCM Data before and after an error happens. When a check against a checked cycle is 'L', R-CH Data is outputted. L-CH Data is outputted when the check is 'H'. As to the timing chart of a interpolator block see figure 19.



$B = \frac{A+C}{2}$: Mean value interpolation

F = E = D : Pre-hold interpolation

G = F + H : Mean value interpolation

Fig. 18

2) Mute and Attenuation

Using a Mute terminal and a ATTM signal of the CNTL-S Reg., AUDIO data is muted or reduced. There are two kinds of mute: zero-cross muting and muting.

A. Zero-Cross Muting
Audio data is muted when a mute terminal is 'H' and when 6 bits in a high position of Audio Data are all 'H' or 'L'.

B. Muting
Audio data is muting when ZCMT of the CNTL-Z Reg. is 'L' and when a mute terminal is 'H'.

C. Attenuation
By means of the ATTM signal of the CNTL-S Reg. and the signal of the Mute terminal, an audio signal attenuation occurs as shown in the following.

ATTM	MUTE	Degree of Attenuation
0	0	0 dB
0	1	– dB
1	0	– 12 dB
1	1	– 12 dB

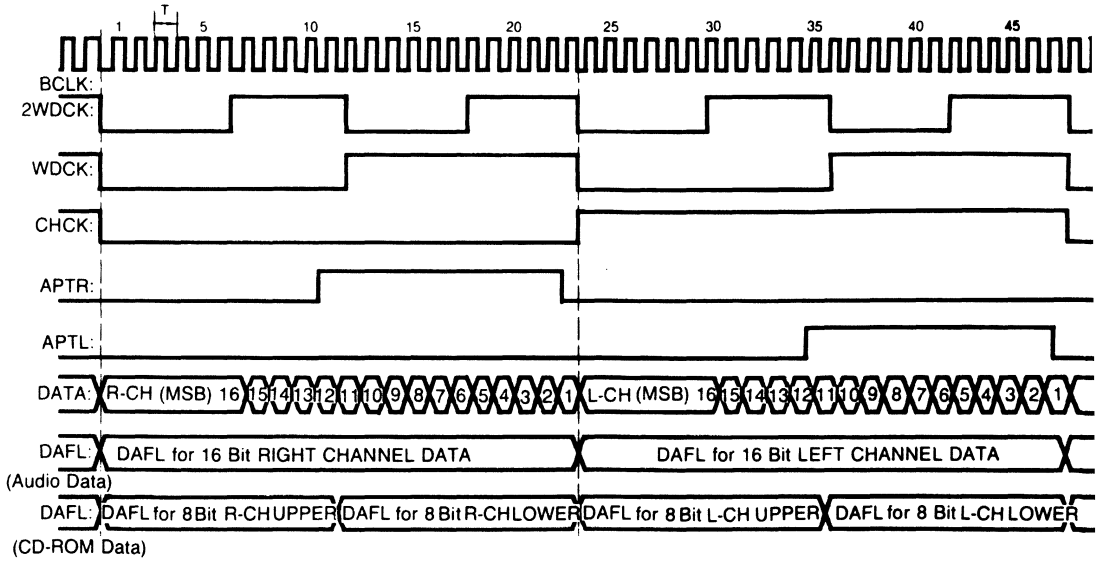


Fig. 19. When Sel. 5 is 'L', and DF is off, the Timing Chart of PCM Data

CLV SERVO

CNTL-C Reg. is selected to control the CLV Servo by the Data inputted from μ-COM. In CNTL-C Reg, the data from μ-com appoint the CLV servo action mode and controls the spindle motor.

1) Forward

The states of the output terminal, related to the mode, to rotate a spindle motor forward are SMDP = 'H', SMSD = Hi-Z, SMEF = 'L' and SMON = 'H', respectively.

2) Reverse

The modes to rotate a spindle motor reversly are SMDP = 'L', SMSD = 'Hi-Z', SMEF = 'L', and SMOD = 'H'.

3) SPEED-Mode

The SPEED-Mode is the mode for the rough control of a spindle motor when a track is jumps or a EFM phase is unlocked. If a cycle of VCO is 'T', the pulse width of a frame sync is '22T'. Sometimes a EFM signal is above 22T, due to noises on a disc, etc. A correct frame sync cannot be detected when the signal is not removed. In this case, the pulse width of an EFM signal is detected at a cycle of XTFR/2 or XTFR/4, which are peak hold clocks. The pulse width of a EFM signal is detected at a cycle of XTFR/16 or XTFR/32, which are bottom hold clock. The value detected is used for a frame synchronization signal. When the frame synchronization signal is smaller than 21T, the SMPD terminal outputs 'L'. When it is 22T, Hi-Z is outputted. 'H' is outputted when it is above 23T.
When the GAIN signal of CNTL-W Reg. is 'L', the SMDP terminal is outputted after being attenuated at – 12dB. When the signal is 'H', the terminal is outputted without any attenuation. <cf. figure 20>
In SMSD, SMEF, and SMON terminals, Hi-Z, 'L', and 'H' are outputted.

4) HSPEED-Mode

The rough servo mode, moves 20,000 tracks in high speed acts between the inside of a CD and the outside in a mirror of the track without a pit EFM and the signal of 20KHz overlap. In this case, since in a speed-mode the peak range of a longer mirror signal than the original frame sync is detected, a servo operation becomes unstable. In HSPEED-mode, a peak hold uses a 8.4672/256 MHz signal, and a bottom hold removes a mirror component and stabilizes the high speed servo operation by using a XTFR/16 or XTFR/32 period signal.
In SMSD, SMEF, and SMON terminals, Hi-Z, 'L', and 'H' are outputted.

5) PHASE-Mode

A PHASE Mode is the mode used to control an EFM Phase. When NCLV of CNTL-Z is 'L', it detects a phase difference between PBFR/4 and XTFR/4, and when NCLV is 'H', it detects the phase difference between read base Counter/4, and write base Counter/4, and then outputs to the SMPD terminal. See figure 8.
If the VCO/2 signal cycle is put as 'T' and the PBFR during a 'H' period as a V_{pb}, it outputs 'H' to a SMSD terminal from the falling edge of PBFR for (W_{pb}-278T) x 32, and later outputs 'L' to the falling edge of PBFR. Refer to figure 22.

6) XPHSP-Mode

A XPHSP mode is the mode used in normal operations. It samples a LKFS signal made in the frame sync block at a cycle of PBFR/16. After sampling 'H', DHASE mode is carried out. When 'L' is sampled continuously 8 times, it goes over to speed-mode. CNTL-W Reg. decides the choice of the peak hold of the speed-mode, the bottom hold cycle of SPEED-and HSPEED-Mode, and the choice of a gain.

7) VPHSP-Mode

A VPHSP-Mode is the mode used for rough servo control. It uses VCO instead of X'tal in the EFM pattern test. When the range of VCO center changes, VCO is easily loaded because the rotation of a spindle motor changes in the same direction.

8) STOP

Stop is the mode to stop a spindle motor.
SMDP = 'L', SMSD = Hi-Z, SMEF = 'L', SMON = 'L'

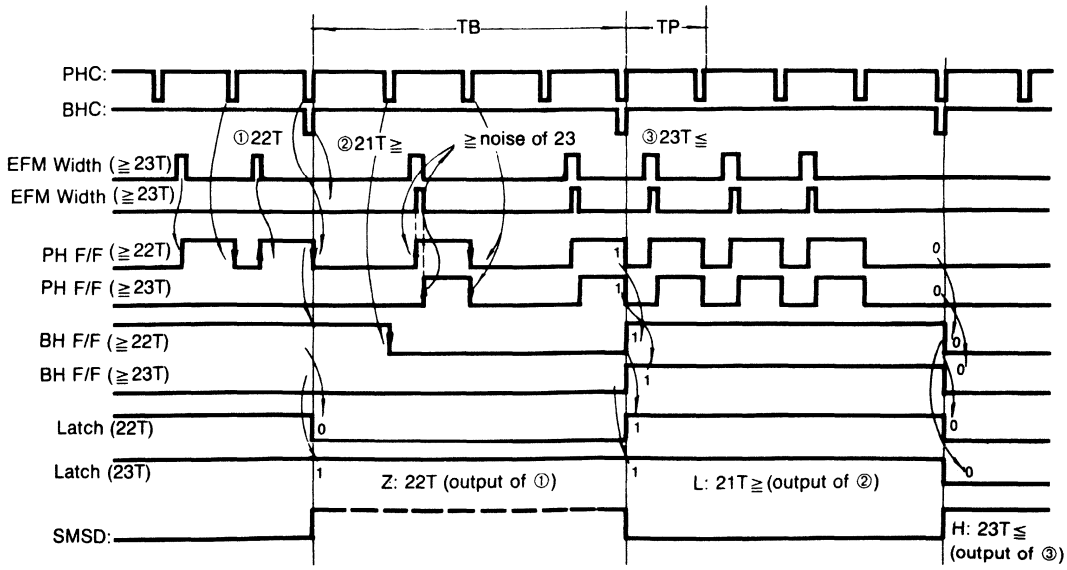


Fig. 20 The Timing Chart of SMSD output when gain is 'H' in a speed-mode

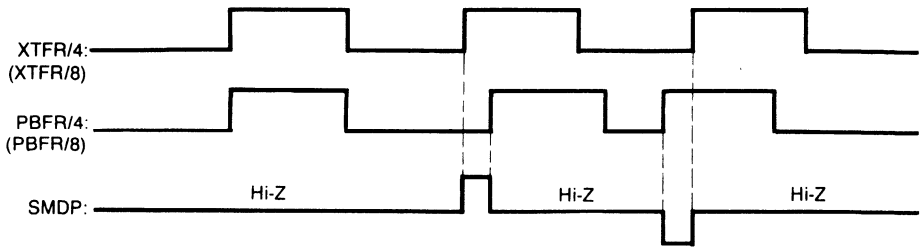
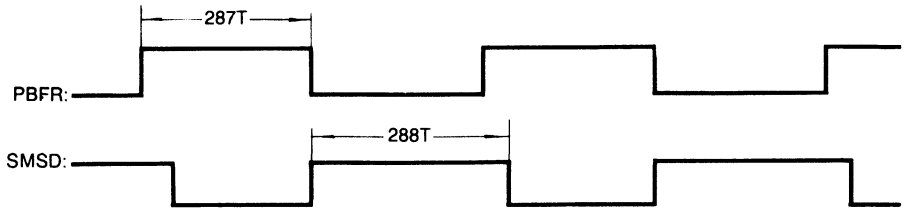
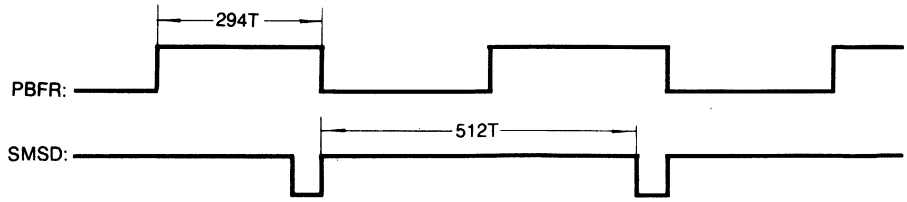


Fig. 21 Output Timing Chart of a SMDP terminal



(a) When PBFR is 287T, Timing Chart of SMSD output

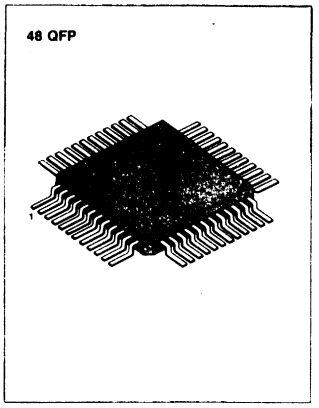


(b) When PBFR is 294T, Timing Chart of SMSD output

Fig. 22 In a PHASE Mode Timing Chart of SMSD output (T: VCO/2)

SERVO SIGNAL PROCESSOR

The KA8309B is Bi-Mos integrated circuit designed for the servo control of the compact disc player application.



FEATURES

- **Servo control functions; (focus, tracking, seld servo control)**
- **Loop filter and VCO for EFM clock reproduction PLL**
- **Provide function**
  Preventing sled runaway
  Anti-shock
  Spindle servo
  Auto-sequencer
- **Provide adjustable peak of focus search, track jump and sled kick with external resistor**
- **Low power consumption (100mW typ; ± 5V, 80mW, 5V)**
- **Single power supply, 5V**
- **Split power supply, ± 5V**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA8309B	48 QFP	−20°C ~ +75°C

BLOCK DIAGRAM

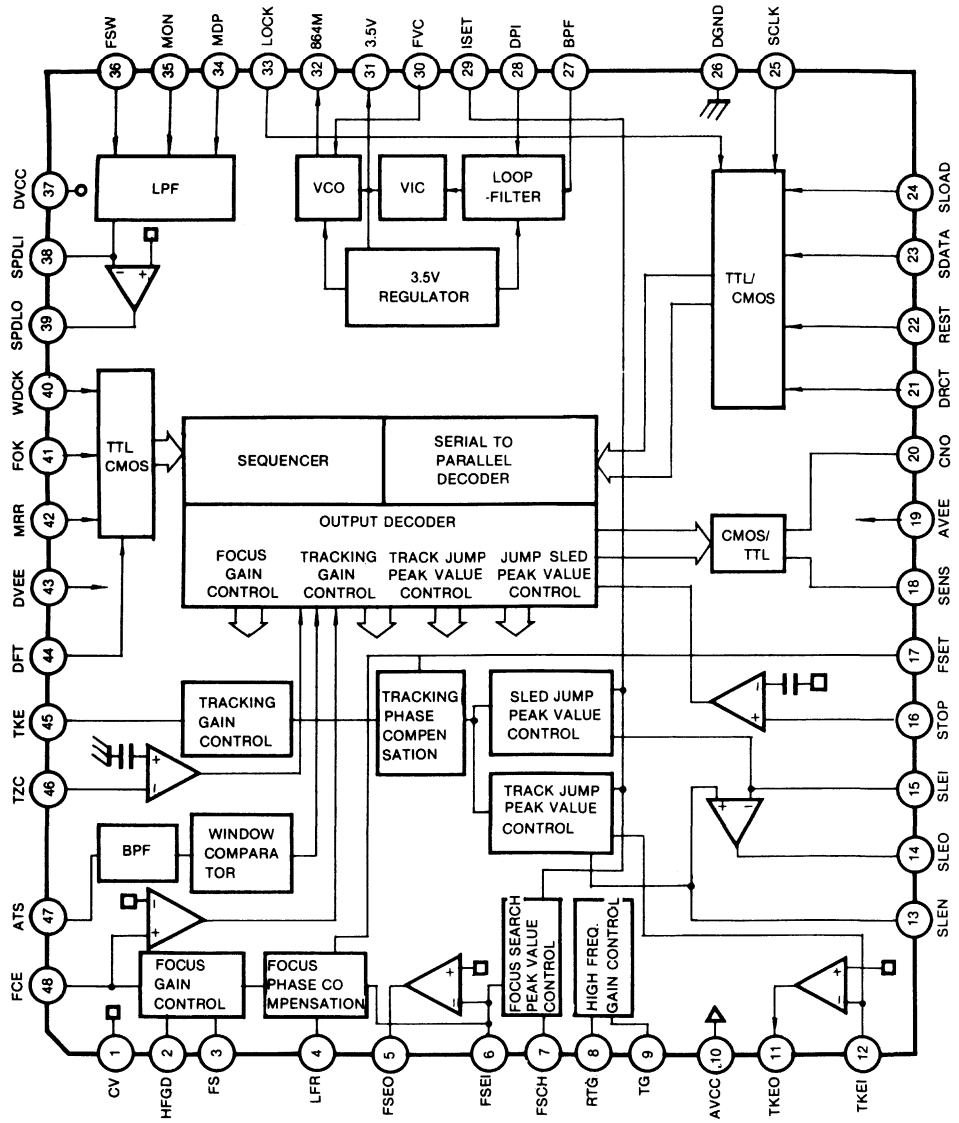


Fig. 1

PIN DESCRIPTION

Pin No	Symbol	Description
1	CV	Center voltage.
2	HFGD	Reduce high frequency gain with capacitor connected between pin 2 and pin 3.
3	FS	High frequency gain of focus servo can be changed by switching FS3 on or off.
4	LFR	Rising low frequency bandwidth of focus loop.
5	FSEO	Focus servo error output.
6	FSEI	Inverting input pin for focus amplifier.
7	FSCH	Time constant external pin to generate focus search waveform.
8	RTG	Time constant external pin to switch the tracking gain of high frequency.
9	TG	Provide time constant to change the high frequency tracking gain.
10	AV_{CC}	Analog positive power supply.
11	TKEO	Tracking error output.
12	TKEI	Inverting input pin for tracking amplifier.
13	SLEN	Non-inverting input pin for tracking amplifier.
14	SLEO	Sled output.
15	SLEI	Inverting input pin for sled amplifier.
16	STOP	Pin for detecting a signal for the on/off limit switch of the innermost part of the disc.
17	FSET	Setting the peak frequency of the focus, tracking phase compensation and to fo the CLV LPF.
18	SENS	Output pin for FZC, AS, TZC, STOP and BUSY by command from CPU.
19	AV_{EE}	Analog negative power supply.
20	CNO	Track number count output.
21	DRCT	Control pin for one track jump.
22	REST	Reset input pin, reset at "L".
23	SDATA	Serial data input.
24	SLOAD	Latch input.
25	SCLK	Serial data transfer clock.
26	DGND	Digital ground.
27	BPF	Provide time constant for the loop filter.

PIN DESCRIPTION (Continued)

Pin No	Symbol	Description
♪ 28	DPI	Input pin for detected phase.
29	ISET	Current is input, determining the peaks of focus search, track jump, and sled kick.
30	FVC	External resistor to adjust free running frequency of VCO.
31	3.5V	Regulated output voltage.
32	864M	Output pin of 8.64MHz VCO.
33	LOCK	Pin for the operation of the sled runaway prevention circuit at "L".
34	MDP	Pin for connecting the DSP.
35	MON	Pin for connecting the DSP.
36	FSW	Providing an external LPF time constant of the CLV servo.
37	DV_{CC}	Digital positive power supply.
38	SPDLI	Inverting input for spindle servo amplifier.
39	SPDLO	Spindle servo error output.
40	WDCK	Clock input for auto-sequence.
41	FOK	Focus ok signal input pin.
42	MRR	Mirror signal input pin.
43	DV_{EE}	Digital negative power supply.
44	DFT	Defect signal input pin.
45	TKE	Tracking error signal input pin.
46	TZC	Input pin for the zero cross tracking comparator.
47	ATS	Input pin for detect ATSC.
48	FCE	Input pin for focus error signal.

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	$V_{CC} - V_{EE}$	12	V
Power Dissipation	P_D	600	mW
Operating Temperature	T_{OPR}	−20 ~ +75	°C
Storage Temperature	T_{STG}	−55 ~ +150	°C

ELECTRICAL CHARACTERISTICS

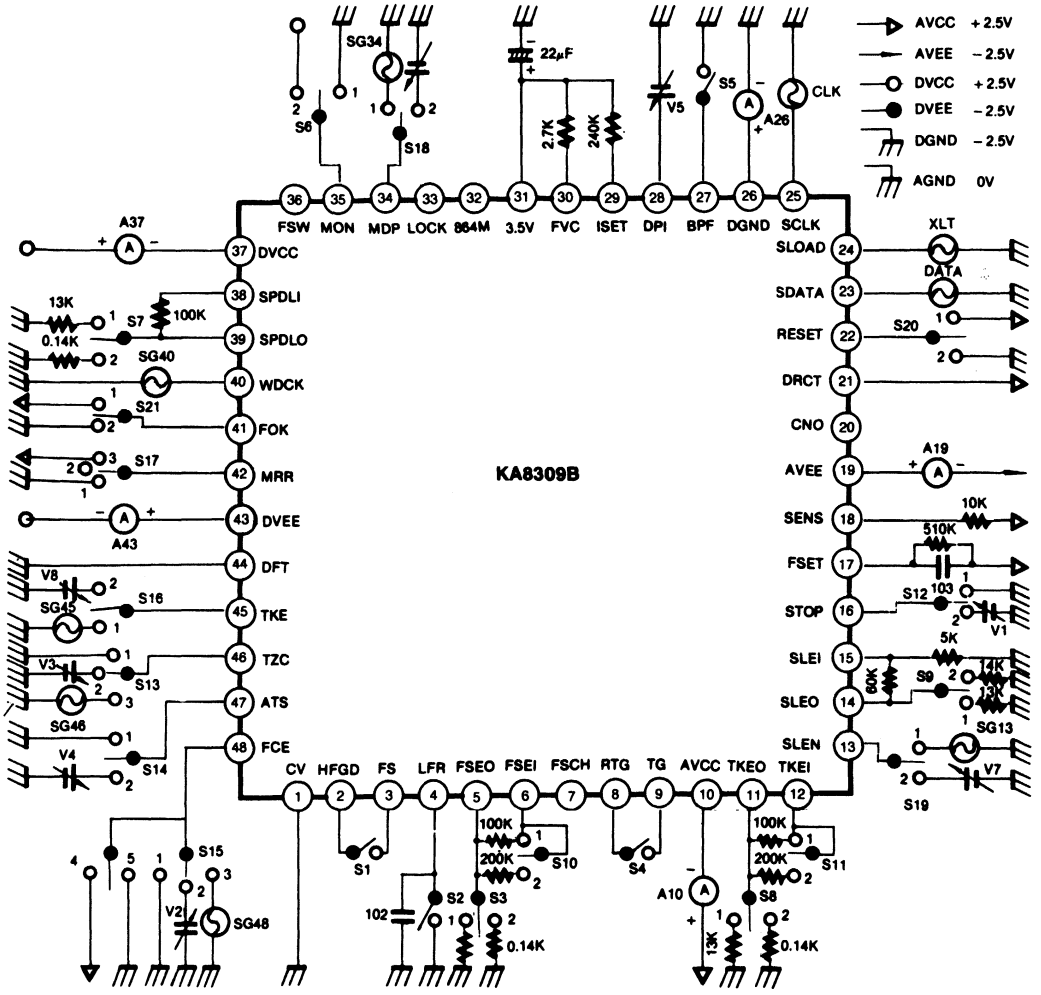
(Ta = 25°C, V_{CC} = 2.5V, V_{DD} = 2.5V, V_{EE} = −2.5V, GND = 0V, unless otherwise specified)

	Characteristic	No.	Symbol	Test Conditions	Min	Typ	Max	Unit
	Circuit Current 1	1	I_{CC1}		2	6	10	mA
	Circuit Current 2	2	I_{CC2}		5	10	15	mA
	Circuit Current 3	3	I_{CC3}		−2	−7	−12	mA
	Circuit Current 4	4	I_{CC4}		−4	−9	−14	mA
Focus Servo	DC Voltage Gain	5	$G_{V\,(DC)\,1}$	SG_{48} = 10Hz, 200mV_{p-p}	19	21	22.5	dB
	Feed Through	6	$G_{V\,(FF)}$	SG_{48} = 10KHz, 40mV_{p-p} Gain difference between 08 and 00 of SD			−35	dB
	Output Voltage 1	7	$V_{O\,(FCS)\,1}$	V_2 = 0.5V	1.98			V
	Output Voltage 2	8	$V_{O\,(FCS)\,2}$	V_2 = 0.5V			−1.98	V
	Output Voltage 3	9	$V_{O\,(FCS)\,3}$	V_2 = 0.5V	1.18			V
	Output Voltage 4	10	$V_{O\,(FCS)\,4}$	V_2 = 0.5V			−1.18	V
	Search Output Voltage 1	11	$V_{O(SEARCH)1}$		−0.62	−0.55	−0.38	V
	Search Output Voltage 2	12	$V_{O(SEARCH)2}$		0.40	0.55	0.64	V
Tracking Servo	DC Voltage Gain	13	$G_{V\,(DC)\,2}$	SG_{45} = 10Hz, 500mV_{p-p}	13.5	14.6	17	dB
	Feed Through	14	$G_{V\,(TF)}$	SG = 10KHz, 500mV_{p-p} Gain difference between 25 and 20 of SD			−39	dB
	Output Voltage 1	15	$V_{O\,(TCK)\,1}$	V_8 = −1.5V	1.98			V
	Output Voltage 2	16	$V_{O\,(TCK)\,2}$	V_8 = +1.5V			−1.98	V
	Output Voltage 3	17	$V_{O\,(TCK)\,3}$	V_8 = −1.5V	1.18			V
	Output Voltage 4	18	$V_{O\,(TCK)\,4}$	V_8 = +1.5V			−1.18	V
	Jump Output Voltage 1	19	$V_{O\,(JUMP)\,1}$		−0.61	−0.55	−0.42	V
	Jump Output Voltage 2	20	$V_{O\,(JUMP)\,2}$		0.42	0.55	0.61	V
Sled Servo	DC Voltage Gain	21	$G_{V\,(DC)\,3}$	SG_3 = 10Hz, 100mV_{p-p}	21.2	22.5	24.2	dB
	Output Voltage 1	22	$V_{O\,(SLD)\,1}$	V_7 = 0.4V	1.98			V
	Output Voltage 2	23	$V_{O\,(SLD)\,2}$	V_7 = −0.4V			−1.98	V
	Output Voltage 3	24	$V_{O\,(SLD)\,3}$	V_7 = 0.4V	1.18			V
	Output Voltage 4	25	$V_{O\,(SLD)\,4}$	V_7 = −0.4V			−1.18	V
	Feed Through	26	$G_{V\,(SF)}$	SG = 10Khz, 200mV Gain difference between 25 and 20 of SD			−34	dB
	Kick Output Voltage 1	27	$V_{O\,(KICK)\,1}$		0.47	0.6	0.70	V
	Kick Output Voltage 2	28	$V_{O\,(KICK)\,2}$		−7.0	−0.6	−0.17	V

ELECTRICAL CHARACTERISTICS (Continued)

	Characteristic	No	Symbol	Test Conditions	Min	Typ	Max	Unit
Spindle Servo	Spindle Servo Gain	29	$G_{V\,(SPD)}$	SG = 10Hz, 200mV$_{p-p}$	14	16.5	19	dB
	Output Voltage 1	30	$V_{O\,(SPD)\,1}$	V_6 = 1.0V	1.78			V
	Output Voltage 2	31	$V_{O\,(SPD)\,2}$	V_6 = −1.0V			−1.78	V
	Output Voltage 3	32	$V_{O\,(SPD)\,3}$	V_6 = 1.0V	1.13			V
	Output Voltage 4	33	$V_{O\,(SPD)\,4}$	V_6 = −1.0V			−1.13	V
PLL	PLL Regulator Output Voltage	34	V_{REG}		3.3	3.5	3.65	V
	Self-running Frequency	35	F_{VCO}	V_5 = 2.5V	7.9	8.6	9.7	MHz
	Frequency Deviation 1	36	ΔF1	Frequency deviation from F_{VCO}, V_5 = 148mV	8.5	11	13.5	%
	Frequency Deviation 2	37	ΔF2	V_5 = −148mV	−13.5	−11	−8.5	%
	Sens Low Level	38	V_{SENSE}				−1.98	V
Output Low Level		39	V_{OL}	SG_{46} = 10KHz, 2V$_{p-p}$			−1.98	V
FZC Threshold Voltage		40	$V_{TH\,(FZC)}$	V_2 = Variable, V_{P18} = 1.1V	39	50	60	mV
ATSC Threshold Voltage		41	$V_{TH\,(ATSC)\,1}$	V_4 = Variable, V_{P18} = 1.1V	−45	−26	−7	mV
ATSC Threshold Voltage		42	$V_{TH\,(ATSC)\,2}$	V_4 = Variable, V_{P18} = 1.1V	7	26	45	mV
TZC Threshold Voltage		43	$V_{TH\,(TZ\overline{C})}$	V_3 = Variable, V_{P18} = 1.1V	−20	0	20	mV
SSTOP Threshold Voltage		44	$V_{TH\,(SSTOP)}$	V_1 = Variable, V_{P18} = 1.1V	−65	−50	−35	mV

TEST CIRCUIT



TEST METHODE (SWITCH CONDITIONS)

No	Symbol	SWITCH Conditions																						I	Input	Test
		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16	S17	S18	S19	S20	S21	S22	S23	SD	Point	Point
1	I_{CC1}	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	1	1	1	1	1	3	1	1	2	1	OFF	1	00		10
2	I_{CC2}	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	2	1	OFF	1	00		37
3	I_{CC3}	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	2	1	OFF	1	00		19
4	I_{CC4}	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	2	1	OFF	1	00		20
5	$G_{V\,(DC)}$	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	1	1	1	3	1	1	1	1	2	1	OFF	1	08	48	5
6	$G_{V\,(FF)}$	ON	ON	1	OFF	OFF	1	1	1	1	1	1	1	1	1	3	1	1	1	1	2	1	OFF	1		48	5
7	$V_{O\,(FCS)\,1}$	OFF	OFF	1	OFF	OFF	1	1	1	1	2	1	1	1	1	2	1	1	1	1	2	1	OFF	1	08	48	5
8	$V_{O\,(FCS)\,2}$	OFF	OFF	1	OFF	OFF	1	1	1	1	2	1	1	1	1	2	1	1	1	1	2	1	OFF	1	08	48	5
9	$V_{O\,(FCS)\,3}$	OFF	OFF	2	OFF	OFF	1	1	1	1	2	1	1	1	1	2	1	1	1	1	2	1	OFF	1	08	48	5
10	$V_{O\,(FCS)\,4}$	OFF	OFF	2	OFF	OFF	1	1	1	1	2	1	1	1	1	2	1	1	1	1	2	1	OFF	1	08	48	5
11	$V_{O\,(SEARCH)\,1}$	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	2	1	OFF	1	03		5
12	$V_{O\,(SEARCH)\,2}$	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	2	1	OFF	1	03		5
13	$G_{V\,(DC)\,1}$	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	2	1	OFF	1	25	45	11
14	$G_{V\,(TF)}$	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	2	1	OFF	1	25	45	11
15	$V_{O\,(TCK)\,1}$	OFF	OFF	1	OFF	OFF	1	1	1	1	1	2	1	1	1	1	2	1	1	1	2	1	OFF	1	25	45	11
16	$V_{O\,(TCK)\,2}$	OFF	OFF	1	OFF	OFF	1	1	1	1	1	2	1	1	1	1	1	1	1	1	2	1	OFF	1	25	45	11
17	$V_{O\,(TCK)\,3}$	OFF	OFF	1	OFF	OFF	1	1	2	1	1	2	1	1	1	1	1	1	1	1	2	1	OFF	1	25	45	11
18	$V_{O\,(TCK)\,4}$	OFF	OFF	1	OFF	OFF	1	1	2	1	1	2	1	1	1	1	1	1	1	1	2	1	OFF	1	25	45	11
19	$V_{O\,(JUMP)\,1}$	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	2	1	OFF	1	20		11
20	$V_{O\,(JUMP)\,2}$	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	2	1	OFF	1	28		11
21	$G_{V\,(DC)\,3}$	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	2	1	OFF	1	20	13	14
22	$V_{O\,(SLD)\,1}$	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	2	2	1	OFF	1	25	13	14
23	$V_{O\,(SLD)\,2}$	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	2	2	1	OFF	1	25	13	14
24	$V_{O\,(SLD)\,3}$	OFF	OFF	1	OFF	OFF	1	1	1	2	1	1	1	1	1	1	1	1	1	2	2	1	OFF	1	25	13	14
25	$V_{O\,(SLD)\,4}$	OFF	OFF	1	OFF	OFF	1	1	1	2	1	1	1	1	1	1	1	1	1	2	2	1	OFF	1	25	13	14
26	$G_{V\,(SF)}$	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	1	1	1	3	1	1	1	1	2	1	OFF	1	20	13	14
27	$V_{O\,(KICK)\,1}$	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	1	1	1	3	1	1	1	1	2	1	OFF	1	22		14
28	$V_{O\,(KICK)\,2}$	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	1	1	1	3	1	1	1	1	2	1	OFF	1	23		14
29	$G_{V\,(SPD)}$	OFF	OFF	1	OFF	OFF	2	1	1	1	1	1	1	1	1	3	1	1	1	1	2	1	OFF	1		34	39
30	$G_{V\,(SPD)\,1}$	OFF	OFF	1	OFF	OFF	2	1	1	1	1	1	1	1	1	3	1	1	2	1	2	1	OFF	1		34	39
31	$G_{V\,(SPD)\,2}$	OFF	OFF	1	OFF	OFF	2	1	1	1	1	1	1	1	1	1	1	1	2	1	2	1	OFF	1		34	39
32	$G_{V\,(SPD)\,3}$	OFF	OFF	1	OFF	OFF	2	2	1	1	1	1	1	1	1	1	1	1	2	1	2	1	OFF	1		34	39
33	$G_{V\,(SPD)\,4}$	OFF	OFF	1	OFF	OFF	2	2	1	1	1	1	1	1	1	1	1	1	2	1	2	1	OFF	1		34	39
34	V_{RFG}	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	1	1	1	3	1	1	1	1	2	1	OFF	1			31
35	F_{VCO}	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	2	1	OFF	1			32
36	ΔF_1	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	2	1	OFF	1			32
37	ΔF_2	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	2	1	OFF	1			32
38	V_{SENSE}	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	1	1	1	1	1	3	1	1	2	1	OFF	1			18
39	V_{OL}	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	1	1	3	1	1	1	1	1	2	1	OFF	1			20
40	$V_{TH\,(FZC)}$	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	1	1	1	1	2	3	1	1	2	1	OFF	1	00	48	18
41	$V_{TH\,(ATSC)\,1}$	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	1	1	2	1	1	1	1	1	2	1	OFF	1	10	47	18
42	$V_{TH\,(ATSC)\,2}$	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	1	1	2	1	1	1	1	1	2	1	OFF	1	10	47	18
43	$V_{TH\,(TZC)}$	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	1	2	1	1	1	1	1	1	2	1	OFF	1	20	46	18
44	$V_{TH\,(SSTOP)}$	OFF	OFF	1	OFF	OFF	1	1	1	1	1	1	2	1	1	1	1	3	1	1	2	1	OFF	1	30	16	18

APPLICATION INFORMATION

CPU Serial Interface Timing Chart

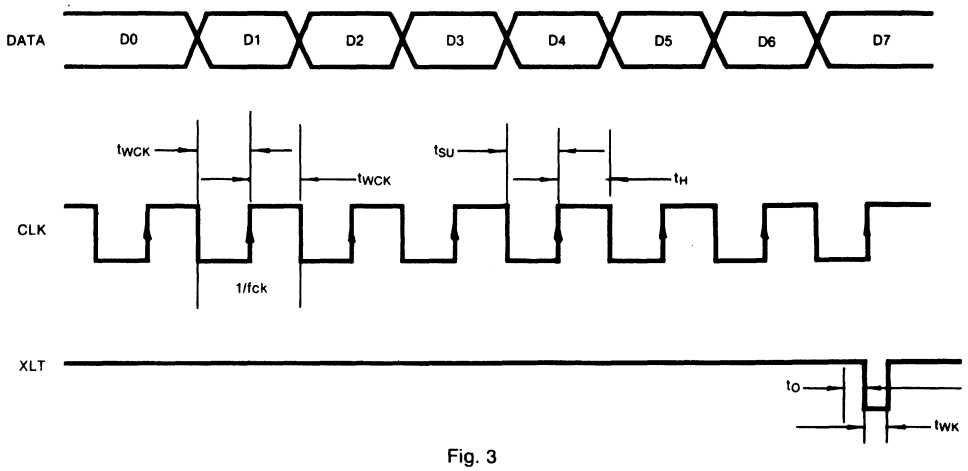


Fig. 3

$DV_{CC} - D_{GND} = 4.5$ to 5.5V

Item	Symbol	Min	Typ	Max	Unit
Clock Frequency	f_{CK}			1	MHz
Clock Pulse Width	f_{WCK}	500			ns
Hold Time	t_{SU}	500			ns
Setup Time	t_H	500			ns
Delay Time	t_D	500			ns
Latch Pulse Width	t_W	1000			ns

SYSTEM CONTROL

Item		Address				Data				Sens Output
		D7	D6	D5	D4	D3	D2	D1	D0	
Focus Control		0	0	0	0	FS4 Focus On	FS3 Gain Down	FS2 Search On	FS1 Search Up	FZC
Tracking Control		0	0	0	1	Anti Shock	Brake On	TG2 Gain Set *1	TG1	A.S
Tracking Mode		0	0	1	0	Tracking Mode *2		Sled Mode *3		TZC
Select		0	0	1	1	PS4 Focus Search + 2	PS3 Focus Search + 1	PS2 Sled Kick + 2	PS1 Sled Kick + 1	SSTOP
Auto Sequence *4		0	1	0	0	AS3	AS2	AS1	AS0	BUSY
	Blind(A,E)/Overflow(C)	0	1	0	1	0.18ms	0.09ms	0.045ms	0.022ms	Hi-Z
	Brake(B)					0.36ms	0.18ms	0.09ms	0.045ms	
	Kick(D)	0	1	1	0	11.6ms	5.8ms	2.9ms	1.45ms	
	Track Jump(N)	0	1	1	1	64	32	16	8	
	Track Move(M)					128	64	32	16	

Note: ***1. GAIN SET**
It is possible to set TG1 and TG2 independently.
When the anti-shock is 1 (00011xxx), invert both TG1 and TG2 when the internal anti-shock is H.

*5 RAM SET

***2 TRACKING MODE**

	D3	D2
OFF	0	0
ON	0	1
FWD JUMP	1	0
REV JUMP	1	1

***3 SLED MODE**

	D1	D0
OFF	0	0
ON	0	1
FWD MOVE	1	0
REV MOVE	1	1

***4 AUTO SEQUENCE**

	AS3	AS2	AS1	AS0
CANCEL	0	0	0	0
FOCUS ON	0	1	1	1
1 TRACK JUMP	1	0	0	X
10 TRACK JUMP	1	0	1	X
2N TRACK JUMP	1	1	0	X
M TRACK MOVE	1	1	1	X

X = 0 FORWARD
X = 1 REVERSE

- When CANCEL $40 is sent, the status immediately preceding the auto sequence mode (just before $4X is sent) is reset.
- The auto sequence mode starts with the first falling of the pin 40 input pulse (WDCK) after the $4X transfer and the falling of latch pulse.

***5 RAM SET**
- Values $0 to $E (not $F) can be set.
- The above set values are ones when WDCK (88.2KHz) is input to pin 40.
- The RAM is preset when the power is switched on and the internal initial set values are as follows:

Address	Data
0 1 0 1	0 1 0 1
0 1 1 0	0 1 1 1
0 1 1 1	1 1 1 0

- The actual count values are slightly different from the set values.

A	set value + 4 to 5	WDCK
B,D,E	set value + 3	WDCK
C	set value + 5	WDCK
N,M	set value + 3	Count out

SERIAL DATA TRUTH TABLE

Serial Data	Hexa.	Function
FOCUS CONTROL		FS = 4321
0 0 0 0 0 0 0 0	$00	0 0 0 0
0 0 0 0 0 0 0 1	$01	0 0 0 1
0 0 0 0 0 0 1 0	$02	0 0 1 0
0 0 0 0 0 0 1 1	$03	0 0 1 1
0 0 0 0 0 1 0 0	$04	0 1 0 0
0 0 0 0 0 1 0 1	$05	0 1 0 1
0 0 0 0 0 1 1 0	$06	0 1 1 0
0 0 0 0 0 1 1 1	$07	0 1 1 1
0 0 0 0 1 0 0 0	$08	1 0 0 0
0 0 0 0 1 0 0 1	$09	1 0 0 1
0 0 0 0 1 0 1 0	$0A	1 0 1 0
0 0 0 0 1 0 1 1	$0B	1 0 1 1
0 0 0 0 1 1 0 0	$0C	1 1 0 0
0 0 0 0 1 1 0 1	$0D	1 1 0 1
0 0 0 0 1 1 1 0	$0E	1 1 1 0
0 0 0 0 1 1 1 1	$0F	1 1 1 1
TRACKING CONTROL		AS = 0 TG = 2 1 / AS = 1 TG = 2 1
0 0 0 1 0 0 0 0	$10	0 0 / 0 0
0 0 0 1 0 0 0 1	$11	0 1 / 0 1
0 0 0 1 0 0 1 0	$12	1 0 / 1 0
0 0 0 1 0 0 1 1	$13	1 1 / 1 1
0 0 0 1 0 1 0 0	$14	0 0 / 0 0
0 0 0 1 0 1 0 1	$15	0 1 / 0 1
0 0 0 1 0 1 1 0	$16	1 0 / 1 0
0 0 0 1 0 1 1 1	$17	1 1 / 1 1
0 0 0 1 1 0 0 0	$18	0 0 / 1 1
0 0 0 1 1 0 0 1	$19	0 1 / 1 0
0 0 0 1 1 0 1 0	$1A	1 0 / 0 1
0 0 0 1 1 0 1 1	$1B	1 1 / 0 0
0 0 0 1 1 1 0 0	$1C	0 0 / 1 1
0 0 0 1 1 1 0 1	$1D	0 1 / 1 0
0 0 0 1 1 1 1 0	$1E	1 0 / 0 1
0 0 0 1 1 1 1 1	$1F	1 1 / 0 0

Serial Data	Hexa.	Function		
TRACKING MODE		DIRC = 1 TM = 654321	DIRC = 0 654321	DIRC = 1 654321
0 0 1 0 0 0 0 0	$20	000000	001000	000011
0 0 1 0 0 0 0 1	$21	000010	001010	000011
0 0 1 0 0 0 1 0	$22	010000	011000	100001
0 0 1 0 0 0 1 1	$23	100000	101000	100001
0 0 1 0 0 1 0 0	$24	000001	000100	000011
0 0 1 0 0 1 0 1	$25	000011	000110	000011
0 0 1 0 0 1 1 0	$26	010001	010100	100001
0 0 1 0 0 1 1 1	$27	100001	100100	100001
0 0 1 0 1 0 0 0	$28	000100	001000	000011
0 0 1 0 1 0 0 1	$29	000110	001010	000011
0 0 1 0 1 0 1 0	$2A	010100	011000	100001
0 0 1 0 1 0 1 1	$2B	100100	101000	100001
0 0 1 0 1 1 0 0	$2C	001000	000100	000011
0 0 1 0 1 1 0 1	$2D	001010	000110	000011
0 0 1 0 1 1 1 0	$2E	011000	010100	100001
0 0 1 0 1 1 1 1	$2F	101000	100100	100001

APPLICATION CIRCUIT

1. ±5V SPLIT POWER SUPPLY

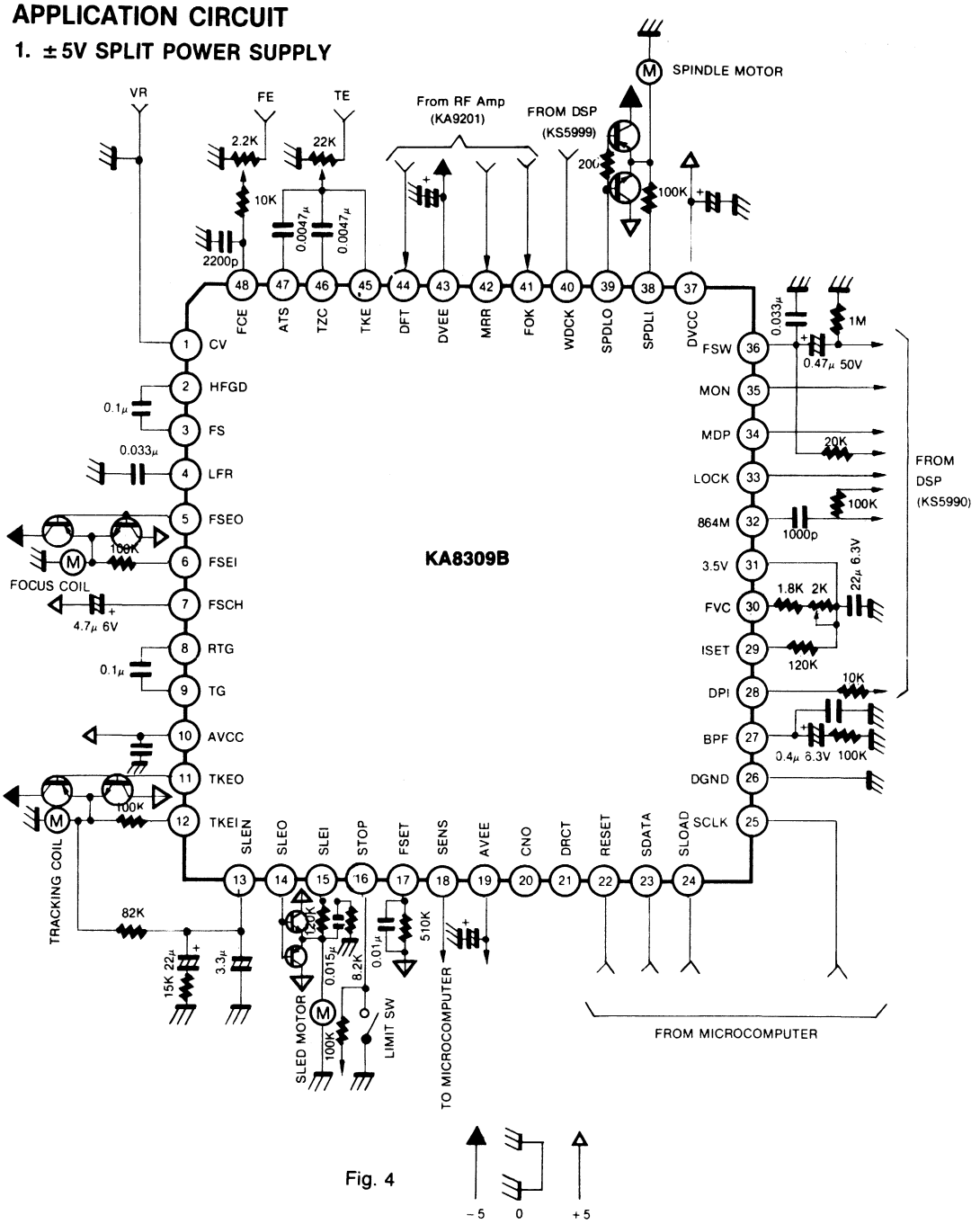


Fig. 4

2. +5V SINGLE POWER SUPPLY

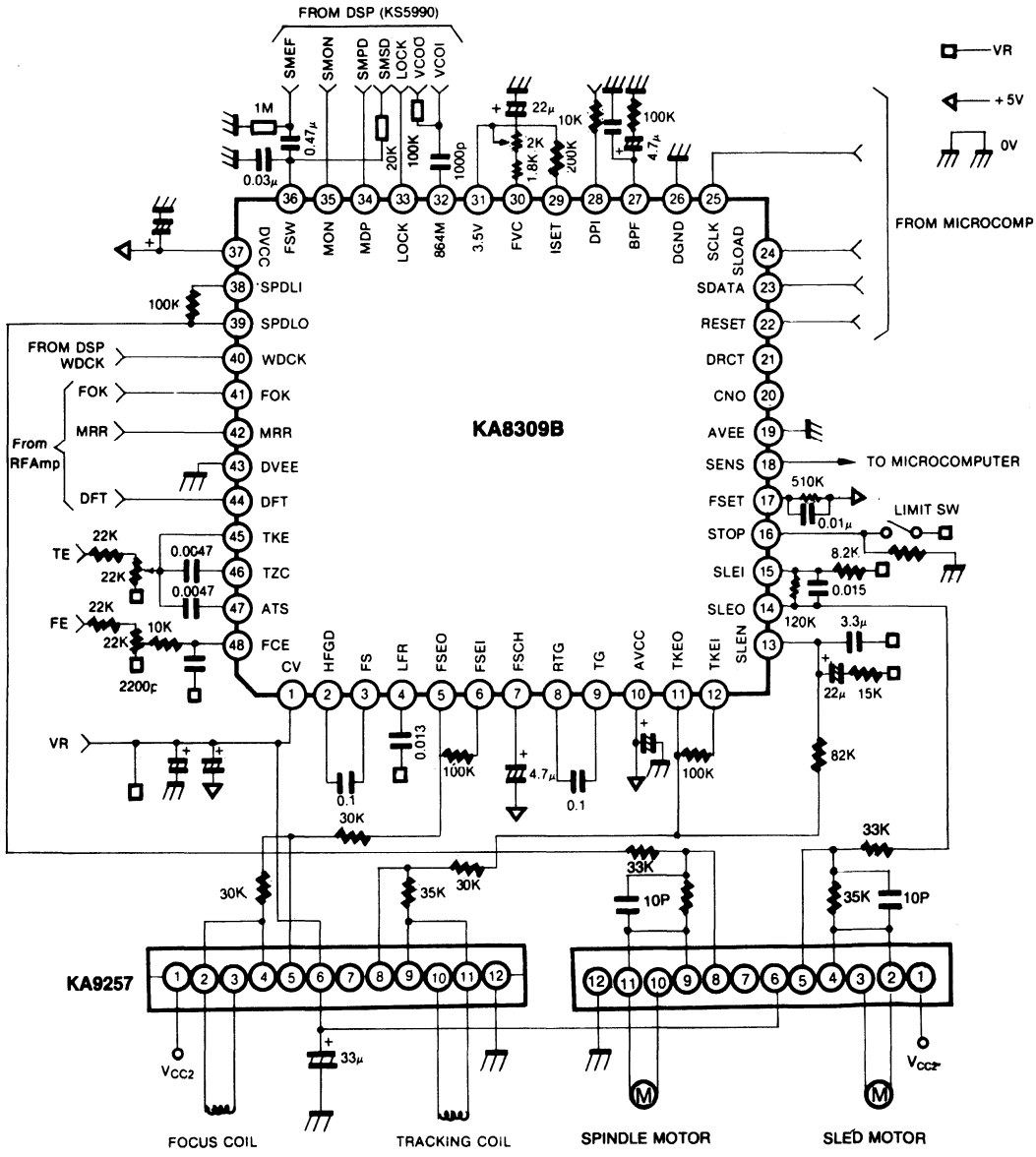
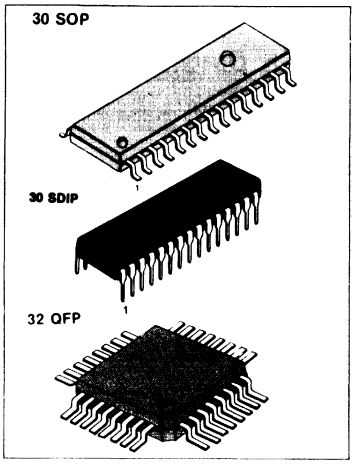


Fig. 5

RF AMP FOR CDP

The KA9201, which is the RF amplifier, is a monolithic integrated circuit designed for three-spot type optical pick-up of the compact disc player.
It consists of a RF signal processing circuit, Focus Error AMP, Tracking Error AMP, Focus OK Detector, Mirror Detector, Defect Detector, EFM Comparator and automatic power controller for laser diode.



FEATURES

- Functions: RF AMP
  Focus Error AMP
  Tracking Error AMP
  Focus OK Detector
  Mirror Detector
  Defect Detector
  EFM (Eight to Fourteen Modulation) Comparator
  Automatic Asymmetry Control AMP
  Center Voltage Buffer
  APC (Automatic Power Control) AMP for Photo-Diode and Laser-Diode drive

ORDERING INFORMATION

Device	Package	Operating Temperature
KA9201M	30 SDIP	-25°C ~ +75°C
KA9201D	30 SOP	
KA9201Q	32 QFP	

- Single power supply operation (+5V) as well as split power supply operation (±5V)
- Low power consumption (100mW at ±5V, 50mW at +5V)
- Built-in automaticpower controller use for P-sub and N-sub of the laser diode
- Minimum number of external components required
- Built-in disc defect detection circuit for improvement to play ability
- Recommend operation supply voltage range: V_{CC}-V_{EE}: 3.4 ~ 11V
  V_{CC}-D_{GND}: 3.4 ~ 5.5V
- Power Supply Condition:

	V_{CC}	V_{EE}	V_C	V_R (V_{ref})	D_{GND}
Single Power Supply	Power Supply	GND	V_R	VC	GND
Split Power Supply	+Power Supply	-Power Supply	D_{GND}	No Connecting	GND

BLOCK DIAGRAM

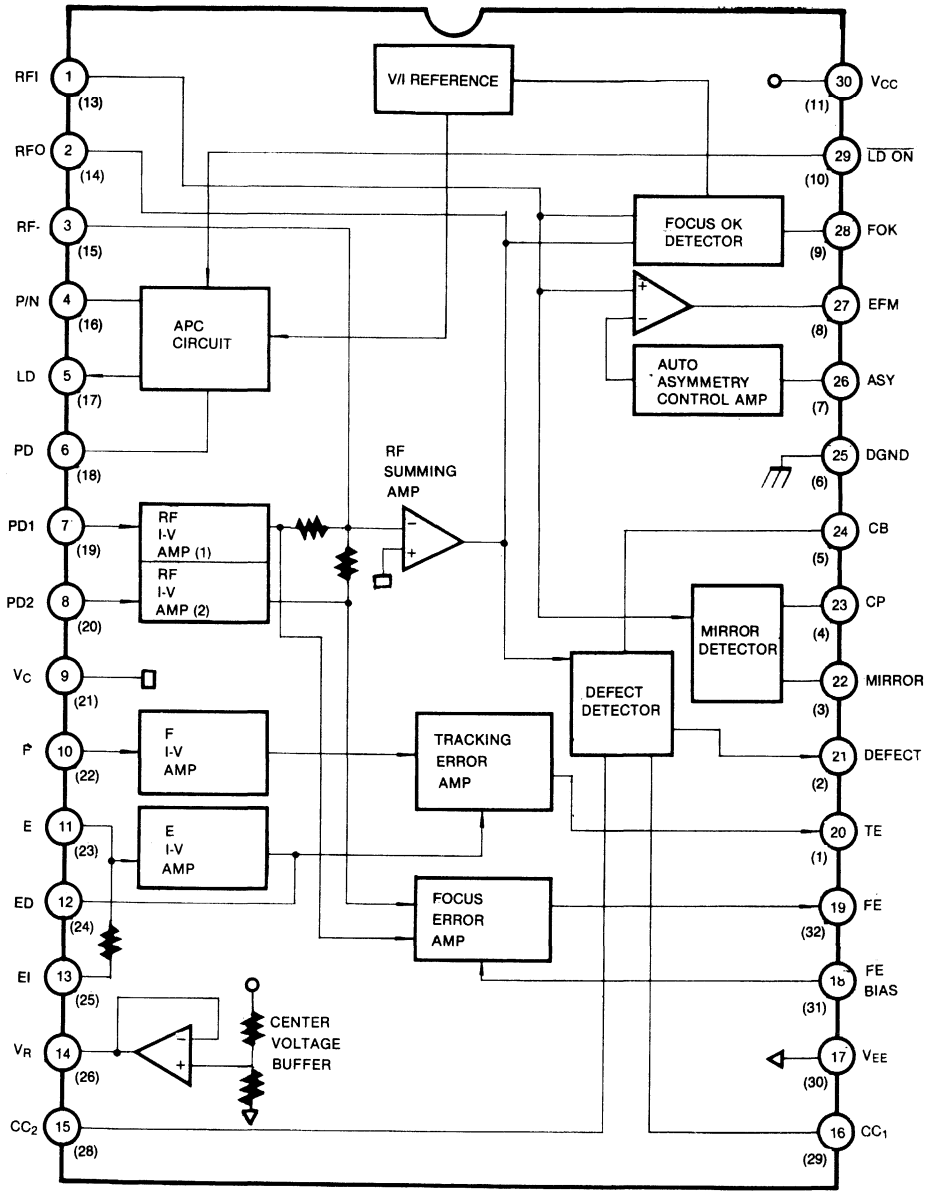


Fig. 1

· PIN12, 27 of 32 QFP is NC

* The number of ( ) is the TYPE of 32 QFP

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	$V_{CC} - V_{EE}$	12	V
Power Dissipation	P_D	800	mW
Operating Temperature	T_{OPR}	−25 ~ +75	°C
Storage Temperature	T_{STG}	−55 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 2.5V, $V_{EE} = D_{GND}$ = −2.5V, VC = GND, unless otherwise specified)

Stage	No	Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Circuit Current	1	V_{CC} Current	I_{CC}	DC Current	8.0	11.4	15.5	mA
	2	V_{EE} Current	I_{EE}		−15.0	−11.0	−7.5	mA
	3	D_{GND} Current	I_D (GND)		−1.1	−0.85	−0.6	mA
RF AMP	4	Input Offset Voltage	V_{IO1}	DC voltage	−50	0	50	mV
	5	Voltage Gain	G_{V1}	V_i = 2KHz, 40mV sinewave, Output; sinewave	25.1	28.1	31.1	dB
	6	Maximum Output Amplitude	$V_{O\,(MAX)\,1}$	V_i = 0.2V DC Output; + peak voltage	1.3			V
	7	Maximum Output Amplitude	$V_{O\,(MAX)\,2}$	V_i = −0.2V DC Output; − peak voltage			−0.3	V
Focus Error AMP	8	Input Offset Voltage	V_{IO2}	DC voltage	−20		120	mV
	9	Voltage Gain	G_{V2}	V_i = 1KHz, 32mV sinewave, Output; sinewave	27	30	33	dB
	10	Voltage Gain	G_{V3}		27	30	33	dB
	11	Gain Difference	ΔG_{V1}		−3	0	3	dB
	12	Maximum Output Amplitude H	$V_{OH\,(MAX)\,1}$	V_i = −0.2V DC Output; − peak voltage	1.9			V
	13	Maximum Output Amplitude L	$V_{OL\,(MAX)\,1}$	V_i = 0.2V DC Output; − peak voltage			−1.9	V
Tracking Error AMP	14	Input Offset Voltage	V_{IO3}	DC voltage	−50		50	mV
	15	Voltage Gain F	G_{V4}	V_i = 1KHz, 0.3V sinewave, input to output ratio Output; sinewave	7	10	13	dB
	16	Voltage Gain E	G_{V5}		7	10	13	dB
	17	Gain Difference	ΔG_{V2}		−3	0	3	dB
	18	Maximum Output Amplitude H	$V_{OH\,(MAX)\,2}$	V_i = 2.0V DC Output; + peak voltage	1.9			V
	19	Maximum Output Amplitude L	$V_{OL\,(MAX)\,2}$	V_i = −2.0V DC Output; − peak voltage			−1.9	V

ELECTRICAL CHARACTERISTICS (Continued)

Stage	No	Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
APC AMP	20	Output Voltage 1	V_{O1}	V_i = 190mV DC	1.4			V
	21	Output Voltage 2	V_{O2}	V_i = 90mV DC			-1.4	V
	22	Output Voltage 3	V_{O3}	V_i = 100mV DC	1.4			V
	23	Output Voltage 4	V_{O4}	V_i = 170mV DC			-1.4	V
	24	Output Voltage 5	V_{O5}	V_i = 0V DC	1.4			V
	25	Output Voltage 6	V_{O6}	V_i = 0V DC			-1.4	V
	26	Maximum Output Amplitude H	$V_{OH\ (MAX)\ 3}$	Va = 0V, Ia = -0.8mA Output; + peak voltage	0			V
	27	Maximum Output Amplitude L	$V_{OL\ (MAX)\ 3}$	Va = 0.6V, Ia = 0.8mA Output; - peak voltage			0	V
Focus OK	28	Threshold Voltage	V_{TH1}	V_i = output $(V_{CC} + D_{GND})/2$ must be adjusted by the DC voltage across RFI and RFO	-430	-390	-350	mV
	29	High Output Voltage	$V_{OH\ (FOK)\ 1}$	Input across RFI and RFO 1V, 375mV/(DC) sinewave, Output; pulse	2.2			V
	30	Low Output Voltage	$V_{OL\ (FOK)\ 1}$				1.8	V
	31	Maximum Operating Frequency	$f_{(MAX)}$		45			KHz
Mirror AMP	32	High Output Voltage	$V_{OH\ (MIR)\ 1}$	V_i = 10KHz 0.8V, -0.4V(DC) sinewave, Output; pulse	1.8			V
	33	Low Output Voltage	$V_{OL\ (MIR)\ 1}$				-2.2	V
	34	Mirror Hold Frequency Response	$f_{RES\ (M)}$	V_i = 0.8V, 0.2V(DC), f(carrier) = 500KHz AM modulation Output; pulse		400	600	Hz
	35	Bottom Hold Frequency Response	$f_{RES\ (B)}$	V_i = 0.8V, 0.4V(DC) sinewave, Output; pulse		500	900	Hz
	36	Maximum Input Operating Frequency	$f_{I\ (MAX)\ 1}$		30	70		KHz
	37	Minimum Input Voltage	$V_{I\ (MIN)\ 1}$	V_i = 10KHz, 0.4V(DC) sinewave, Output; pulse		0.1	0.2	V
	38	Maximum Input Voltage	$V_{I\ (MAX)\ 1}$		1.8			V
Defect AMP	39	High Output Voltage	$V_{OH\ (DEF)\ 1}$	V_i = 32mV, +15mV(DC) sinewave, Output; pulse	1.8			V
	40	Low Output Voltage	$V_{OL\ (DEF)\ 1}$				-2.2	V

ELECTRICAL CHARACTERISTICS (Continued)

Stage	No	Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Defect AMP	41	Minimum Input Operating Frequency	$f_{I\,(MIN)\,2}$	V_i = 32mV, +15mV/(DC) sinewave, Output; pulse		670	1000	Hz
	42	Maximum Input Operating Frequency	$f_{I\,(MAX)\,2}$		2.0	4.7		KHz
	43	Mininum Input Voltage	$V_{I\,(MIN)\,2}$	V_i = 50Hz, 15mV(DC) pulsewave, symmetry; 95% Output; pulse		0.3	0.5	V
	44	Maximum Input Voltage	$V_{I\,(MAX)\,2}$		1.8			V
EFM Comparator	45	Duty Cycle 1	D_1	V_i = 750KHz, 0.7V sinewave, Output; DC voltage	−50	0	50	mV
	46	Duty Cycle 2	D_2	V_i = 750KHz, 0.7V, +0.25V(DC) sinewave Output; DC voltage	0	50	100	mV
	47	High Output Voltage	$V_{OH\,(EFM)1}$	V_i = 750KHz, 0.7V sinewave Output; pulse	1.2			V
	48	Low Output Voltage	$V_{OL\,(EFM)1}$				−1.2	V
	49	Minimum Input Voltage	$V_{I\,(MIN)\,3}$	V_i = 750KHz sinewave Output; pulse			0.12	V
	50	Maximum Input Voltage	$V_{I\,(MAX)\,3}$		1.8			V
	51	Maximum Input Operating Frequency	$f_{I\,(MAX)\,3}$	V_i = 750KHz, 0.7V sinewave, Output; pulse	4.0			MHz
Center Voltage Buffer	52	Input Offset Voltage	V_{IO4}	DC voltage	−100	0	100	mV
	53	Maximum Output Current (+)	$I_{O+\,(MAX)}$		5			mA
	54	Maximum Output Current (−)	$I_{O-\,(MAX)}$				−5	mA
(Ta = 25°C, V_{CC} = 5.0V, V_{EE} = −5.0V, D_{GND} = VC = GND, unless otherwide specified)								
RF AMP	55	Maximum Output Amplitude (H)	$V_{OH\,(MAX)\,4}$	V_i = 0.2V DC Output; DC voltage	3.5			V
	56	Maximum Output Amplitude (L)	$V_{OL\,(MAX)\,4}$	V_i = −0.2V DC Output; DC voltage			0.3	V
Focus Error AMP	57	Maximum Output Amplitude (H)	$V_{OH\,(MAX)\,5}$	V_i = −0.2V DC Output; DC voltage	4.2			V
	58	Maximum Output Amplitude (L)	$V_{OL\,(MAX)\,5}$	V_i = 0.2V DC Output; DC voltage			−2.2	V
Tracking Error AMP	59	Maximum Output Amplitude (H)	$V_{OH\,(MAX)\,6}$	V_i = 2.0V DC Output; DC voltage	4.2			V
	60	Maximum Output Amplitude (L)	$V_{OL\,(MAX)\,6}$	V_i = −2.0V DC Output; DC voltage			−2.2	V

ELECTRICAL CHARACTERISTICS (Continued)

Stage	No	Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
APC AMP	61	Output Voltage 7	V_{O7}	V_i = 190mV DC Output DC voltage	1.4			V
	62	Output Voltage 8	V_{O8}	V_i = 90mV DC Output DC voltage			−1.4	V
	63	Output Voltage 9	V_{O9}	V_i = 100mV DC Output DC voltage	1.4			V
	64	Output voltage 10	V_{O10}	V_i = 170mV DC Output DC voltage			−1.4	V
	65	Output Voltage 11	V_{O11}	V_i = 0V DC Output DC voltage	3.8			V
	66	Output Voltage 12	V_{O12}	V_i = 190mV DC Output DC voltage			−3.8	V
	67	Maximum Output Amplitude H	$V_{OH\ (MAX)\ 7}$	Va = 0V DC, Ia = −0.8mA Output; DC voltage	2.5			V
	68	Maximum Output Amplitude L	$V_{OL\ (MAX)\ 7}$	Va = 0.6V DC, Ia = 0.8mA Output; DC voltage			−2.5	V
Focus OK AMP	69	Threshold Voltage	V_{TH2}	Input DC voltage; output $(V_{CC} + D_{GND})/2$ must be adjusted by the DC voltage across RFI And RFO	−430	−390	−350	mV
	70	High Output Voltage	$V_{OH\ (FOK)\ 2}$	V_i = 1V, −375mV(DC) across RFI and RFO; sinewave, Output; pulse	4.7			V
	71	Low Output Voltage	$V_{OL\ (FOK)\ 2}$				0.7	V
Mirror AMP	72	High Output Voltage	$V_{OH\ (MIR)\ 2}$	V_i = 10KHz 0.8V, −0.4V(DC) sinewave, Output; pulse	4.3			V
	73	Low Output Voltage	$V_{OL\ (MIR)\ 2}$				0.3	V
Defect AMP	74	High Output Voltage	$V_{OH\ (DEF)\ 2}$	V_i = 1KHz 32mV, +15mV(DC) sinewave, Output; pulse	4.3			V
	75	Low Output Voltage	$V_{OL\ (DEF)\ 2}$				−0.3	V
EFM Comparator	76	Duty 3	D_3	V_i = 750KHz 0.7V sinewave Output; DC voltage	2.45	2.50	2.55	V
	77	Duty 4	D_4	V_i = 750KHz 0.7V, +0.25V(DC) sinewave Output; pulse	2.50	2.55	2.60	V
	78	High Output Voltage	$V_{OH\ (EFM)\ 2}$	V_i = 750KHz 0.7V, sinewave, Output; pulse	3.7			V
	79	Low Output Voltage	$V_{OL\ (EFM)\ 2}$				1.3	

TEST CIRCUIT

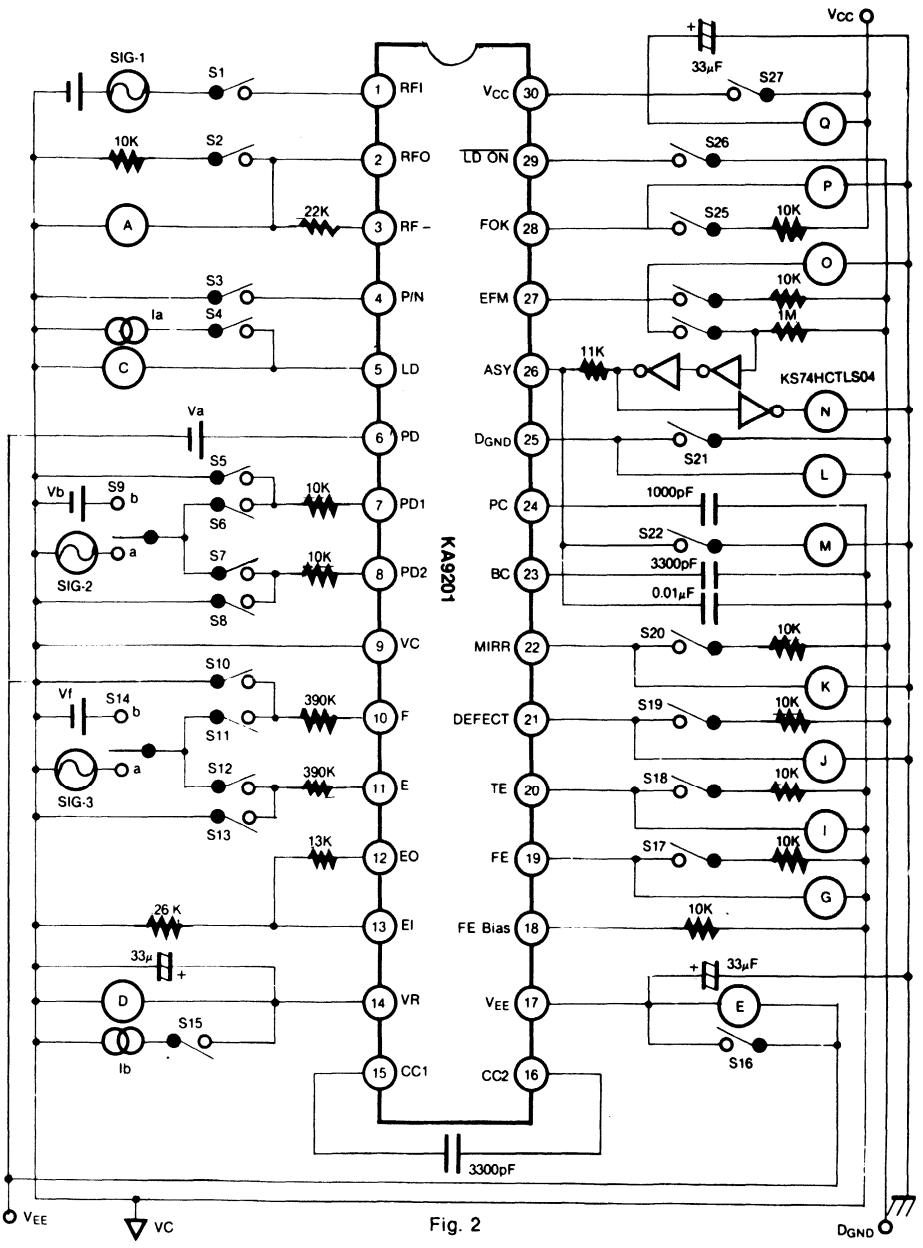


Fig. 2

*) Note: KS74HCTLS04: Supply Voltage = 5V

TEST METHODE (SWITCH CONDITION) (V_{CC} = 2.5V, V_{EE} = D_{GND} = − 2.5V, V_C = GND)

Stage	No	Characteristic	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16	S17	S18	S19	S20	S21	S22	S23	S24	S25	S26	S27	Input	Test Point
Circuit Current	1	I_{CC}			ON													ON	ON	ON	ON	ON	ON				ON	ON		—	Q
	2	I_{EE}			ON														ON	ON	ON	ON	ON				ON	ON	ON	—	E
	3	$I_{D\ (GND)}$																ON	ON	ON	ON	ON					ON		ON	—	L
RF AMP	4	V_{IO1}			ON													ON					ON					ON	ON	—	A
	5	G_{V1}						ON	ON									ON					ON						ON	SIG-2	A
	6	$V_{O\ (MAX)\ 1}$		ON				ON	ON		b							ON					ON						ON	V_b	A
	7	$V_{O\ (MAX)\ 2}$		ON				ON	ON		b							ON					ON						ON	V_b	A
Focus Error AMP	8	V_{IO2}																ON					ON					ON	ON	—	G
	9	G_{V2}						ON		ON	a							ON					ON						ON	SIG-2	G
	10	G_{V3}					ON		ON		a							ON					ON						ON	SIG-2	G
	11	ΔG_{V1}																													
	12	$V_{OH\ (MAX)\ 1}$						ON		ON	b								ON	ON				ON						ON	V_b	G
	13	$V_{OL\ (MAX)\ 1}$						ON		ON	b							ON	ON				ON						ON	V_b	G
Tracking Error AMP	14	V_{IO3}			ON													ON					ON					ON	ON	—	I
	15	G_{V4}											ON		ON	a		ON					ON						ON	SIG-3	I
	16	G_{V5}										ON		ON		a		ON					ON						ON	SIG-3	I
	17	ΔG_{V2}																													
	18	$V_{OH\ (MAX)\ 2}$											ON		ON	b		ON		ON			ON						ON	Vt	I
	19	$V_{OL\ (MAX)\ 2}$											ON		ON	b		ON		ON			ON						ON	Vt	I
APC AMP	20	V_{O1}																ON					ON					ON	ON	Va	C
	21	V_{O2}																ON					ON					ON	ON	Va	C
	22	V_{O3}			ON													ON					ON					ON	ON	Va	C
	23	V_{O4}			ON													ON					ON					ON	ON	Va	C
	24	V_{O5}																ON					ON						ON	Va	C
	25	V_{O6}			ON													ON					ON						ON	Va	C
	26	$V_{OH\ (MAX)\ 3}$			ON	ON												ON					ON					ON	ON	Va, Ia	C
	27	$V_{OL\ (MAX)\ 3}$			ON	ON												ON					ON					ON	ON	Va, Ia	C
Focus OK AMP	28	V_{TH1}	ON															ON					ON				ON		ON	SIG-1	P
	29	$V_{OH\ (FOK)\ 1}$	ON															ON					ON				ON		ON	SIG-1	P
	30	$V_{OL\ (FOK)\ 1}$	ON															ON					ON				ON		ON	SIG-1	P
	31	$f_{(MAX)}$	ON															ON					ON				ON		ON	SIG-1	P
Mirror AMP	32	$V_{OH\ (MIR)\ 1}$	ON															ON				ON	ON						ON	SIG-1	K
	33	$V_{OL\ (MIR)\ 1}$	ON															ON				ON	ON						ON	SIG-1	K
	34	$f_{RES\ (M)}$	ON															ON				ON	ON						ON	SIG-1	K
	35	$f_{RES\ (B)}$	ON															ON				ON	ON						ON	SIG-1	K
	36	$f_{I\ (MAX)\ 1}$	ON															ON				ON	ON						ON	SIG-1	K
	37	$f_{I\ (MIN)\ 1}$	ON															ON				ON	ON						ON	SIG-1	K
	38	$V_{I\ (MAX)\ 1}$	ON															ON				ON	ON						ON	SIG-1	K

TEST METHODE (SWITCH CONDITION) (Continued)

Stage	No	Characteristic	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16	S17	S18	S19	S20	S21	S22	S23	S24	S25	S26	S27	Input	Test Point
Defect AMP	39	$V_{OH\ (DEF)\ 1}$						ON	ON		a							ON			ON		ON						ON	SIG-2	J
	40	$V_{OL\ (DEF)\ 1}$						ON	ON		a							ON			ON		ON						ON	SIG-2	J
	41	$f_{I\ (MIN)\ 2}$						ON	ON		a							ON			ON		ON						ON	SIG-2	J
	42	$f_{I\ (MAX)\ 2}$						ON	ON		a							ON			ON		ON						ON	SIG-2	J
	43	$V_{I\ (MIN)\ 2}$						ON	ON		a							ON			ON		ON						ON	SIG-2	J
	44	$V_{I\ (MAX)\ 2}$						ON	ON		a							ON			ON		ON						ON	SIG-2	J
EFM Comparator	45	D_1	ON		ON													ON					ON	ON	ON				ON	SIG-1	M
	46	D_2	ON		ON													ON					ON	ON	ON				ON	SIG-1	M
	47	$V_{OH\ (EFM)\ 1}$	ON															ON					ON		ON	ON			ON	SIG-1	O
	48	$V_{OL\ (EFM)\ 1}$	ON															ON					ON		ON	ON			ON	SIG-1	O
	49	$V_{I\ (MIN)\ 3}$	ON															ON					ON	ON					ON	SIG-1	N
	50	$V_{I\ (MAX)\ 3}$	ON															ON					ON	ON					ON	SIG-1	N
	51	$f_{I\ (MAX)\ 3}$	ON															ON					ON	ON					ON	SIG-1	N
Center Voltage Buffer	52	V_{IO4}			ON													ON					ON						ON	—	D
	53	$I_{O+\ (MAX)}$			ON												ON	ON					ON						ON	Ib	D
	54	$I_{O-\ (MAX)}$			ON												ON	ON					ON						ON	Ib	D
(V_{CC} = 5.0V, V_{EE} = −5.0V, D_{GND} = V_C = GND)																															
RF AMP	55	$V_{OH\ (MAX)\ 4}$		ON				ON	ON		b							ON					ON						ON	Vb	A
	56	$V_{OL\ (MAX)\ 4}$		ON				ON	ON		b							ON					ON						ON	Vb	A
Focus Error AMP	57	$V_{OH\ (MAX)\ 5}$						ON		ON	b							ON	ON				ON						ON	Vb	G
	58	$V_{OL\ (MAX)\ 5}$						ON		ON	b							ON	ON				ON						ON	Vb	G
Tracking Error AMP	59	$V_{OH\ (MAX)\ 6}$											ON		ON	b		ON		ON			ON						ON	Vt	I
	60	$V_{OL\ (MAX)\ 6}$											ON		ON	b		ON		ON			ON						ON	Vt	I
APC AMP	61	V_{O7}																ON					ON					ON	ON	Va	C
	62	V_{O8}																ON					ON					ON	ON	Va	C
	63	V_{O9}			ON													ON					ON					ON	ON	Va	C
	64	V_{O10}			ON													ON					ON					ON	ON	Va	C
	65	V_{O11}																ON					ON						ON	Va	C
	66	V_{O12}			ON													ON					ON						ON	Va	C
	67	$V_{OH\ (MAX)\ 7}$			ON	ON												ON					ON					ON	ON	Va, Ia	C
	68	$V_{OL\ (MAX)\ 7}$			ON	ON												ON					ON					ON	ON	Va, Ia	C
Focus OK AMP	69	V_{TH2}	ON															ON					ON				ON		ON	SIG-1	P
	70	$V_{OH\ (FOK)\ 2}$	ON															ON					ON				ON		ON	SIG-1	P
	71	$V_{OL\ (FOK)\ 2}$	ON															ON					ON				ON		ON	SIG-1	P
Mirror AMP	72	$V_{OH\ (MIR)\ 2}$	ON															ON				ON	ON						ON	SIG-1	K
	73	$V_{OL\ (MIR)\ 2}$	ON															ON				ON	ON						ON	SIG-1	K
Defect AMP	74	$V_{OH\ (DEF)\ 2}$						ON	ON		a							ON			ON		ON						ON	SIG-2	J
	75	$V_{OL\ (DEF)\ 2}$						ON	ON		a							ON			ON		ON						ON	SIG-2	J
EFM Comparator	76	D_3	ON		ON													ON					ON	ON	ON				ON	SIG-1	M
	77	D_4	ON		ON													ON					ON	ON	ON				ON	SIG-1	M
	78	$V_{OH\ (EFM)\ 2}$	ON															ON					ON		ON	ON			ON	SIG-1	O
	79	$V_{OL\ (EFM)\ 2}$	ON															ON					ON		ON	ON			ON	SIG-1	O

APPLICATION CIRCUIT

1) +5V Single Power Supply for P-sub Laser Diode

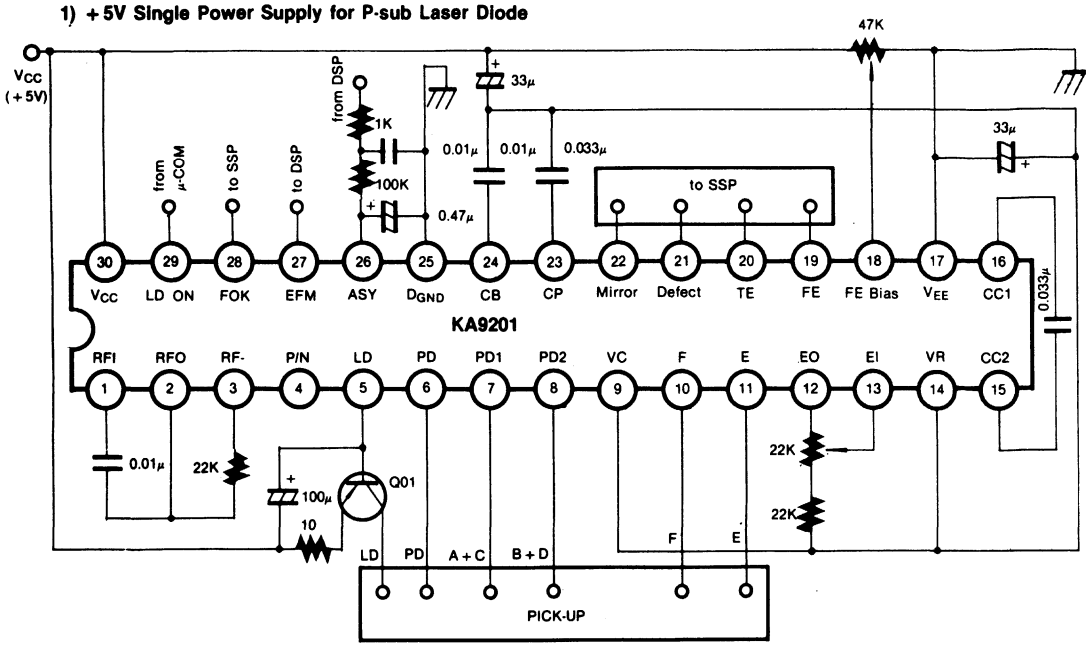


Fig. 3

2) +5V Single Power Supply for N-sub Laser Diode

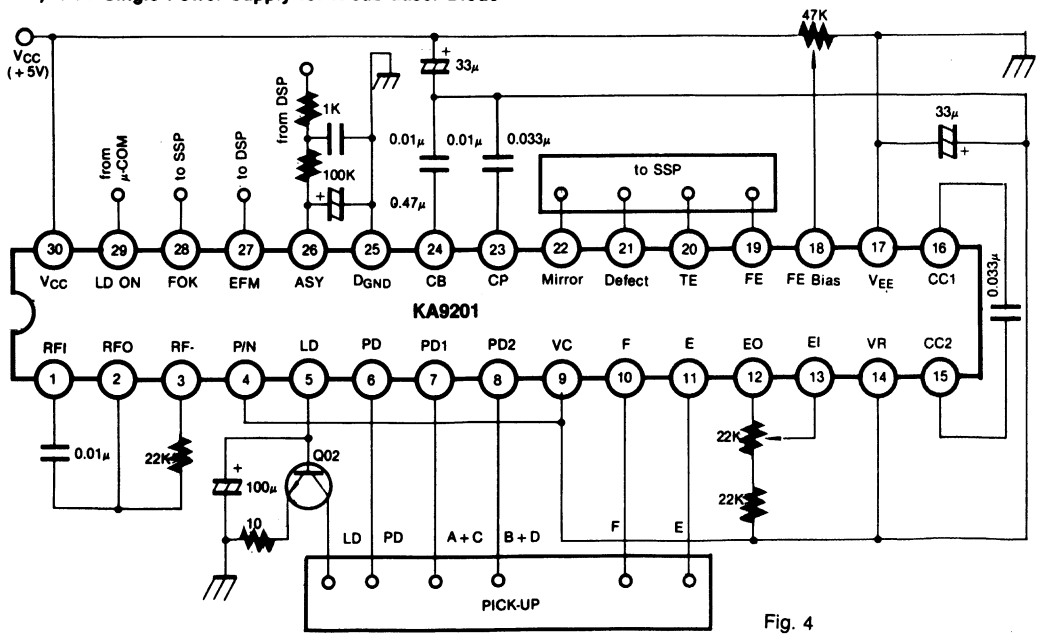


Fig. 4

APPLICATION CIRCUIT

3) ± 5V Split Power Supply for P-sub Laser Diode

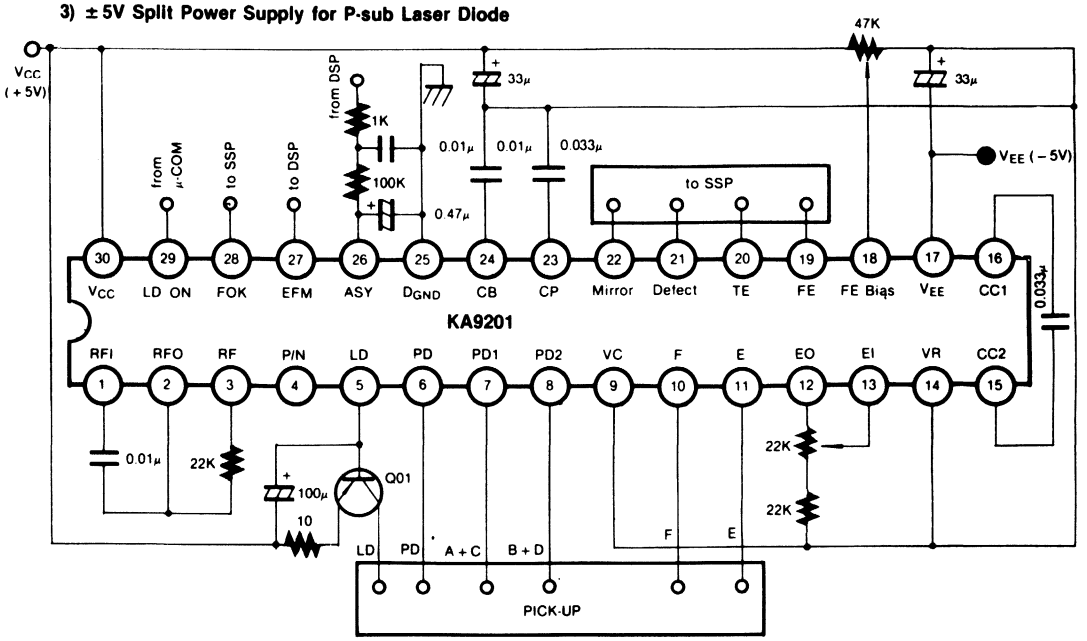


Fig. 5

4) ± 5V Split Power Supply for N-sub Laser Diode

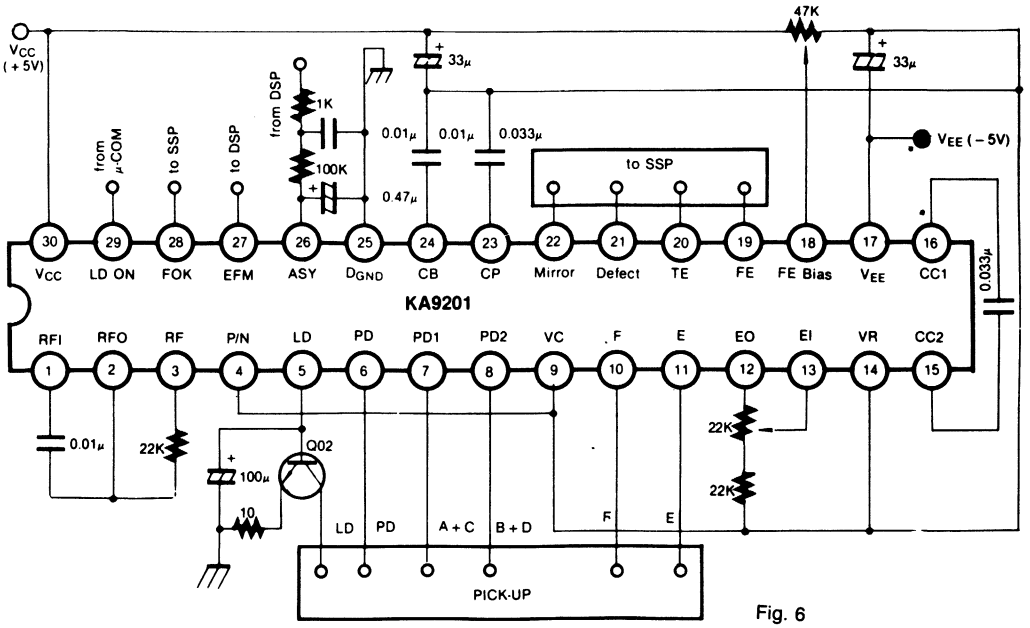
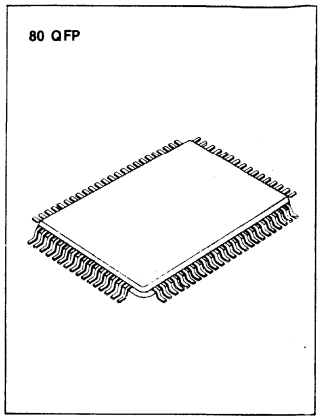


Fig. 6

DIGITAL SIGNAL PROCESSOR

The KS9210 which is CDP DSP IC improved digital filter characteristic includes digital audio output to interface other system directly.



FEATURES

- **EFM Phase detector circuit**
- **EFM data demodulator**
- **Include sync frame detection, protection, and injection circuit**
- **Correction of C1, C2 error**
- **Interpolator**
- **Subcode data processor**
- **CLV-servo controller**
- **Tracking counter**
- **μ-com interface**
- **Digital filter (Linear-phase FIR)**
- **S-RAM address generator**
- **16K SRAM**
- **Digital Audio out**
- **1.2μm CMOS process**

ORDERING INFORMATION

Device	Package	Operating Temperature
KS9210	80 QFP	−20°C ~ +75°C

BLOCK DIAGRAM

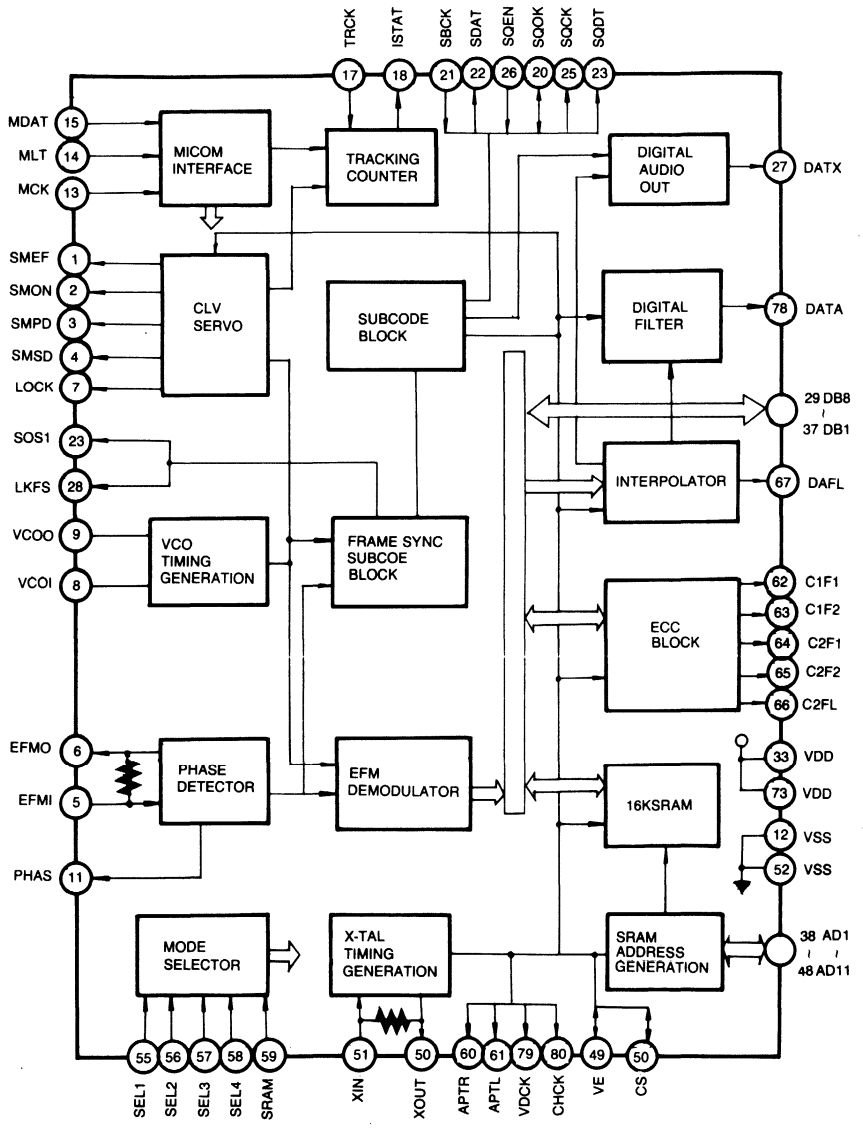


Fig. 1

PIN CONFIGURATION

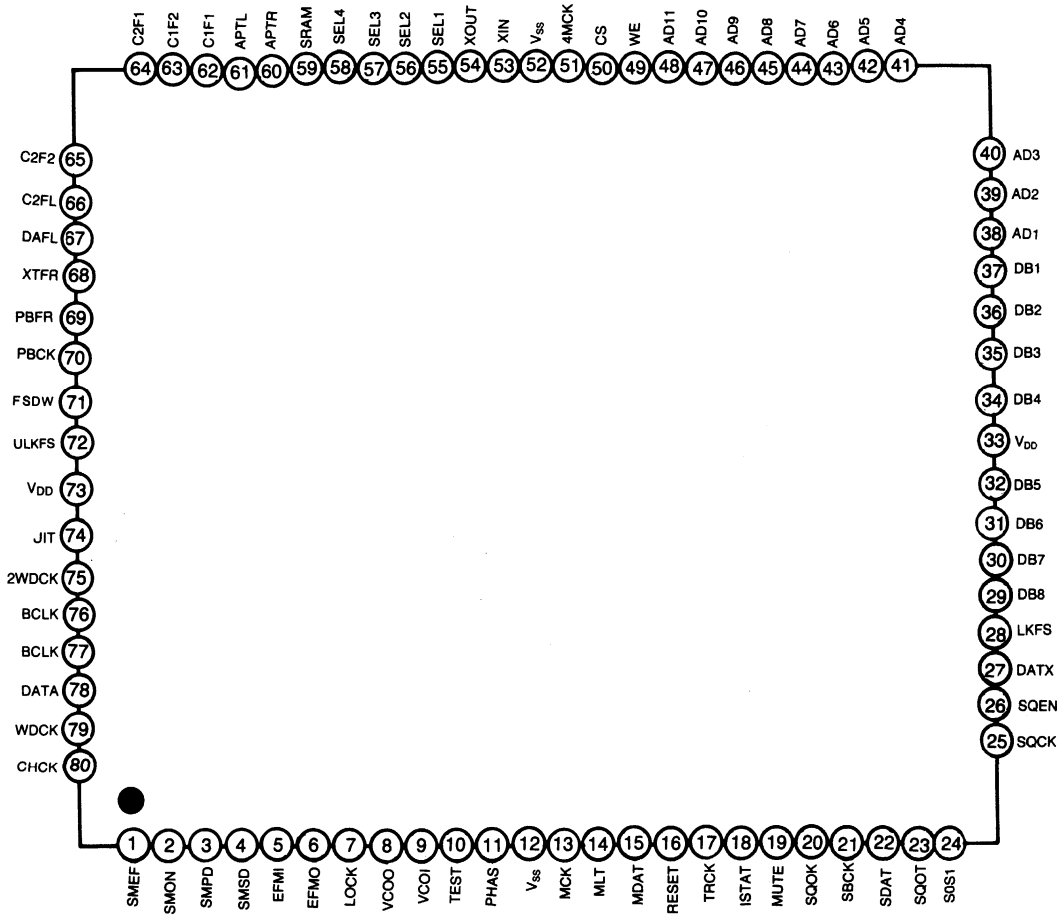


Fig. 2

PIN DESCRIPTION

Pin No	Symbol	I/O	Description
1	SMEF	O	LPF time constant control signal of the spindle motor error signal
2	SMON	O	On/Off control signal for the spindle motor
3	SMPD	O	Spindle motor drive, (Rough control in the S-Mode, phase control in the P-Mode)
4	SMSD	O	Spindle motor drive. Velocity control in the P-Mode
5	EFMI	I	EFM signal input terminal
6	EFMO	O	Slice level control signal of EFM signal
7	LOCK	O	Output signal of LKFS conditions sampled $\frac{PBFR}{16}$ (if LKFS is 'H', Lock is 'H'. If the LKFS is sampled "L" at test 8 times by $\frac{PBFR}{16}$, Lock is 'L')
8	V_{COO}	O	V_{CO} Output, when PBFR is locked the frequency is 8.6436 MHz
9	V_{COI}	I	V_{CO} Input
10	TEST	I	Momal operating is 'L', TEST is 'H'
11	PHAS	O	Phase comparison output signal between EFM and $V_{COI}/2$
12	V_{SS}	—	Ground
13	MCK	I	DATA Transportation clock from μ-com
14	MLT	I	LATCH CLOCK from μ-com
15	MDAT	I	DATA from μ-com
16	RESET	I	System reset at 'L'
17	TRCK	I	Tracking counter input puise signal
18	ISTAT	O	Output internal condition as designated by address
19	MUTE	I	Muting input
20	SQOK	O	Output the CRC check result of sub mode Q Data
21	SBCK	I	Clock signal to output Subcode Data
22	SDAT	O	Serial output of Subcode Data
23	SQDT	O	Output of Subcode Q Data
24	S0S1	O	Output of Subcode Sync Signal (S0 + S1)
25	SQCK	I/O	Clock to output Subcode Q Data
26	SQEN	I	SQCK I/O selection terminal ('L': SQCK output, 'H': SQCK input)
27	DATX	O	Digital Audio Output
28	LKFS	O	Output the Lock Conditions of frame sync
29	DB8	I/O	CMSB
~	~	~	Hi-2 at the normal operating (TEST = "L", SRAM = "L")
32	DB5	I/O	Data In/output at SRAM TEST
33	V_{DD}	—	+ 5V
34	DB4	I/O	
~	~	~	
37	DB1	I/O	(LSB)

PIN DESCRIPTION (Continued)

Pin No	Symbol	I/O	Description
38	AD1	I/O	(LSB) Hi-2 at the normal operating (TEST = 'L', SRAM = 'L')
~	~	~	in/output at test (TEST = 'H', SRAM = 'H')
48	AD11	I/O	(MSB)
49	WE	I/O	Hi-Z output at the normal operating, and Write enable input at the SRAM test
50	CS	I/O	Hi-Z output at the normal operating Chip enable input at the SRAM test
51	4MCK	O	Divider output of X_{IN} f = 4.2336 MHz
52	V_{SS}	—	Ground
53	X_{IN}	I	Input terminal of crystal oscillation circuit. According to mode, f = 8.4672 MHz or 16.9344 MHz
54	X_{OUT}	O	Output terminal of crystal oscillation circuit
55	SEL1	I	Mode selection terminal 1
56	SEL2	I	Mode selection terminal 2
57	SEL3	I	Mode selection terminal 3
58	SEL4	I	Mode selection terminal 4
59	SRAM	I	Normal operating = 'L', TEST = 'H'
60	APTR	O	Output to compensate R-CH Aperture ('H' = R-CH)
61	APTL	O	Output to compensate L-CH Aperture ('H' = L-CH)
62	C1F1	O	Output when SEL4 is 'L'
63	C1F2	O	Output when SEL4 is 'L'
64	C2F1	O	Output when SEL4 is 'L'
65	C2F2	O	Output when SEL4 is 'L'
66	C2FL	O	Output when SEL4 is 'L'
67	DAFL	O	Output when SEL4 is 'L'
68	XTFR	O	Output when SEL4 is 'L'
69	PBFR	O	Output when SEL4 is 'L'
70	PBCK	O	Output when SEL4 is 'L'
71	FSDW	O	Output when SEL4 is 'L'
72	ULKFS	O	Output when SEL4 is 'L'
73	V_{DD}	—	+5V
74	JIT	O	Output when SEL4 is 'L'
75	2WDCK	O	Output when SEL4 is 'L'
76	BLCK	O	Output when SEL4 is 'L'
77	BLCK	O	Output when SEL4 is 'L'
78	DATA	O	Output when SEL4 is 'L'
79	WDCK	O	Strobe signal digital filter on = 176.4 KHz off = 88.2 KHz
80	CHCK	O	Strobe signal digital filter on = 88.2 KHz off = 44.1 KHz

Notes) 1. XTFR : 7.35 KHz frame sync signal made by X'tal.
2. $\overline{\text{PBFR}}$: 7.35 KHz frame sync signal of PLAY BACK made by DATA which being reproduced.
3. $\overline{\text{PBCK}}$: Channel bit clock of DATA which being reproduced.
$\frac{V_{COI}}{2}$ at the normal mode.
4. FSDW : Unprotected frame sync.
5. $\underline{\text{ULKFS}}$: FRAME sync protection condition.
6. $\overline{\text{JIT}}$: Display of either RAM overflow or underflow for ± 4 frame jitter margin.
7. 2WDCK : Strobe signal
Digital filter On = 352.8 KHz
Off = 176.4 KHz
8. BLCK : BIT CLOCK Output signal. Digital filter On = 4.2336 MHz
Off = 2.1168 MHz

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{DD}	−0.3 ~ +7	V
Input Voltage	V_I	−0.3 ~ +7	V
Output Voltage	V_O	−0.3 ~ +7	V
Operating Temperature	T_{OPR}	−20 ~ +75	°c
Storage Temperature	T_{STG}	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(V_{DD} = 5V ± 10%, V_{SS} = 0V, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Input High Voltage	V_{IH1}	Note 1	0.7V_{DD}		V_{DD}	V
Input Low Voltage	V_{LH1}	Note 1	0		0.3V_{DD}	V
Input High Voltage	V_{IH2}	Note 2	0.8V_{DD}			V
Input Low Voltage	V_{LH2}	Note 2			0.2V_{DD}	V
Output High Voltage	V_{OH}	I_{OH} = −1mA	V_{DD} − 0.5		V_{DD}	V
Output Low Voltage	V_{OL}	I_{OL} = 1mA	0		0.4	V
Input Leakage Current	I_{LKG}	V_{IN} = 0 ~ 5.5V			±5	μA
Three State Pin Output Leakage Current	I_{LKG}	V_{OUT} = 0 ~ 5.5V			±5	μA

Note 1. Related Pins – EFMI, RESET, TEST, MUTE, SEL 2 ~ 5, MLT, MDAT, SQEN. SQCK.
Note 2. Related Pins – TRCK, MCK, SRAM

2. AC Characteristics

A. X_{IN} and V_{COI} terminal

(V_{DD} = 5V ± 10%, V_{SS} = 0V, T_{OPR} = 0 ~ +70°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Oscillation Frequency	f_{OSC}				18	MHz

B. Pins MCK, MDAT, MLT, TRCK, SQCK
(V_{DD} = 5.0V ± 10%, V_{SS} = 0V, T_{OPR} = 25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Clock Frequency	f_{CK1}			1	MHz
Clock Pulse Width	t_{WCK1}	300			nS
Set Up Time	t_{SU}	300			nS
Hold Time	t_H	300			nS
Delay Time	t_D	300			nS
Latch Pulse Width	t_W	300			nS
TRCK, SQCK frequency	t_{CK2}			1	MHz
TRCK, SQCK Frequency, Pulse Width	t_{WCK2}	300			nS

C. D/Ā Converter Interface Terminal
(Pins CHCK, WDCK, APTR, APTL, C1F1, C1F2, C2FL, DAFL, XTFR, 2WDCK, DATA)

Item	Symbol	DF OFF			DF ON			Unit
		Min	Typ	Max	Min	Typ	Max	
Clock Pulse Width	t_{WCK}		236			118		nS
Clock Skew (FAST)	t_{FCK}			40			40	nS
DATA Skew (FAST)	$t_{F(SK)}$			0			0	nS
DATA Skew (Delay)	$t_{D(SK)}$			8			80	nS

APPLICATION INFORMATION

1. MODE SELECTOR

SEL1	SEL2	SEL3	SEL4	SRAM	XIN	BO	DF	DAC		AUDIO /ROM	16KSRAM
								P/S	2S/OB		
O	O	O	O	O	16M	ON	ON	S	2S	AUDIO	internal
O	O	O	I	O	↓	↓	↓	P	OB	↓	↓
O	O	I	O	O	↓	↓	OFF	S	2S	↓	↓
O	I	O	O	O	↓	OFF	ON	↓	↓	↓	↓
O	I	O	I	O	↓	↓	↓	P	OB	↓	↓
O	I	I	O	O	↓	↓	OFF	S	2S	↓	↓
O	I	I	I	O	↓	↓	↓	P	OB	↓	↓
I	O	O	O	O	8M	↓	ON	S	2S	↓	↓
I	O	O	I	O	↓	↓	↓	P	OB	↓	↓
I	O	I	O	O	↓	↓	OFF	S	2S	↓	↓
I	O	I	I	O	↓	↓	↓	P	OB	↓	↓
I	I	I	O	O	16M	ON	↓	S	2S	↓	↓
I	I	I	I	O	8M	OFF	↓	↓	↓	ROM	↓

1) X_{IN} is the input terminal of crystal oscillator.
   16M = 16.9344 MHz, 8M = 8.4672 MHz
2) DF is internal digital filter
   On condition: Output the data after pass by filter
   Off condition: The opposite of ON condition
   DO shows digital audio out
3) S of DAC is outputed serially to PAD 78 and 2S is 2's complement.
   OB is OFFSET BINARY and shows inversed MSB.
4) When SRAM is 'L', use internal SRAM.
5) Audio use Audio Application and ROM use CD-ROM application in the Audio/ROM.

2. μ-Com Interface

The DATA inputed from μ-Com is inputed to MDAT and transfered by MCK.
The signal is inputed to MLT terminal in order that the data inputed is loaded to one of six control register.

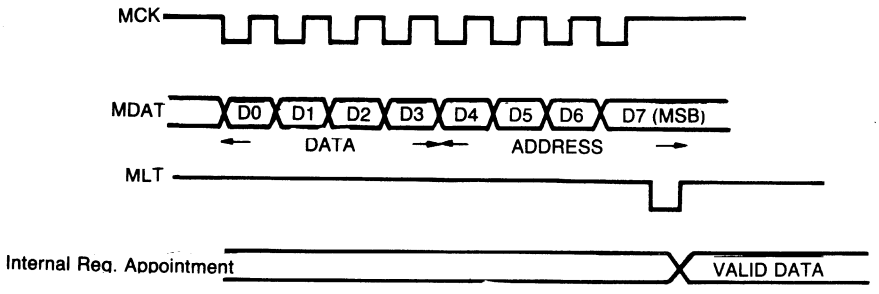


Fig. 3 μ-COM DATA INPUT TIMING CHART

CONTROL REGISTER	COMMENT	ADDRESS D7~D4	DATA D3	D2	D1	D0	JSTAT TERMINAL
CNTL-Z	DATA CONTROL	1001	ECMT	HIPD	NCLV	CRCD	Hi-Z
CNTL-S	FRAME SYNC PROTECTION ATTENUATION CONTROL	1010	FSEM	FSEL	WSEL	ATTM	Hi-Z
CNTL-L	TRACKING COUNTER LOWER 4 BIT	1011	TRC3	TRC2	TRC1	TRC0	$\overline{\text{COMPLETE}}$
CNTL-U	TRACKING COUNTER UPPER 4 BIT	1100	TRC7	TRC6	TRC5	TRC4	$\overline{\text{COUNT}}$
CNTL-W	CLV CONTROL	1101	COM	WB	WP	GAIN	Hi-Z
CNTL-C	CLV MODE	1110	CLV-MODE				$\overline{\text{PW}\geqq 64}$

Table 1. Control Register Selection μ-Com Data

1) CNTL-Z REGISTER

It is a register to control zero cross mute of audio data, phase terminal, control signal of phase servo, and have or not of CRCF DATA in SQDT.

		DATA = 0	DATA = 1
ZCMT	D3	Zero cross mute is off	ON
HIPD	D2	It operate PHAS normally	LKFS became "L" to "Hi-Z"
NCLV	D1	Phase servo being acted by frame sync	Phase servo being acted by base counter
CRCQ	D0	SQDT output except SQOK	SQDT is CRCF during rising time

2) CNTL-S Register

It is a register to control FRAME SYNC, PROTECTION, ATTENUATION.... etc.

FSEM	FSEL	FRAME
0	0	2
0	1	4
1	0	8
1	1	13

WSEL	CLOCK
0	±3
1	±7

ATTM	MUTE	dB
0	0	0
0	1	$-\infty$
1	0	-12
1	1	-12

3) CNTL-L, U REGISTER

After the number of track that must be counted is inputed from μ-com, The Data is loaded to tracking counter by CNTL-L, U register

4) CNTL-W Register

		DATA = 0	DATA = 1	Comments
COM	D3	XTFR/4 & PDFR/4	XTFR/4 & PBFR/4	Phase comparative frequency control during phase-mode
WB	D2	XTFR/32	XTFR/16	Bottom hold period control during speed, or H speed-mode
WP	D1	XTFR/4	XTFR/2	PEAK hold period control during speed-mode
GAIN	D0	-12dB	0dB	SMPD gain control during speed, or H speed-mode

5) CNTL-C Register

MODE	D7 ~ D4	D3 ~ D0	SMDP	SMSD	SMEF	SMON
FORWARD		1000	H	Hi-Z	L	H
REVERSE		1010	L	Hi-Z	L	H
SPEED		1110	SPEED	Hi-Z	L	H
HSPEED	1110	1100	HSPEED	Hi-Z	L	H
PHASE		1111	PHASE	PHASE	Hi-Z	H
XPHSP		0110	SPEED, PHASE	Hi-Z, PHASE	L, Hi-Z	H
VPHSP		0101	SPEED	Hi-Z, PHASE	L, Hi-Z	H
STOP		0000	L	Hi-Z	L	L

3. Tracking Counter

This block used for track jump perform that the data, which must be jumped, inputed from μ-Com is loaded to CNTL-L, U at rising edge. Loaded Data is starting the count by tracking counter clock track, if CNTL-L is selected $\overline{\text{COMPLETE}}$ signal is outputed to $\overline{\text{ISTAT}}$ terminal, and if CNTL-U is selected, $\overline{\text{COUNT}}$ signal is outputed to.
When CNTL-L reg is selected, if the pulse width of bottom hold exceed 64T (T: a period of PBFS) 'L' is outputed to $\overline{\text{ISTAT}}$ terminal. The result is detected after reverse command is inputed from μ-com and is that the speed of spindle motor reduce.
The following is timing chart of tracking counter block.

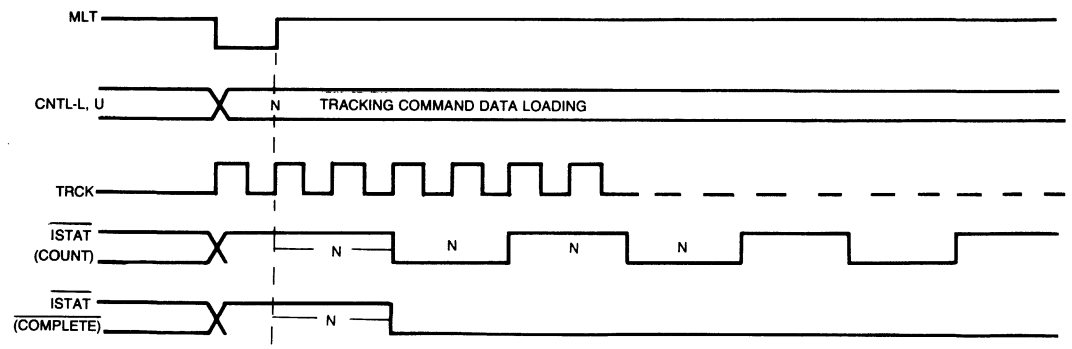


Fig. 4 Tracking Count Timing Chart

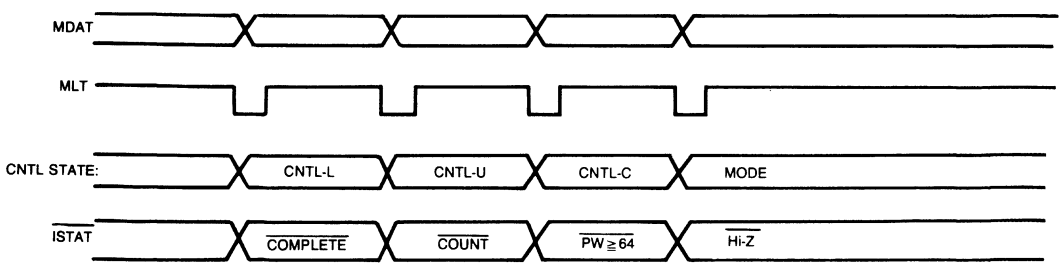


Fig. 5 CNTL Reg. According to Output Signal of $\overline{\text{ISTAT}}$

1) Block Diagram

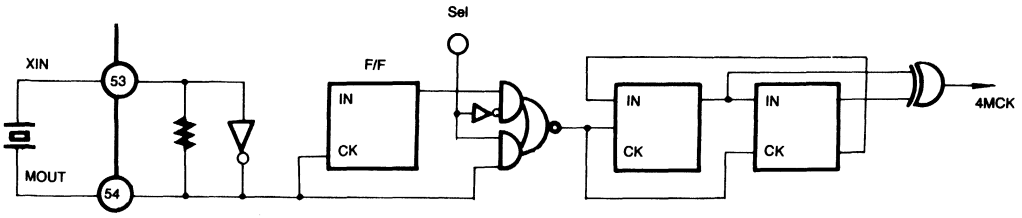
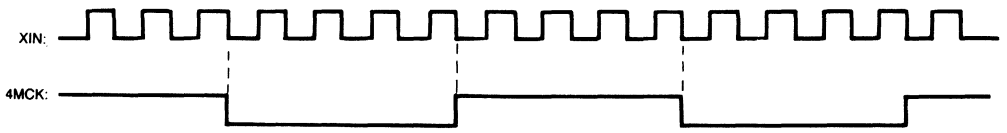
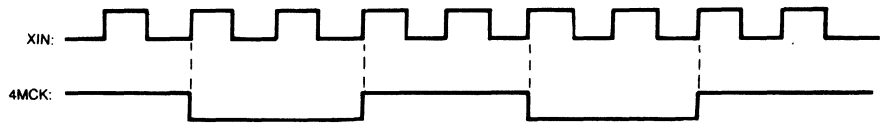


Fig. 6 X'tal OSC Block Diagram

2) Using the X'tal osc of 16.9344 MHz, Timing Chart (Sel = 0)



3) Using the X'tal osc of 8.4672 MHz, Timing Chart (Sel = 1)



5. EFM

EFM consist of EFM demodulator which demodulate EFM DATA inputed from the Disk, EFM phase detector, frame sync detector/protector/inserter, subcode sync detector, and controller which controls EFM block .... etc.

1) EFM Phase Detector

As EFM inputed from disk includes the component of 2.11 MHz, EFM Phase Detector generate the bit clock (PBCK) of 4.32 MHz to detect the phase of this signal.
This PBCK detects the phase at the edge of EFM signal and the result is outputed to phase terminal.

A. At normal operating

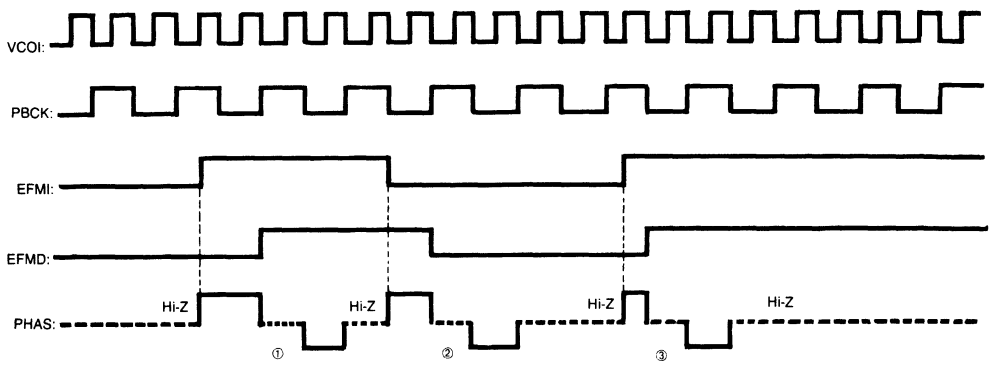


Fig. 7 EFM Phase Detection Timing Chart

In case of ①: when EFM signal is slow than VCO
In case of ②: when EFM signal is locked with VCO
In case of ③: when EFM signal is faster than VCO

B. At abnormal operation
If HIPD of CNTL-2 is selected "L" by μ-com EFM phase detector operates like (Figure 5)
If HIPD is 'H' and 'L' of LKFS is shorter than 3.5T (a period of PBFS is T)
Hi-Z is outputed to PHAS terminal as many as 'L' and be over 3.5T, Hi-Z is outputed as many as 3.5T

2) EFM Demodulator

Modulated 14 Bit DATA is inputed into NRE-I circuit in the DSP.
The 14 bit DATA through the circuit changes demodulated 8 bit DATA as NRE-I circuit convert 14 bit EFM data to 8 bit data. Demodulated DATA have two kind of signal, the one is subcode data and the other is PCM data, and that one is inputed into subcode block and this one is written in the 16K SRAM by CE and WE signal.

3) FRAME SYNC DETECTOR INSERTER/PROTECTOR

a. Frame sync detector

The Data consist of PRAME units, that is, it consist of frame sync, subcode data, PCM data, redundancy data..... etc.
The frame sync is detected by one per frame unit

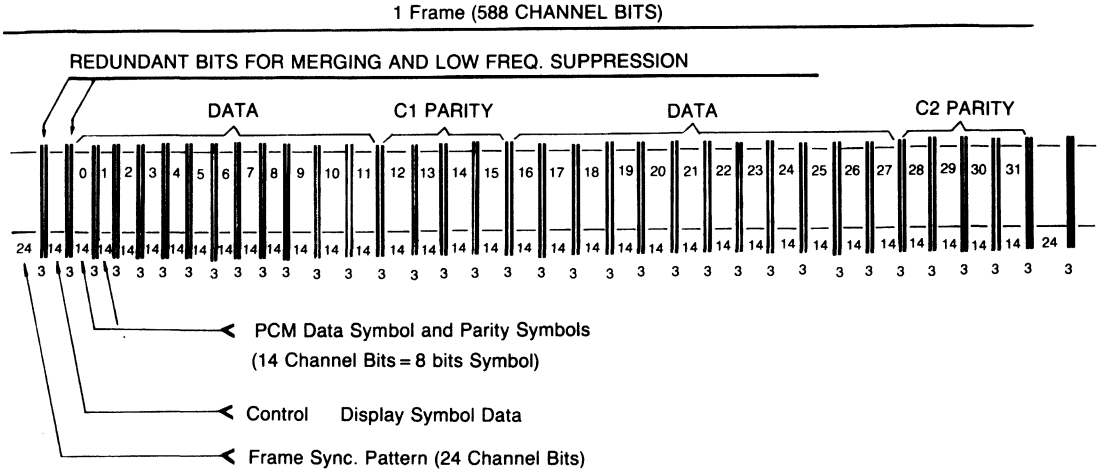


Fig. 8 (Frame Format)

B. Frame sync protector/inserter

Frame sync is omitted or detected in the place where it don't exist by the effect of ERROR or JITTER on the disk.
In these cases, we need to insert or protect the signal.
The window is made by using the WSEL signal to protect the Frame Sync.
The frame sync inputed to window is ture data, and don't inputed is ignored.
A width of window is determined by WSEL of CNTL-S Reg.
If frame sync didn't be detected in the FRAME SYNC PROTECTION WINDOW, frame sync made by EFM Block is inserted in case of the sync is inserted sequencely. When the appointed number of FRAMEs is achieved by FSEM, FSEL of CNTL-S Reg, the ULKFS becomes "L" and FRAM SYNC PROTECTION WINDOW is ignored.
FRAME SYNC is received absolutely at that time. When Frame Sync is received, the ULKFS signal becomes "H" and FRAME sync detected in window is received.

LKFS	ULKFS	Explanations
I	I	Accordance with PLAYBACK FRAME SYNC and generated FRAME SYNC.
O	I	① Out of accordance with PLAYBACK FRAME SYNC and generated FRAME SYNC, but PBFR SYNC is detected in the window selected by WSEL. ② Out of accordance with PBFR SYNC and XTFR SYNC, and SYNC is inserted because it don't be detected in the window selected by WSEL.
O	O	① After insertion as many as the Frame decided by FSFM and FSEL of CNTL-S Reg. as frame sync don't be detected in the window. ② In case that PBFR SYNC don't be detected.

6. Subcode

14 bit Subcode Sync Signal (this is S0, S1) is detected in the Subcode Sync.
After S0 is detected, a frame of S1 is detected.
At that time S0 + S1 signal is outputed to S0S1 terminal, and S0, S1 signal is outputed to SDAT terminal when S0S1 signal is "H".
After 14 bit subcode data becomes EFM demodulation, the 8 BIT of subcode data (P, Q, R, S, T, U, V, W) is syncronized with PBFR signal and is outputed to SDAT by SBCK CLOCK.
Among the eight subcode DATA, Q1 data is selected and loaded to the eighty shift resister by PBFR signal. The result of checking the CRC (cycle redundancy check) of roading data is syncronized with S0S1 rising edge and outputed to SQOK terminal.
If the result of checking is error.
"L" is outputed to SQOK terminal and if it is true "H" is outputed to and if the CRCD of CNTL-Z Mode is "H", the result of CRC CHECK is outputed to SQDT terminal during from S0S1, 'H' to SQCK FALLING EDGE.
The following is the timing chart of subcode block.

1) at SQEN = 'L', SDAT, SQDT, S0S1, SQOK, VCOI Timing Chart

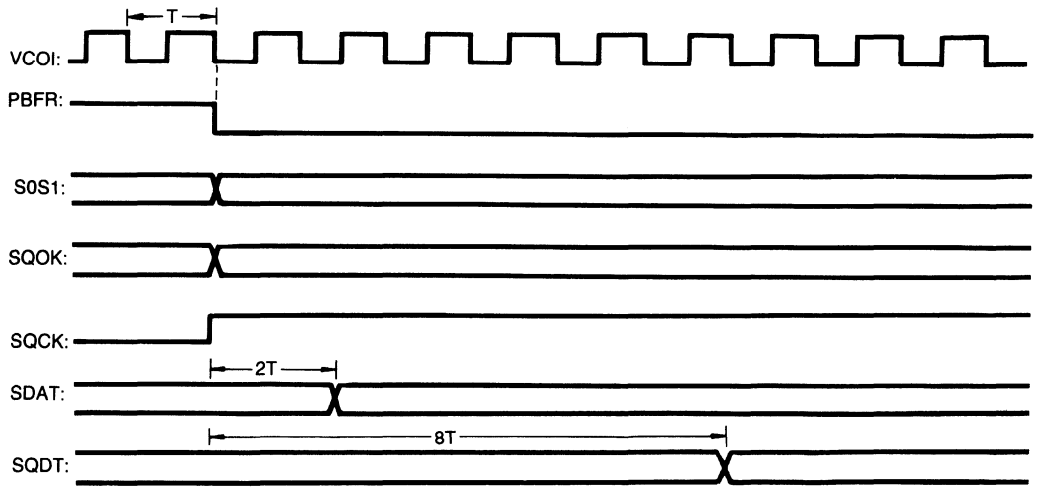


Fig. 9

2) at SQEN = 'L', SQOK, SQDT, S0S1 Timing Chart

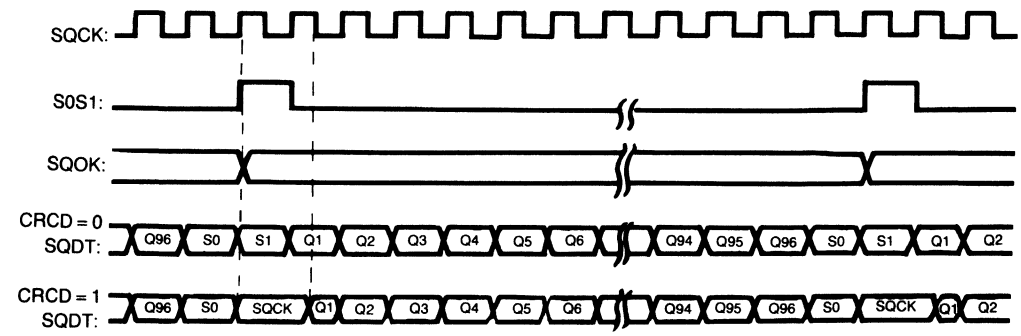


Fig. 10

3) at SQEN = 'H', SQOK, SQDT, S0S1, SQCK Timing Chart

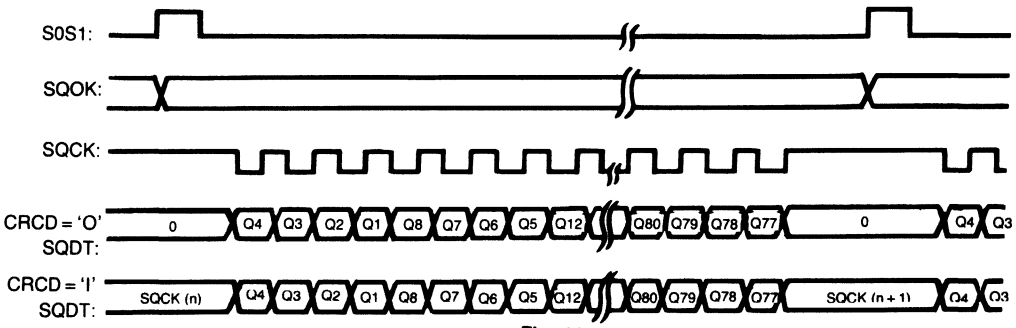


Fig. 11

Comment: If the SQOK of the subcode Q data is "H", subcode data is outputed to SQDT according to subcode, and it is "L" is outputed.

4) VCOI, SDAT, SBCK Timing Chart

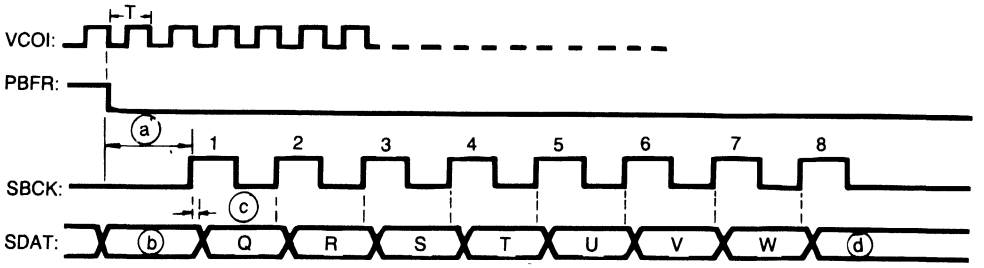


Fig. 12

a) after PBFR becomes falling edge
SBCK become "L" during about 10 sec.
b) If S0S1 is "L", subcode P is outputed and "H", S0, S1 is outputed.
c) If a period of VCOI is "T", the width of ⓒ is 4T ~ 6T.
d) If the pulse inputed to SBCK terminal be over seven, subcode data (P, Q, R, S, T, U, V, W) is repeated.

7. ECC

In case the data on the disk is damaged, ECC block corrects the damaged data.
C1 (32,28) and C2 (28,24) error is corrected by CIRC.
ECC is performed by the unit of one symbol of eight bit.
C1 pointer is generated for C1 correction, and C2 pointer is generated for C2 correction. C1, C2 send the error information of the DATA which ECC is performed.
The data which don't be corrected is showed the error data by outputing C2 FIAG.
The C2FL signal is handled in the interpolator by using the signal of C2F1 and C2F2.

C1F1	C1F2	C1C2 Error Condition	C2F1	C2F2	C2FL
O	O	No error	O	O	O
O	I	Single error correction	O	I	O
I	O	Double error correction	I	O	O
I	I	Irretrievable error	I	I	I

C1F1, C1F2: the error correct condition is outputed by C1 decoder.
C2F1, C2F2: the error correct condition is outputed by C2 decoder.
C2FL : In case that error can't be corrected by C2 decoder becomes 'H' and the reverse case becomes 'L'

8. 16K SRAM

SRAM Adress Generator and 16KSAM is built in DSP to write the data in the RAM, to read/write the data at the ECC processing, and to output the data to D/A converter after the EFM data from the disk is demodulated.
The SRAM (PAD 59) must be 'L' when the 16KSRAM is operating.

1) Address Generation Priority Control

These are processed at the same time that write when EFM is demodulated, R/W at the ECC processing at D/A converter read, the priority must be controlled. When these signals are required simultainiously the processing priority is that the first is D/A converter read, the second is EFM write, the third is ECC R/W.

2) EFM demodulation data write

When write requirement signal is send to SRAM ADDRESS GENERATOR, as the demodulated EFM DATA must be written in the SRAM, the priority is controlled and the enable signal is inputed to EFM block and the generated address is send to SRAM INTERFACE circuit.
The generated adress is a data considering deinterleave thirty-two addresses are generated in the one frame.

A. At the time being used 16K SRAM (EFM & ECC write)
- DB1 ~ DB8 is 'H'
- AD1 ~ AD11 is Hi-Z
- CE, WE don't care

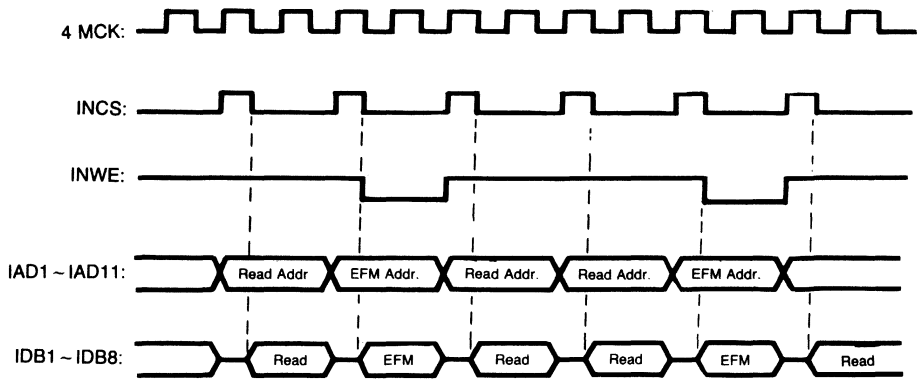
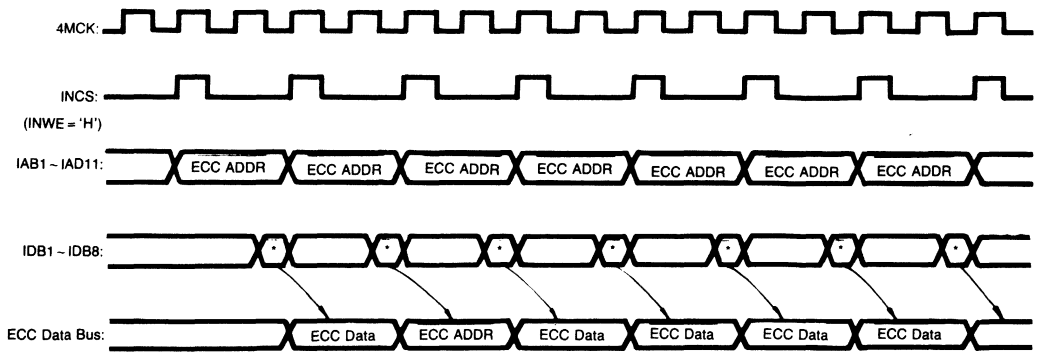


Fig. 13

3) ECC DATA R/W

At C1, C2 ECC processing, one hundred and twinty-nine address signal is generated during one frame processing as sixty-four PCM Datas and sixty-five pointer must be R/W, at ECC processing, write function is equal to 2). The following is at READ.

A. The reading time at 16K SRAM



*: Valid ECC Data

Fig. 14

4) D/A Converter Read

Thirty-six read enable signals are generated during one frame as six sampling data and twelve C2 pointer data must be read in each L, R-CH. The timing chart is equal to R/W block of ECC data for D/A converter read.
In conclusion, one hundred and seventy-nine of R/W processing action are requerd.

5) Address Generator

The Data interleaved at encode is deinterleaved at decode.
One hundred and eight frame data is needed for getting one frame of PCM data in CDP format.
Two counter is used to get data mached to CDP Format. That is, write base counter is used to write the EFM demodulated data in the SRAM, and read base counter is used to read the data in RAM.

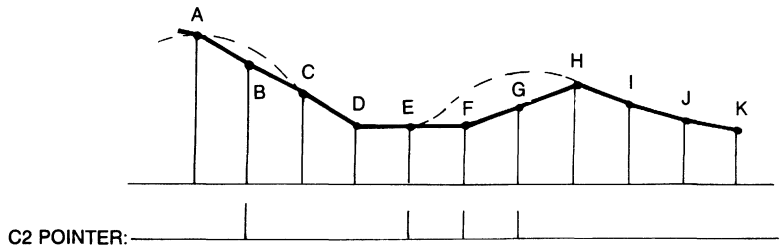
6) JITTER MARGIN

The EFM demodulated DATA is disturbed by rolling of the disk, or instability of servo system when the data is written in the SRAM. The data is distructed by time limit when the value of R/W base counter exceed ±5 FRAME because of SRAM SIZE.
The JITTER MARGIN became less than ±4 frame when the value of R/W base counter exceed ±5 FRAME be due to the value of READ BASE COUNTER is loaded to the value of WRITE BASE COUNTER compulsorily.
The value of READ BASE COUNTER is loaded to the value of WRITE BASE COUNTER compulsarily when the difference of READ/WRITE BASE COUNTER exceed ±4 frame, 'H' signal is outputed to JIT during a period of PBER.

9. Interpolator Mute

1) Interpolator

If the BURST ERROR occur on the disk although ECC process is performed, THE data can't be corrected, according to circumstance. The data is corrected by using C2 pointer of ECC in the interpolator block.
The PCM data is inputed to DATA BUS and the priority is that the first is 8 BIT C2 pointer the second is lower 8 bit, the third is upper 8 bit against each L. R-CH. When DA FLAG is 'H' takes pre hold, and in case that single error occur the average compensation method is performed with the value of PCM DATA, against a period of CHCK, when CHCK is 'L', R-CH DATA is outputed and when CHCK is 'H', L-CH DATA is outputed the timing chart of interpolator block refer to (Figure 16)



$B = \frac{A+C}{2}$: average compensation

F = E = D: Pre hold compensation

$G = \frac{F+H}{2}$: average compensation

Fig. 15

2) Mute, Attenuation

The audio data is muted or reduced by the ATTN signal is muting terminal and CNTL-S Reg.
The mute have two kind of muting, one is ZERO cross muting, the other is muting.

a) Zero cross muting
The audio data is muted, after ZCMT of CNTL-Z reg goes to 'H', and in case that mute is 'H' and the upper 6 bit of audio data became all 'L' or 'H'.

b) Muting
The audio data is muted in case that the ECMT of CNTL-Z Reg. is 'L' and mute terminal is 'H'.

c) Attenuation
The signal reduction is occured by ATTM of CNTL-S reg and mute signal as following.

ATTM	MUTE	
O	O	0dB
O	I	$-\infty$dB
I	O	-12dB
I	I	-12dB

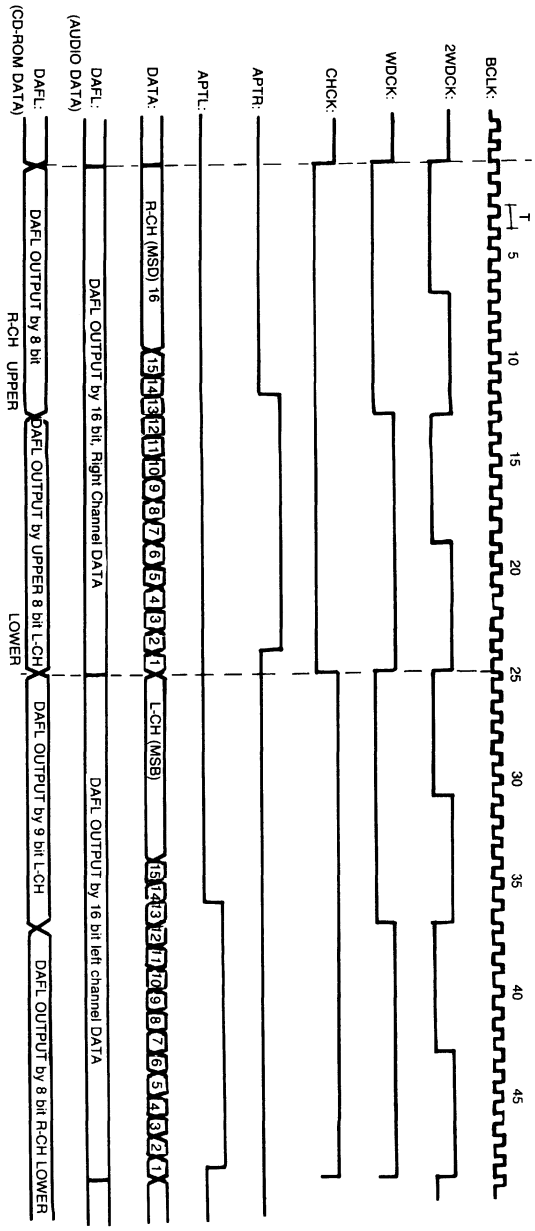


Fig. 16 The timing chart of PCM data output in case that sel 5 is 'L' and DF is off.

10. Digital Filter

The FIR (finite impulse response) digital filter is build in KS9210.
This block consist of register multiplier, S/P & P/S converter, controller.....etc.

1) Block diagram

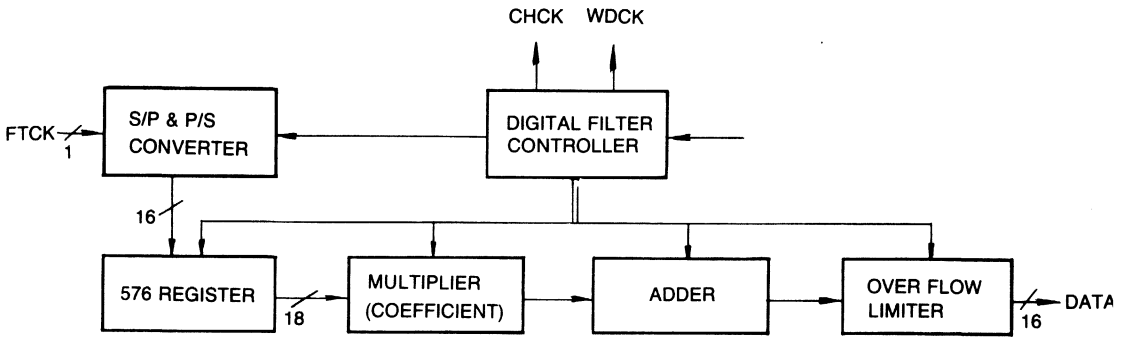
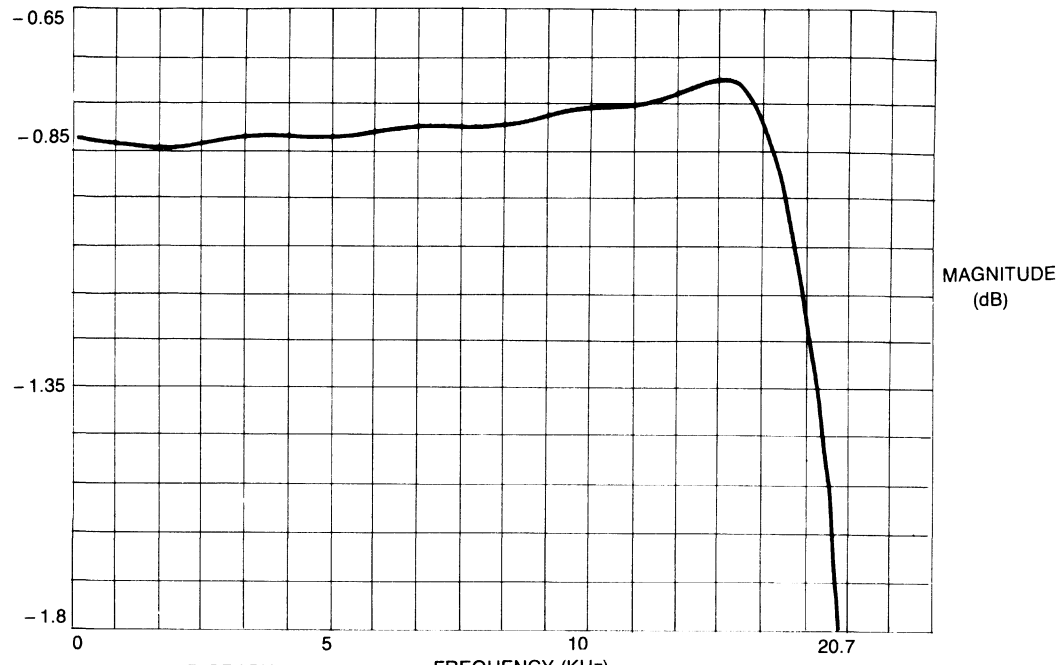


Fig. 17

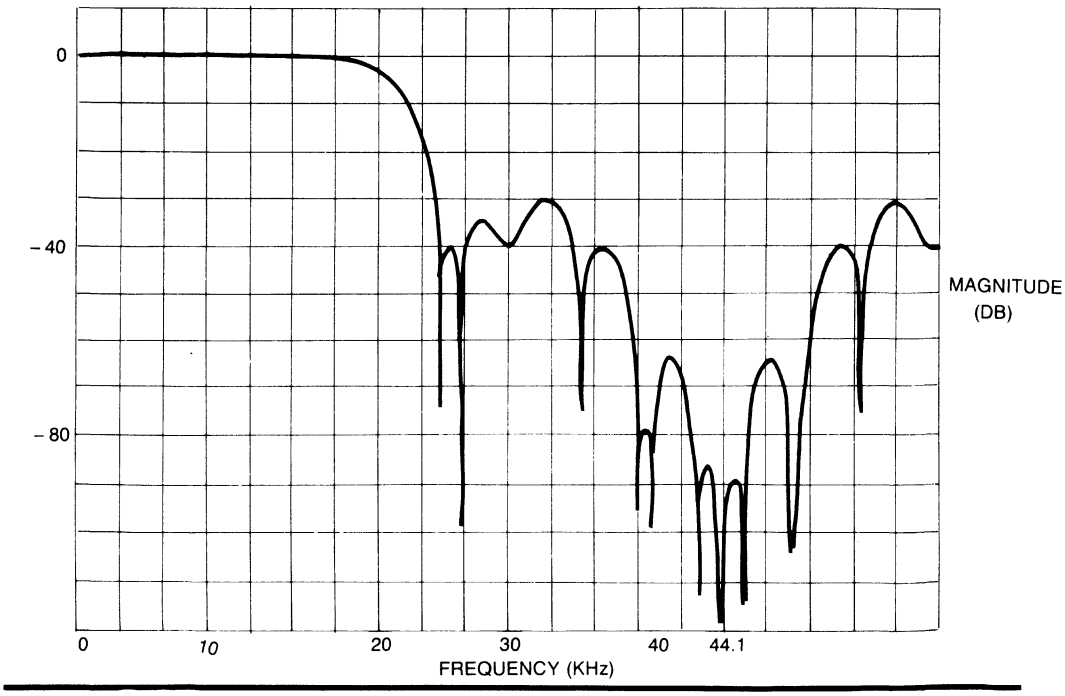
2) Specification

PASS BAND	• Ripple up to 18 KHz band • Reduction of 1 KHz in 20 KHz	±0.07 Max 0.55 Max
FILTER BAND	• Reduction of 1 KHz in 44.1 ± 1 KHz • Reduction of 1 KHz in 44.1 ± 5 KHz • Reduction of 1 KHz in 44.1 ± 10 KHz • Reduction of 1 KHz in 44.1 ± 20 KHz • – 30dB frequency range of 1 KHz • – 60dB frequency range of 1 KHz	91 dB Min 60 dB Min 44 dB Min 24 dB Min 44.1 ± 20 KHz 44.1 ± 6 KHz

A. RIPPLE GRAPH



B. LOW PASS FILTER GRAPH



11. CLV Servo

The CNTL-C Reg. is selected to control the CLV servo by Data inputed μ-Com.
The CLV servo action mode is appointed by the data inputed from μ-com to control spindle motor in CNTL-C Reg.

1) Forward
The terminal condition of output mode is that SMDP is "H", SMSD is "Hi-Z", SMEF is "L", and SMON is "H".

2) Reverse
The condition of reverse mode is that SMOP is 'L', SMSD is 'Hi-Z', SMEF is 'L', and SMOD is 'H'.

3) Speed-Mode
The spindle motor is controlled roughly by the mode when track jumping or EFM phase is unlocked.
If a period of VCO is 'T', the pulse width of frame sync is '22T'.
In case that the signal detected from EFM signal exceed '22T' by noise on the disk, ... etc., it must be removed, if not, the right frame sync can't be detected. In these case, the pulse width of EFM signal is detected by the period of XTFR/2 or XTFR/4 and the pulse width of EFM signal is detected by the period of XTFR/16 or XTFR/32.

* Peak hold clock is XTFR/2 or XTFR/4, and bottom hold clock is XTFR/16 or XTFR/32.

The detected value is used for syncronized frame signal.
If syncronized frame signal is less than 24T, the SMPD terminal outputs 'L', equal to 22T, outputs 'Hi-Z', and more than 23T, outputs 'H'.
If the gain signal of CNTL-W Reg. is 'L' the output of SMPD terminal is reduced up to -12 dB. If it is 'H', there is no reduction. (refer to figure 7)
Output conditions SMSD = Hi-Z, SMEF = 'L', SMON = 'H'

4) Hi-Speed-Mode
The mirror do main of track which havn't pit is duplicated with 20KHz signal to EFM.
In this case, servo action be to unstable because the peak value of mirror signal which is longer than original frame sync signal is detected. In Hi-speed mode, by using the 8.4672/256 MHz signal against peak hold and XTFR/16 or XTFR/32 signal against bottom hold, the mirror is removed, and hi-speed servo action be to stable. Output is that SMSD is 'Hi-Z', SMEF is 'L' SMON is 'H'.

5) Phase-Mode
The mode for controls EFM phase. Phase difference between PBFR/r and XTFR/4 is detected when NCLV of CNTL-Z is 'L' and phase difference between Read Base Counter/4 and Write Base Counter/4 is detected when NCLV is 'H', and the difference is outputed to SMPD.
(refer to figure 8)
'H' is outputed from falling edge of PBFR during (WPO-278T) x 32 to SMSD terminal and 'L' is outputed up to falling edge of next PBFR.
(refer to figure 9)

6) XPHSD-Mode
The mode for using normal action.
The LKFS signal made from frame sync block is to sampling which period is PBFR. If sampling is 'H', Phase Mode is performed, and if the sampling is eight of 'L' continuously, speed mode is performed automatically. Selecting Peak hold period of speed mode, and bottom hold period and gain of speed/hi-speed mode is determined by CNTL-W Reg.

7) VPMSP-Mode
The mode to controls rough servo. Instead of X'tal VCO is used to test EFM pattern.
If the center value of VCO is varid the rotation of spindle motor is varied to same direction and VCO is locked easily.

8) STOP
The mode for stop spindle motor. Output is that SMDP is 'L', SMSD = 'Hi-Z' SMEF is 'L', and SMON is 'L'.

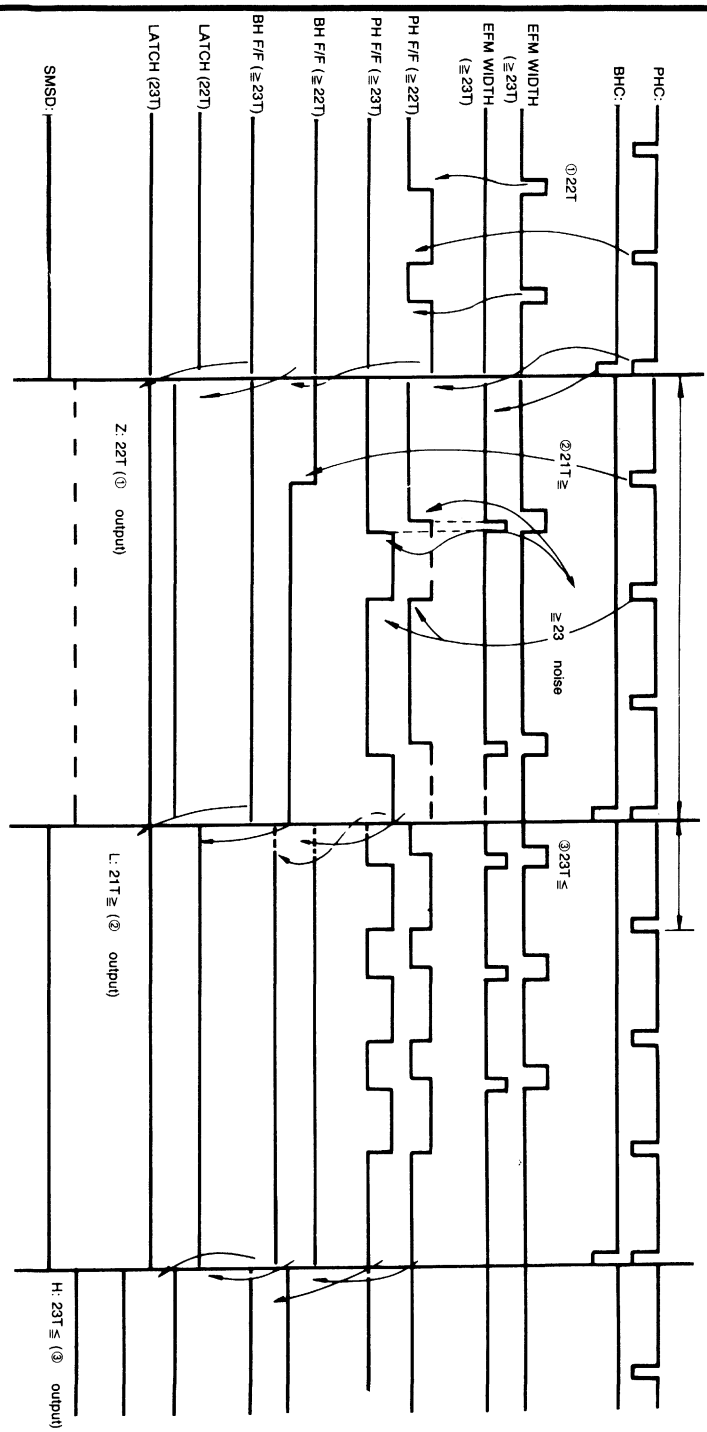


Fig. 18 The timing chart of SMSD output when gain is 'H'

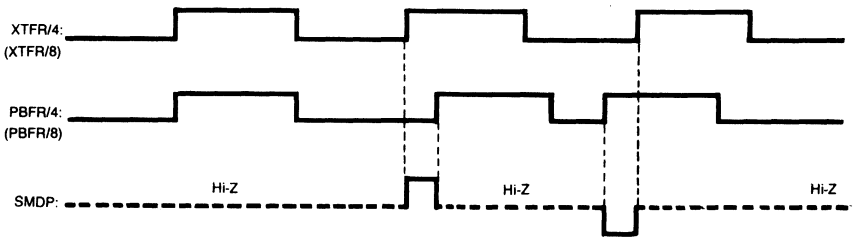
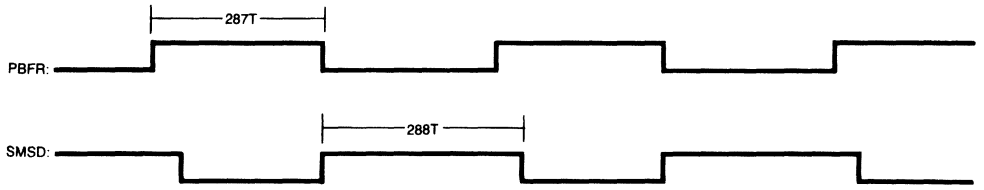
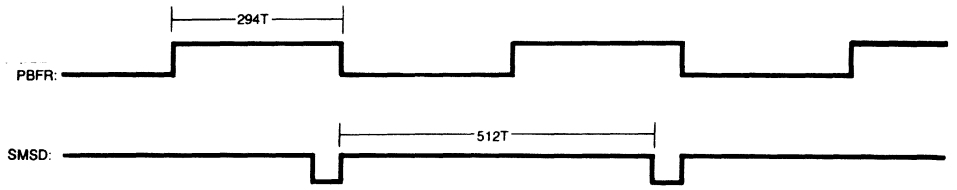


Fig. 19 The timing chart of SMDP output



(a) The timing chart of SMSD output when PBFR is '287T'



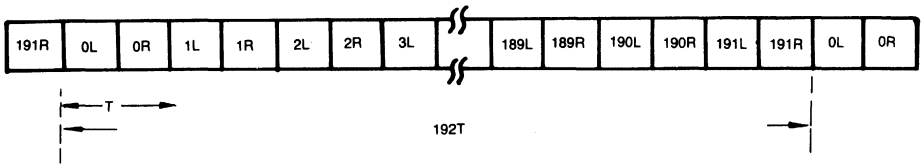
(b) The timing chart of SMDP output when PBFR is '294T'

Fig. 20 The timing chart of SMDP output at phase mode

12. Digital Audio Out

The data is outputed serially by audio interface format to other digital set.

1) Digital Audio Interface Format for CDP



0L: L-CH Format included block sync preamble
1L-191L: L-CH Format included L-CH sync preamble
0R~191R: R-CH format included R-CH sync preamble

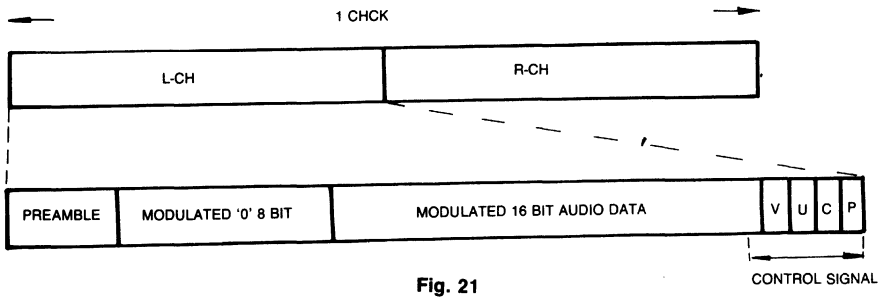


Fig. 21

a) PREAMBLE

Use for discrimate the block of data, L and R-CH DATA

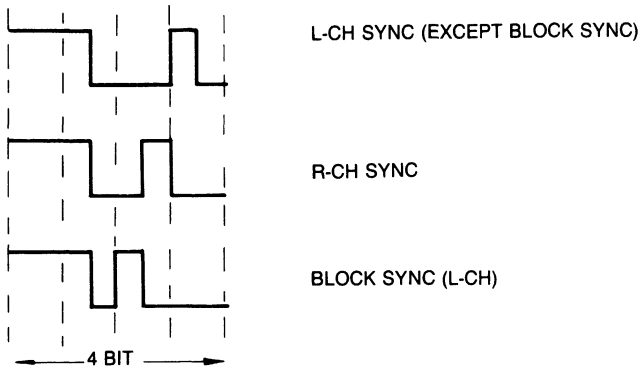


Fig. 22

b) Control Signal

① Validity bit: it is indicated that the error of 16 bit audio data exists, or don't
② User definable bit: subcode data output

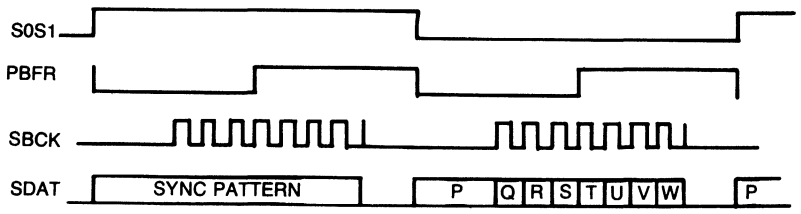
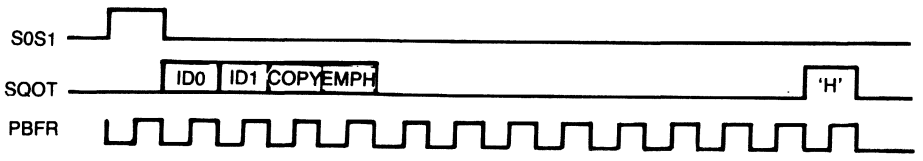


Fig. 23

③ Channel status bit:
Output a high position information of 4 bit of subcode Q indicate the number of channel, pre-emphasis and copy.... etc.
Indicate CDP-category.

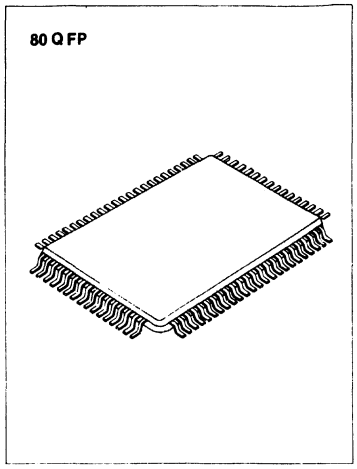


④ Parity Bit: Make even parity.

Fig. 24

DIGITAL SIGNAL PROCESSOR

The KS9211 is a CMOS integrated circuit designed for compact disc player applications. It consists of 16KSRAM, digital filter, and digital signal processing circuits.



FEATURES

- **All digital signals for regeneration are processed using one chip.**
- **Internal aperture compensation digital filter**
- **EFM-PLL circuit for bit clock regeneration**
- **EFM data demodulation**
- **Frame synchronous signal detection, protection**
- **Compensation using mean value and prior value retention**
- **Subcode signal demodulation subcode Q detection**
- **CLV servo for spindle motor**
- **8-bit tracking counter**
- **CPU interface with serial bus**
- **Subcode Q register**
- **Built-in 17th digital filter**
- **Built-in 16KSRAM**
- **80 Quad flat package type**
- **Operating supply voltage: V_{DD} = 3.4 ~ 5.5V**

ORDERING INFORMATION

Device	Package	Operating Temperature
KS9211	80 QFP	−20°C ~ +75°C

BLOCK DIAGRAM

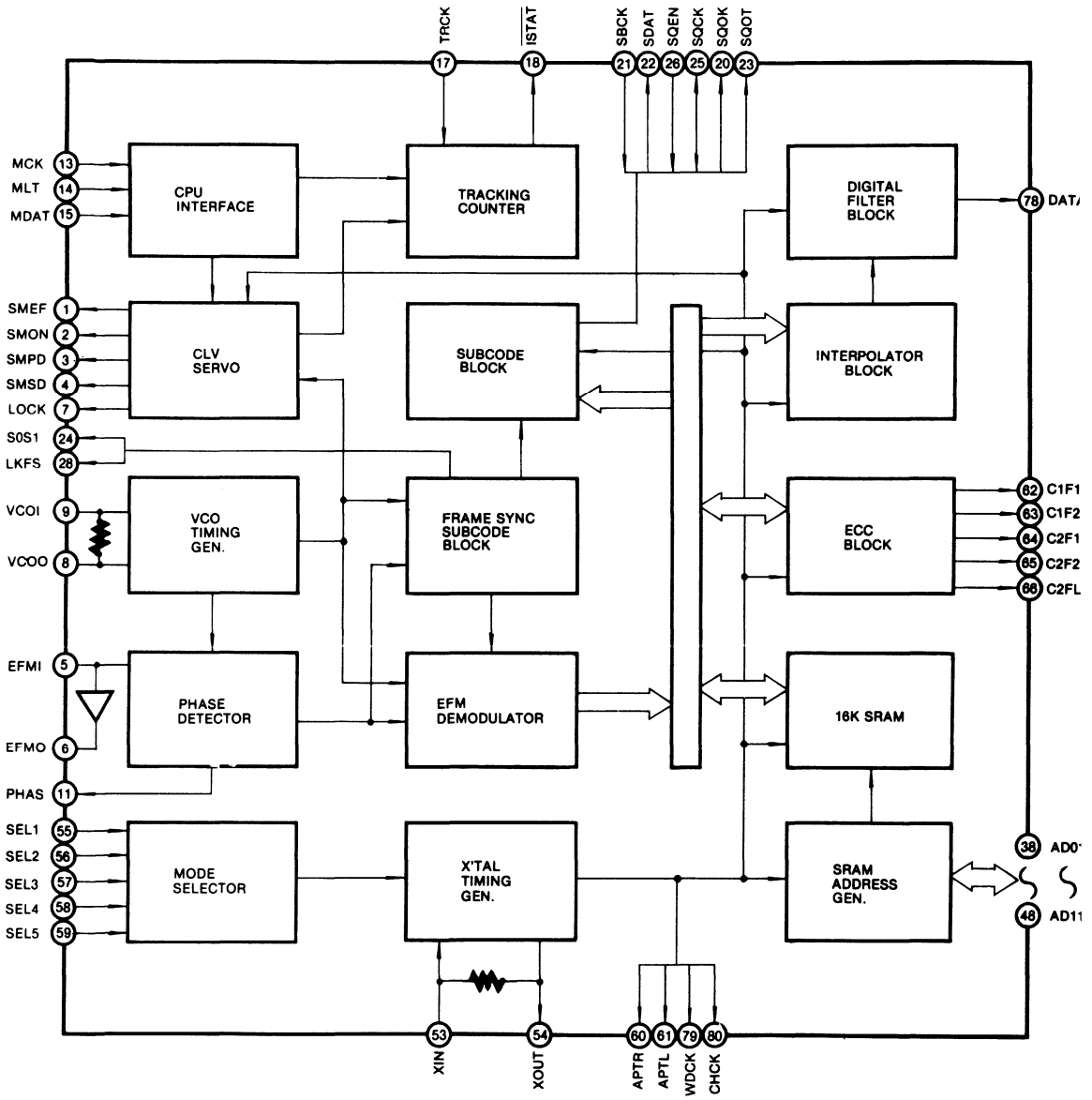


Fig. 1

PIN CONFIGURATION

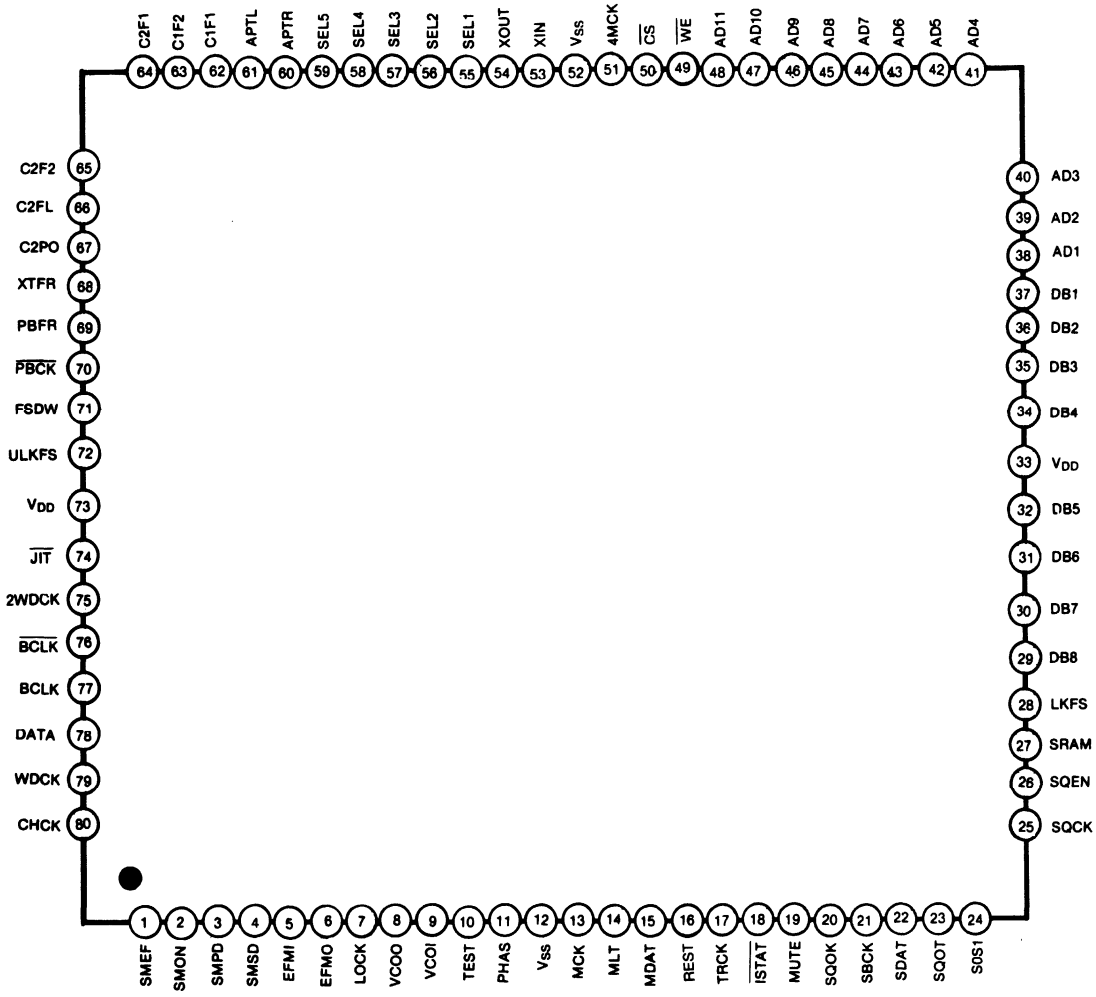


Fig. 2

PIN DESCRIPTION

Pin No	Symbol	I/O	Description
1	SMEF	O	Pin 1 output is switched constant when output filter of the spindle motor is energized.
2	SMON	O	ON/OFF control for spindle motor.
3	SMPD	O	Spindle motor drive. Provides rough control during CLV-S mode and phase control during CLV-P mode.
4	SMSD	O	Spindle motor drive. Controls speed during CLV-P mode.
5	EFMZ	I	EFM signal from RF amplifier.
6	EFMO	O	Controls slice level of the EFM signal.
7	LOCK	O	The output of pin 7 reflects the status of the GFS signal which is sampled at PBFR/16. When the GFS signals is "H", but, when the signal has remained "L" for at least 8 samples, the output of pin 7 is "L".
8	VCOO	O	VCO output. The frequency is f = 8.6436MHz, when locked by the DBFR signal.
9	VCOI	I	VCO input.
10	TEST	I	(0V).
11	PHAS	O	The output of Pin 11 provides phase comparison of EFM signal and VCO/2.
12	V_{SS}	—	GND (0V).
13	MCK	I	Pin 13 provides serial transmission clock from the CPU. Data is latched on the leading edge of the clock.
14	MLT	I	Pin 14 provides latch input from the CPU. 8-bit shift register data (serial data received from the CPU) is latched in each of the registers.
15	MDAT	I	Serial data from the CPU.
16	REST	I	System reset ("L").
17	TRCK	I	Tracking pulse input.
18	ISTAT	O	Output reflecting internal condition as designated by address.
19	MUTE	I	Muting input. MUTE is "L" when ATTM of internal register A is "L" (normal condition). MUTE is "H" when meting condition is set.
20	SQOK	O	Output the results CRC check of subcode Q.
21	SBCK	I	Clock input for subcode serial output.
22	SDAT	O	Serial output of subcode.
23	SQDT	O	Output of subcode Q.
24	S0S1	O	Output of subcode sync S0 + S1.
25	SQCK	I/O	Clock for reading subcode Q.
26	SQEN	I	Input for selecting SQCK (L; SQCK is output, H; SQCK is input)
27	SRAM	I	SRAM is "H" in Nomal, SRAM is "L" when system is testing.
28	LKFS	O	Display output for frame sync lock status.

PIN DESCRIPTION (Continued)

Pin No	Symbol	I/O	Description
29	DB8	I/O	Data pin for external RAM. DATA8 (MSB) in test mode. Hi-Z in normal
30	DB7	I/O	Data pin for external RAM. DATA7 in test mode. Hi-Z in normal
31	DB6	I/O	Data pin for external RAM. DATA6 in test mode. Hi-Z in normal
32	DB5	I/O	Data pin for external RAM. DATA5 in test mode. Hi-Z in normal
33	V_{DD}	—	Power supply (+5V).
34	DB4	I/O	Data pin for external RAM. DATA4 in test mode. Hi-Z in normal
35	DB3	I/O	Data pin for external RAM. DATA3 in test mode. Hi-Z in normal
36	DB2	I/O	Data pin for external RAM. DATA2 in test mode. Hi-Z in normal
37	DB1	I/O	Data pin for external RAM. DATA1 (LSB) in test mode. Hi-Z in normal
38	AD01	O	(LSB)
39	AD02	O	In normal mode (TEST = 'L', SRAM = 'H'), these pins are High impedance (Hi-Z) In test mode (TEST = 'H', SRAM = 'L'), these pins are Output address of external RAM
40	AD03	O	
41	AD04	O	
42	AD05	O	
43	AD06	O	
44	AD07	O	
45	AD08	O	
46	AD09	O	
47	AD10	O	
48	AD11	O	(MSB)
49	$\overline{WE}$	I/O	In normal mode, this is WE output. In test mode, write enable input.
50	$\overline{CE}$	I/O	In normal mode, this is CE output. In test mode, chip enable input.
51	4MCK	O	Divider output for crystal. f = 4.2336MHz
52	V_{SS}	—	GND (0V)
53	XIN	I	Input to crystal oscillator circuit. Depending on the mode, the frequency is either f = 8.4672 r 16.9344MHz.
54	XOUT	O	Output from crystal oscillator circuit. Depending on the mode, the frequency is either f = 8.4672 or 16.9344MHz.
55	SEL1	I	Mode selection input 1.
56	SEL2	I	Mode selection input 2.
57	SEL3	I	Mode selection input 3.
58	SEL4	I	Mode selection input 4. Code switch input for audio data output. 2's complement output when "L", and offset binary output when "H"
59	SEL5	I	Mode selection input 5. Code switch input for audio data output. Serial output when "L", parallel output when "H".

PIN DESCRIPTION (Continued)

Pin No	Symbol	I/O	Description
60	APTR	O	Output for aperture compensation. "H" when R-ch.
61	APTL	O	Output for aperture compensation. "H" when L-ch.
62	C1F1	O	Monitor output reporting status of error correction for C1 decoder. When SEL5 = 'L', DA01 (LSB of parallel audio data) is output when SEL5 = 'H'.
63	C1F2	O	Monitor output reporting status of error correction for C1 decoder when SEL5 = 'L', DA02 is output when SEL5 = 'H'.
64	C2F1	O	Monitor output reporting status of error correction for C2 decoder when SEL5 = 'L', DA03 is output when SEL5 = 'H'.
65	C2F2	O	Monitor output reporting status of error correction for C2 decoder when SEL5 = 'L', DA04 is output when SEL5 = 'H'.
66	C2FL	O	Output of status condition when SEL5 = 'L'. C2FL is set 'H' when the C2 sequence, being corrected becomes impossible to correct. DA05 is output when SEL5 = 'H'.
67	C2PO	O	Display output of the C2 pointer when SEL5 = 'L'. DA06 is output when SEL5 = 'H'.
68	XTFR	O	When SEL5 = 'L', output of read frame dock, which is 7.35KHz of the crystal system. DA07 is output when SEL5 = 'H'.
69	PBFR	O	When SEL5 = 'I', output of write frame clock, which is 7.35KHz when locked by the crystal system. DA08 is output when SEL5 = 'H'.
70	$\overline{\text{PBCK}}$	O	When SEL5 = 'L', output of VCO/2 (f = 4.3218MHz when locked by the EFM signal). DA09 is output when SEL5 = 'H'.
71	FSDW	O	When SEL5 = 'L', output for unprotected frame sync patterns. DA10 is output when SEL5 = 'H'.
72	ULKFS	O	Output for display of status of frame sync protection when SEL5 = 'L', DA11 is ouput when SEL5 = 'H'.
73	V_{DD}	—	Power supply (+5V).
74	$\overline{\text{JIT}}$	O	When SEL5 = 'L', output for display of either RAM overflow or underflow for +4 frame jitter absorption. DA12 is output when SEL5 = 'H'.
75	ZWDCK	O	When SEL5 = 'L', output for strobe signal (352.8KHz when DF is ON, 176.4KHz when DF is OFF). DA13 is output when SEL5 = 'H'.
76	$\overline{\text{BLCK}}$	O	When SEL5 = 'L', inverse output of BLCK. DA14 is output when SEL5 = 'H'.
77	BLCK	O	When SEL5 = 'L', bit clock output (4.2336MHz when DF is ON, 2.1168MHz when DF is OFF) DA15 is output when SEL5 = 'H'.
78	DATA	O	Serial data output of audio signal when SEL5 = 'L'. DA16 is output when SEL5 = 'H'.
79	WDCK	O	Strobe signal output. Output is 176.4KHz when DF is on. Output is 88.2KHz when DF is off.
80	CHCK	O	Strobe signal output. Output is 88.2KHz when DF is on. Output is 44.1KHz when DF is off.

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{DD}	−0.3 ~ +7	V
Input Voltage	V_I	−0.3 ~ +7	V
Output Voltage	V_O	−0.3 ~ +7	V
Operating Temperature	T_{OPR}	−20 ~ +75	°C
Storage Temperature	T_{STG}	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(V_{DD} = 5V ± 10%, V_{SS} = 0V, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Input High Voltage	V_{IH1}	Note 1	0.7 V_{DD}		V_{DD}	V
Input Low Voltage	V_{IL1}	Note 1			0.3 V_{DD}	V
Input High Voltage	V_{IH2}	Note 2	0.8 V_{DD}			V
Input Low Voltage	V_{IL2}	Note 2			0.2 V_{DD}	V
Output High Voltage	V_{OH}	I_{OH} = −1mA	V_{DD} − 0.5		V_{DD}	V
Output Low Voltage	V_{OL}	I_{OL} = 1mA	0		0.4	V
Input Leakage Current	I_{LKG}	V_{IN} = 0 ~ 5.5V	−5		+5	μA
Three-State Pin Output Leakage Current	I_{LKG}	V_{OUT} = 0 ~ 5.5V	−5		+5	μA
SRAM Input Leakage Current	I_{LKG}	V_{IN} = 0 ~ 5.5V	−5		+200	μA

Note 1. Related pins—EFMI, RESET, TEST, MUTE, SEL 2 ~ 5, MLT, MDAT, SQEN, SQCK.
Note 2. Related pins—TRCK, MCK, SRAM.

2. AC Characteristics

A. XIN Pin, VCOI Pin

(1) When pulse applied to XIN and VCO, V_{DD} = 5V ± 10%, V_{SS} = 0V, and Ta = 25°C, unless otherwise specified.

Characteristic	Symbol	Min	Typ	Max	Unit
"H" Level Pulse Width	t_{WHX}	20			ns
"L" Level Pulse Width	t_{WLX}	20			ns
Pulse Frequency	t_{CK}	55			ns
Input "H" Level	V_{IH}	V_{DD} − 1.0			V
Input "L" Level	V_{IL}			0.8	V
Rising Time Breaking Time	t_R			15	ns

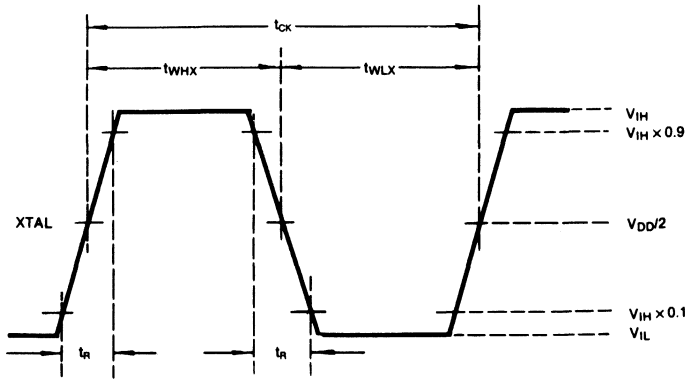


Fig. 3

B. Pins MCK, DATA, MLT, TRCK, SQCK

($V_{DD} = 5.0V \pm 10\%$, $V_{SS} = 0V$, $T_{OPR} = -20 \sim +75°C$)

Characteristic	Symbol	Min	Typ	Max	Unit
Clock Frequency	f_{CK}			1	MHz
Clock Pulse Width	t_{WCK}	300			ns
Setup Time	t_{SU}	300			ns
Hold Time	t_H	300			ns
Delay Time	t_D	300			ns
Latch Pulse Width	t_W	300			ns
CNIN SQCK Frequency	f_{CK2}			1	MHz
CNIN SQCK Pulse Width	t_{WCK2}	300			ns

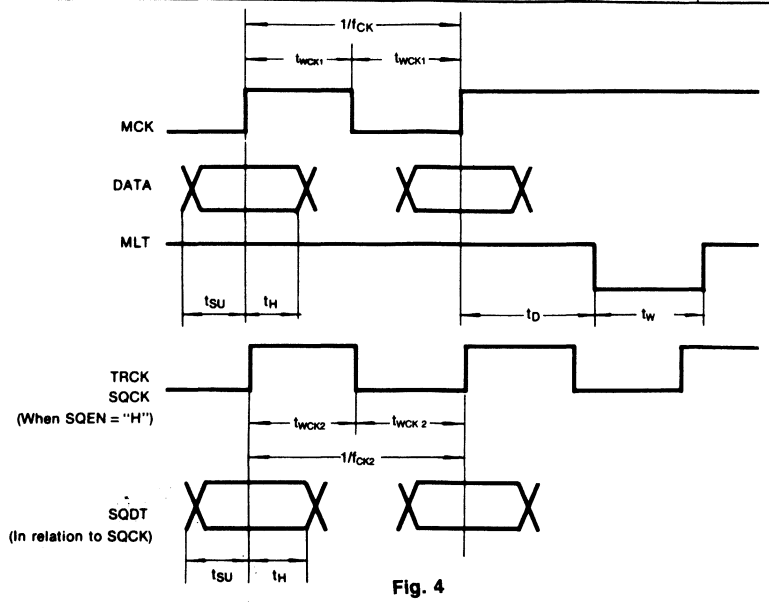


Fig. 4

C. DAC Interface (V_{DD} = 5V ± 10%, V_{SS} = 0V, T_{OPR} = −20 ~ +75°C, C_L = 50pF)

Item	Symbol	DF is OFF			When DF ON			Unit
		Min	Typ	Max	Min	Typ	Max	
Clock Pulse Width	t_{WCK}		236			118		ns
Clock Skew (Fast)	t_{FCK}			40			40	ns
Data Skew (Fast)	$t_{F(SK)}$			0			0	ns
Data Skew (Delay)	$t_{D(SK)}$			80			80	ns

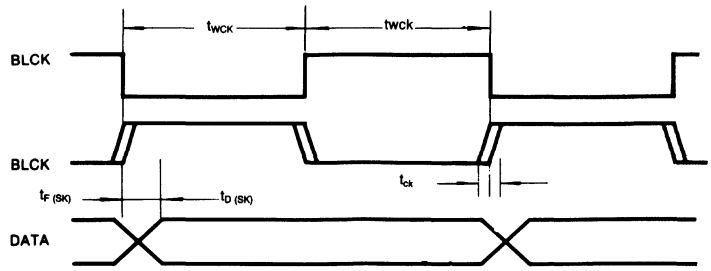


Fig. 5

*Note: CHCK, WDCK, APTR, APTL
DA01 through DA16 during parallel DA conversion or C1F1, C1F2, C2F1, C2F2, C2FL, C2PO, XTFR, 2WDCK, DATA during serial conversion.

APPLICATION INFORMATION
FUNCTION DESCRIPTION

MODE SELECTOR

To control several blocks in KS5991, there are 5 selecting pin signals. Table 1. shows selected mode by these signals.

Input Pins					Function*				
SEL1	SEL2	SEL3	SEL4	SEL5	XIN	DF	P/S	OB/2'S	CD ROM/Audio
0	1	0	0	0	16M	ON	S	2'S	Audio
0	1	0	1	1	16M	ON	P	OB	Audio
0	1	1	0	0	16M	OFF	S	2'S	Audio
0	1	1	1	1	16M	OFF	P	OB	Audio
1	0	0	0	0	8M	ON	S	2'S	Audio
1	0	0	1	1	8M	ON	P	OB	Audio
1	0	1	0	0	8M	OFF	S	2'S	Audio
1	0	1	1	1	8M	OFF	P	OB	Audio
1	1	1	1	0	8M	OFF	S	2'S	CD ROM

Table 1. Mode Selection

* Note: • 8M/16M: Selection of either the XIN or XOUT clocks will provide either a 8.4672MHz or 16.9344MHz signals.
  - DF: Digital Filter
  - P/S: Parallel mode/serial mode
  - OB/2'S: Offset

- Clock selection
  Selectioin of an 16.9344MHz or 8.4672MHz oscillator clock is possible at pins XIN and XOUT. However only 16.9344MHz clocks are provided for digital out usage.

- Digital filter selection
  When the digital filter function is switched to ON, all signals on the DAC interface are handled at twice the normal speed.

- Parallel/Serial output selection
  When the output is parallel, 16-bit parallel data is output from pins DA01 through DA16.
  When the output is serial, the following signals are output at pin DA01 through DA16.

DATA (DA16)	Serial data output (MSB or LSB first output)
BLCK (DA15)	Internal system clock (with DF ON 4.2336MHz and with DF OFF 2.1168MHz)
$\overline{\text{BLCK}}$ (DA14)	Bit clock (BLCK inversion signal)
2WDCK (DA13)	4X multiplied CHLK signal
$\overline{\text{JIT}}$ (DA12)	Jitter Margin Overflow/Underflow signal
ULKFS (DA11)	Display output of frame sync protection status
FSDW (DA10)	Unguarded (unprotected) frame sync signal
PBCK (DA09)	Signal at 1/2 V_{CO} pin cycle times. When locked 4.3218MHz
PBFR (DA08)	Write Frame Clock signal. When locked 7.35KHz.
XTFR (DA07)	Read Frame Clock signal. Crystal system 7.35KHz.
C2PO (DA06)	C2 Pointer signal
C2FL (DA05)	Correction mode output, C2FL = C2F1, C2F2
C2F2 (DA04) C2F1 (DA03)	Monitor Output of Error Correction Mode for C2 Decode
C1F2 (DA02) C1F1 (DA01)	Monitor Output of Error Correction Mode for C1 Decode

- OFFSET Binary/2's Complement Selection
  When pin SEL4 is at "H" output occurs at OFFSET BINARY; when it is at "L" output occurs at 2's complement.
- CD-ROM/AUDIO Selection
  When SEL1 = SEL2 = SEL3 = "H",CD-ROM is selected. Then the C2 pointer is output with each byte (8 bits) and neither the mean value interpolation nor the preceding value hold are exercised. That is, if an error occurs in the upper 8 bits of a 16-bit data, only the C2 pointer related to those upper 8 bits switches to "H" while the lower 8 bits are handled as correct data.

Microcomputer Interface

Data from the microcomputer are inputed through MDAT pins by MCK which is the clock signal of the microcomputer and the pulse signal through MLT pin is for inputed data load one of 6 kinds of control registers.

Fig. 6 Shows the timing diagram of data input from microcomputer.

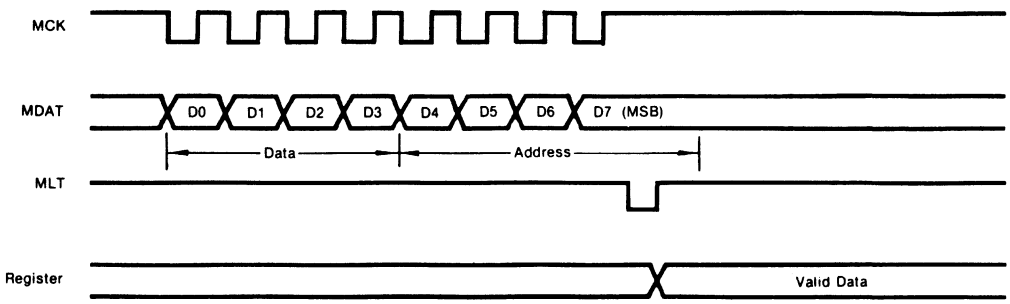


Fig. 6 Data Input Timing Diagram

According to the address of MDAT, control register is selected as below table 2.

Control Register	Comment	Address D7 ~ D4	Data				$\overline{ISTAT}$ Pin
			D3	D2	D1	D0	
CNTL-Z	Data Control	1 0 0 1	ZCMT	HIPD	NCLV	CRCD	Hi-Z
CNTL-S	Frame Sync Protection Attenuation Control	1 0 1 0	FSEM	FSEL	WSEL	ATTM	Hi-Z
CNTL-L	Tracking Counter Lower 4 Bit	1 0 1 1	TRC3	TRC2	TRC1	TRC0	$\overline{Complete}$
CNTL-U	Tracking Counter Upper 4 Bit	1 1 0 0	TRC7	TRC6	TRC5	TRC4	$\overline{COUNT}$
CNTL-W	CLV Control	1 1 0 1	COM	WB	WP	GAIN	Hi-Z
CNTL-C	CLV Mode	1 1 1 0	CLV Mode				$\overline{PW \geq 64}$

Table 2. Data of Selected Control Register

According to D0 through D1 DAA,
The function of each control register is described below.

1) CNTL-Z Register

This is a control register for the zero cross mute of audio data, PHAS, the control signal of phase servo and CRCF data.

		Data = 0	Data = 1
ZCMT	D3	Zero cross mute "OFF"	Zero cross mute "ON"
HIPD	D2	Phase normally active	Phase convert "L" to "Hi-Z" by LKFS
NCLV	D1	Phase servo driven by frame sync	Phase servo is controlled by base counter
CRCQ	D0	SQDT output without SQOK	SQDT = CRCF during the rising time of S0S1

2) CNTL-S Control Register

This is a control register for the frame sync. Protection and attenuation.

FSEM	FSEL	Frame
0	0	2
0	1	4
1	0	8
1	1	13

WSEL	Clock
0	±3
1	±7

ATTM	MUTE	dB
0	0	0
0	1	–
1	0	–12
1	1	–12

3) CNTL-L, U Control Register

When the numbers of tract to be counted are inputed from a microcomputer, data load these registers.
(See tracking counter)

4) CNTL-W Control Register

This is a control register for CLV-Servo.

		Data = 0	Data = 1	Comments
COM	D3	XTFR/4 & PBFR/4	XTFR/4 & PBFR/4	Phase comparative frequency during PHASE-mode
WB	D2	XTFR/32	XTFR/16	Bottom hold period during SPEED and HSPEED-mode
WP	D1	XTFR/4	XTFR/2	Peak hold period during SPEED-mode
GAIN	D0	– 12dB	0dB	SMPD gain during SPEED & HSPEED-mode

5) CNTL-C Control Register

This is a control register for CLV-Servo.

Mode	D7 ~ D4	D3 ~ D0	SMDP	SMSD	SMEF	SMON
Forward	1 1 1 0	1 0 0 0	H	Hi-Z	L	H
Reverse		1 0 1 0	L	Hi-Z	L	H
SPEED		1 1 1 0	SPEED mode	Hi-Z	L	H
HSPEED		1 1 0 0	HSPEED mode	Hi-Z	L	H
PHASE		1 1 1 1	PHASE mode	PHASE mode	Hi-Z	H
XPHSP		0 1 1 0	SPEED, PHASE mode	Hi-Z or PHASE mode	L or Hi-Z	H
VPHSP		0 1 0 1	SPEED PHASE mode	Hi-Z or PHASE mode	L or Hi-Z	H
STOP		0 0 0 0	L	Hi-Z	L	L

TRACKING COUNTER

This counter is used to improve track-jumping characteristics. The number of tracks that are to be jumped are loaded into either register CNTL-L or CNTL-U. After either register CNTL-L or CNTL-U have been loaded and at the rising edge of the next MLT, TRCK pulse count begins. If register CNTL-L = register = CNTL-U = 0, then n = 256n is loaded into the register, and when the address is set in CNTL-L, the signal ($\overline{\text{COMPLETE}}$) is output from pin SENS at high level until the "n"th pulse and then at low level for succeeding pulses. When the address is set in CNTL-U, the signal ($\overline{\text{COUNT}}$) TRCK/2n is output. Fig. 7 shows the timing of the tracking counter.

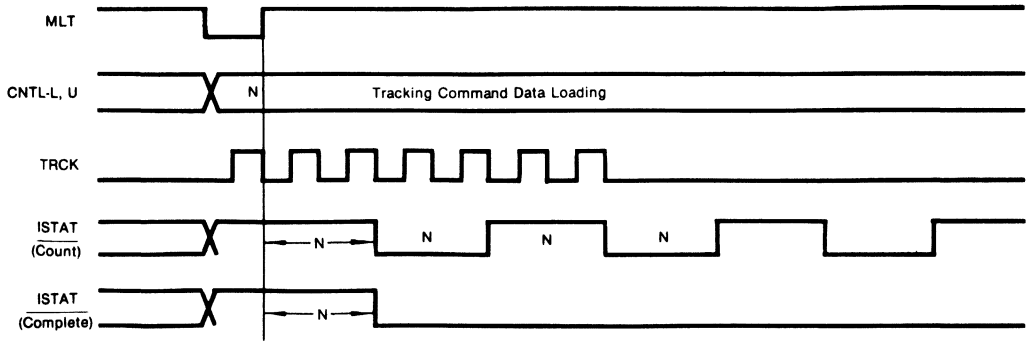


Fig. 7 Tracking Count Timing Chart

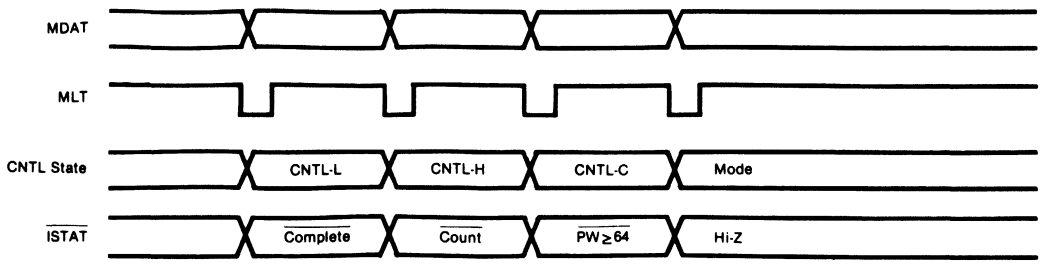
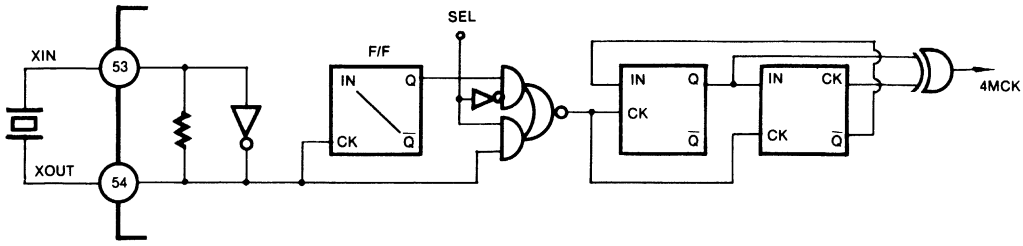


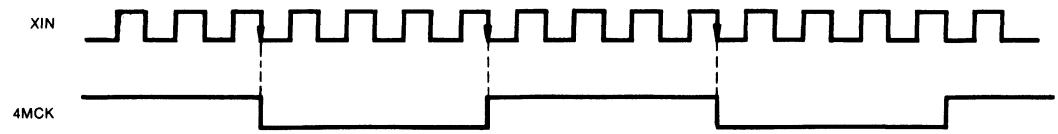
Fig. 8 $\overline{\text{ISTAT}}$ Output Signal by CNTL Register

X'TAL OSCILLATION

1) Block Diagram



2) Timing Chart (SEL = 0) in Use f = 16.9344MHz X'tal OSC.



3) Timing Chart (SEL = 1) in use f = 8.4672MHz X'tal OSC.

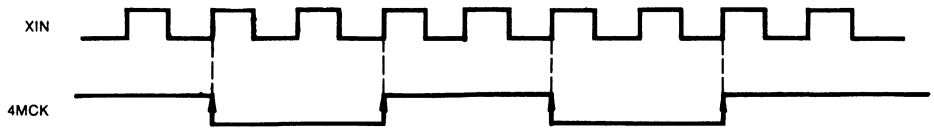


Fig. 9

DIGITAL FILTER

KS5990 is built-in 17th FIR Digital Filter.
The digital filter consists of RAM, multiplier, serial to parallel and parallel to serial converter and controller.

1) Block Diagram

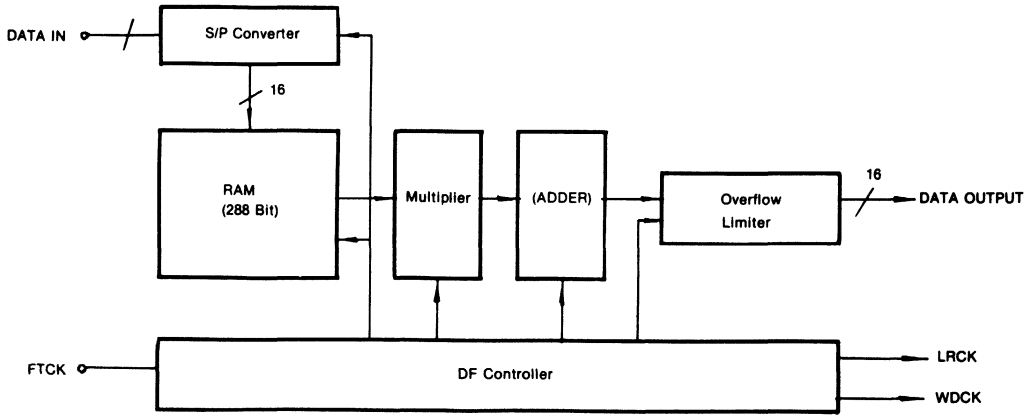


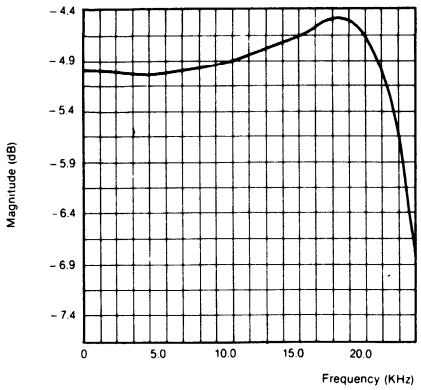
Fig. 10

2) Specification

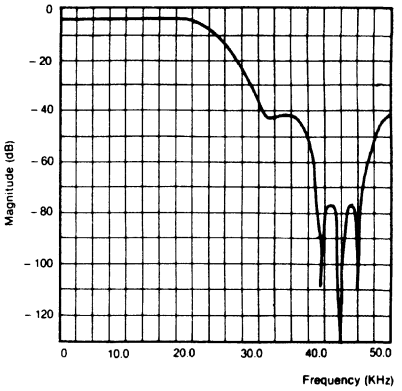
	DC through 18KHz ripple 20KHz of attenuation against 1KHz	±0.07dB max 0.65dB max
	44.1 ± 1KHz attenuation against 1KHz 44.1 ± 5KHz attenuation against 1KHz 44.1 ± 10KHz attenuation against 1KHz 44.1 ± 20KHz attenuation against 1KHz – 30dB frequency range against 1KHz – 60dB frequency range against 1KHz	87dB min 58dB min 44dB min 10dB min 44.1 ± 14KHz 44.1 ± 4KHz

3) Frequency Characteristic

A. Ripple Characteristic Graph



B. Low Pass Filter Frequency Characteristic Graph



EFM BLOCK

The EFM Block is made up of an EFM Demodulator which demodulates the EFM data inputted from a recorded disc, EFM Phase Detector, Frame Sync Detector/Protector/Inserter, Subcode Sync Detector, and Controller for the EFM Block.

1) EFM Phase Detector

As the EFM signal inputted from the disc contains a 2.16 MHz component, a 4.32 MHz bit clock is generated to detec the phase of the signal. The PBCK outputs the result to the PHAS terminal after detecting the phase on the edge of the EFM signal. The relationship between the EFM signal and the PBCK is explained in the following Timing Chart.

A. In normal operation

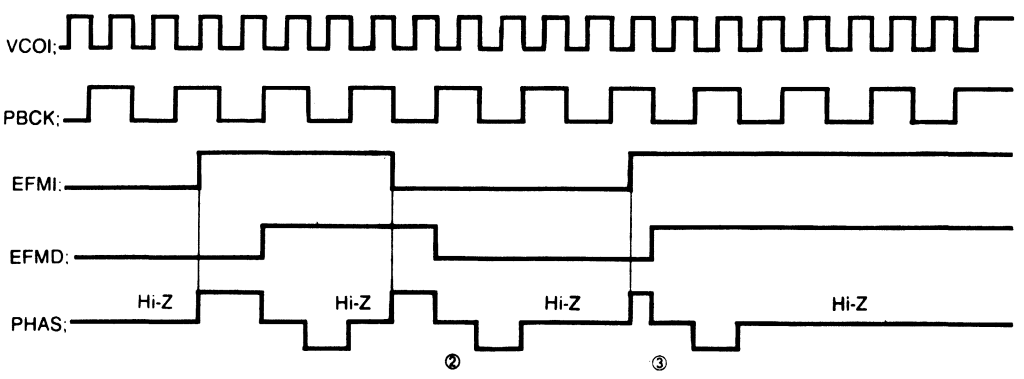


Fig. 11 EFM Phase Detection Timing Chart

Case ① : When the EFM signal is slower than the VCO
Case ②: When the EFM signal is locked up the VCO
Case ③: When the EFM signal is faster than the VCO

B. In abnormal operation

When the HIPD of CNTL-Z is chosen as 'L' from M-COM, the detector of the EFM phase operates as in Fig. 11 When the HIPD is 'H' and the time 'L' of LKFS is below 3.5T, against a PBFS period T, it outpputs Hi-Z to the PHAS terminal as long as "L". When it is above 3.5T, it outputs Hi-Z as long as 3.5T.

2) EFM (Eight to Fourteen) Demodulator

The modulated 14 bit Data is inputted from a disc, then it is inputted into a NRZ-I circuit. As the EFM Data passes by the NRZ-I circuit which converts 14 bit data into 8 bit data, it gets demodulated as 8 bit data. There are two kinds of demodulated data: subcode and PCM data. The subcode data is inputted into the subcode Block, and the PCM Data is written into 16KSRAM by, with both CE and WE signals.

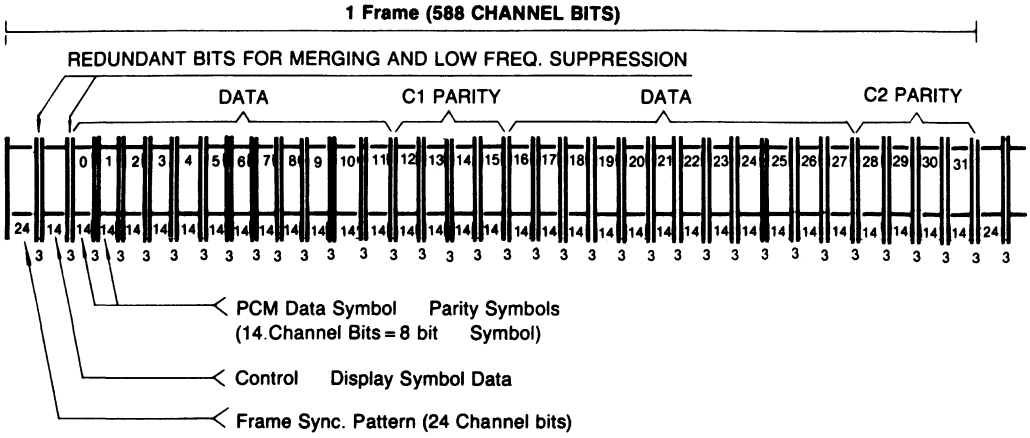
3) Frame Sync Detector/Inserter/Protector

A. Frame Sync Detector

CDP data are composed of units of a frame. A frame is made up of Frame Sync, Subcode Data, PCM Data, and Redundancy Data. A Frame sync is detected per frame against this format.

B. Frame Sync Protector/Inserter

There are cases in which the Frame Sync is left out or detected from the data beside the frame sync because of the effects of an error on the disk or Jitter. In this case the frame sync needs to be protected and inserted. To protect the frame sync, a window is made by the use of a WSEL signal of CNTL-S Reg. The frame sync which comes into the window is true data, and the frame sync deviating from the window is disregarded.



(Frame Format)

The width of the window is determined by the WSEL signal from the CNTL-S Reg. (cf. CNTL-S) being inserted in the frame When the frame sync reaches the number of a frame designated by the FSEM and FSEL, using the CNTL-S Reg, ULKFS becomes 'L' and the frame sync protection window is disregarded. In this case, an outputted frame sync is unconditionally accepted. After the frame sync is received, the ULKFS signal becomes 'H' and accepts a frame sync detected inside the window.

LKFS	ULKFS	Explanation
I	I	When a play back frame sync coincides with a generated frame sync.
O	I	① When a PBFR sync is detected in the window chosen by WSEL even if a play back frame sync does not coincide with a generated frame sync ② In the case of sync insertion, when PBFR sync does not coincide with a XTER sync and a frame sync within the window chosen by WSEL is not detected.
O	O	①After inserting a sync as many as times the number of frames decided by the FSEM and FSEL by the CNTL-S Reg., because Frame Sync is not detected within a window. ②When PBFR sync is not continuously detected after situation ① happens.

SUBCODE BLOCK

The 14 bit subcode sync signal S0, S1 is outputted to the Subcode Sync Block. In a frame delay after the output of S0, S1 is outputted. In this case, the signal of S0 + S1 is outputted through the S0S1 terminal, and the signal of S0·S1 is outputted through the SDAT terminal, when the signal S0S1 becomes 'H'. After the 14 bit Subcode Data inputted to the EFMI terminal has the EFM demodulated, an 8-bit P, Q, R, S, T, U, V, W subcode datum is outputted to SDAT by SBCK clock after it syncronizes with the signal PBFR. Only Q data are chosen among the 8 subcode data, and it is loaded on to 80 shift registers. The CRC-checked results of the loaded data is synchronized with the S0S1 rising edge, and is outputted to the SQCK terminal.
If the result of CRC checking is an error, 'L' is outputted to the SQCK terminal. If it is true, 'H' is outputted to the SQOK terminal. If the CRCD of CNTL-Z mode is 'H', the result of CRC checking is outputted to the SQDT terminal from the S0S1 section 'H' to the period of the SQCK falling edge.
The timing chart of a subcode block is as follows:

1) In SQEN = 'L': SDAT, SQDT, S0S1, SQOK, VCOI Timing Relation

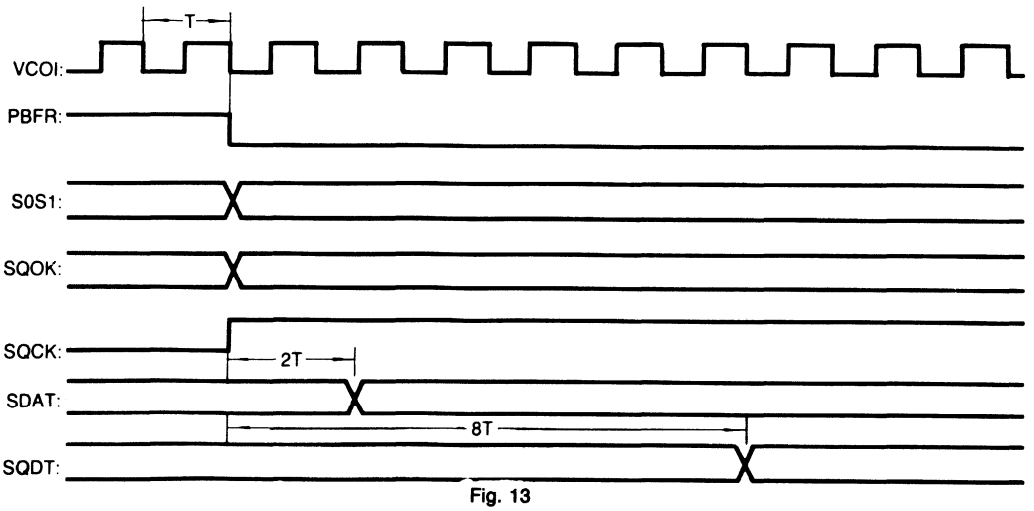


Fig. 13

2) In SQEN = 'L': SQOK, SQDT, S0S1, Timing Chart

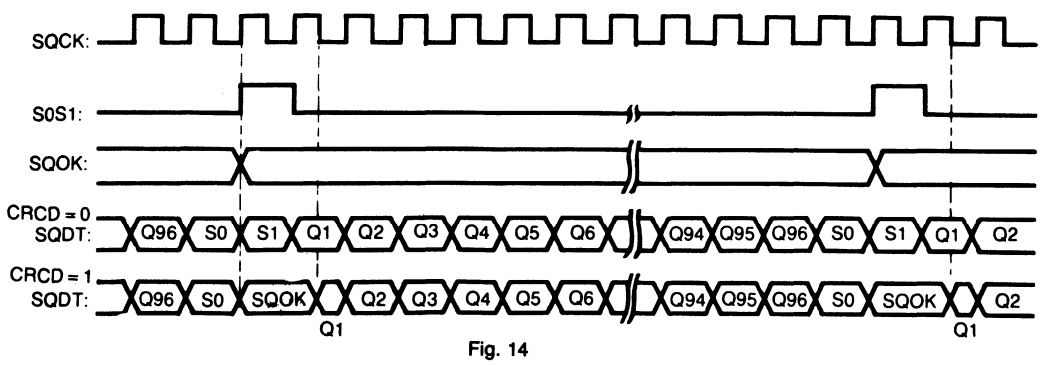
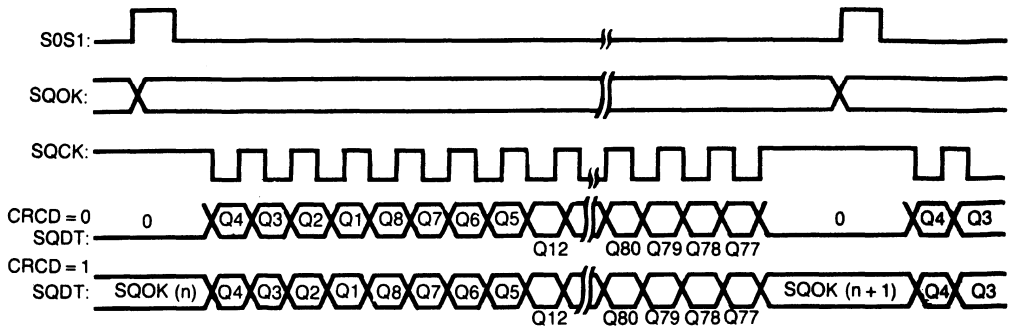


Fig. 14

3) In SQEN = 'H': SQOK, SQDT, S0S1, SQCK Timing Chart



Comment: When a SQOK of subcode Q Data is 'H', subcode data is outputted to SQDT according to SQCK. When SQOK is 'L', 'L' is outputted to the SQDT terminal.

Fig. 15

4) VCO1, SDAT, SBCK Timing Chart

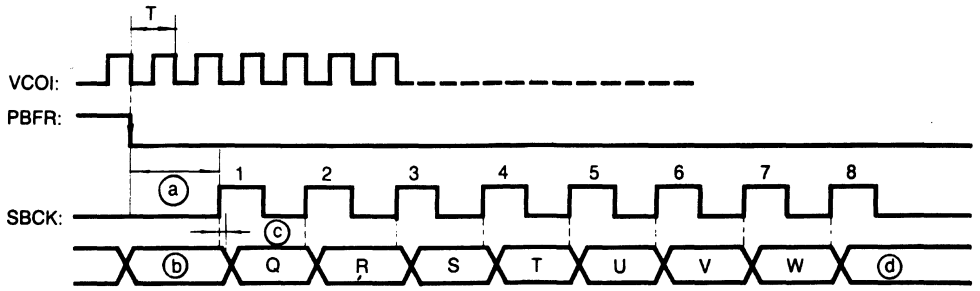


Fig. 16

ⓐ : SBCK is set to "L" for about 10μS after PBFR becomes a falling edge.

ⓑ : When S0S1 is 'L', a subcode P is outputted. When S0S1 is 'H', S0S1 is outputted.

ⓒ : When a cycle of VCO1 is 'T', the width of ⓒ is 4T ~ 6T.

ⓓ : When the pulse inputted to the SBCK terminal is above 7, subcode data P, Q, R, S, T, U, V, W data are repeated.

ECC (Error-Correction Code) Block

The function of ECC Block is to recover damaged data to some extent when data on a disk is damaged. By using CIRC (Crossed-Interleave Reed-Solomon Code), C1 (32, 28) and C2 (28, 24) errors are corrected. ECC is performed with an 8-bit as a symbol unit. In correcting C1, a C1 Pointer is generated, and in correcting C2, a C2 pointer is generated. C1, C2 Pointers send error information or the data to which ECC is given. After correcting C2, against uncorrectable data, Error Data is sent by outputing a C2 Flag.
The signal C2FL is AND signal of C2F1 and C2F2. By using this information, Data is treated in the interpolator block.

C1F1	C1F2	C1, C2 Error	C2F1	C2F2	C2FL
0	0	No Error	0	0	0
0	1	Single Error	0	1	0
1	0	Double Error	1	0	0
1	1	Irretrievable Error	1	1	1

Fig. 17

C1F1, C1F2 — Output the state of an error correction by C1 Decoder

C2F1, C2F2 — Output the state of an error correction by C2 Decoder

C2FL — Becomes 'L' when an error correction by C2 Decoder is possible and an 'H' error correction is impossible.

16K SRAM BLOCK

After EFM demodulation of EFM modulated data inputted from disc, when the data is written into RAM is outputted to Read/Write and D/A Converters in ECC Processing for reading a SRAM Address Generator and a 16K SRAM is installed. SRAM terminal must be 'H' in a 16K SRAM application.

1) Address Generation Priority Control

Writing in EFM demodulation, reading the data with R/W, and a D/A Converter in the ECC process are sometimes required at the same time.
When 3 signals are demanded at the same time, priority of the data process needs to be controlled. Priority is D/A Converter Read demand > EFM Write demand > ECC R/W demand.

2) EFM Demodulation Data Write Demand

EFM demodulated data must be written to SRAM. Priority is controlled when the write demand signal is transmitted to the SRAM Address Generator, and the Enable signal is transmitted to the EFM Block. The generated address is transmitted to the SRAM Interface circuit.
A generated address is data in which deinterleave is considered, and a frame 32 address is generated.

A. In the use of 16K SRAM (in EFM & ECC Write): SRAM terminal 'H'

DB1 ~ DB8 and AD1 ~ AD11 terminals are in a state of Hi-Z. $\overline{CE}$ and $\overline{WE}$ are 'Don't Care.'

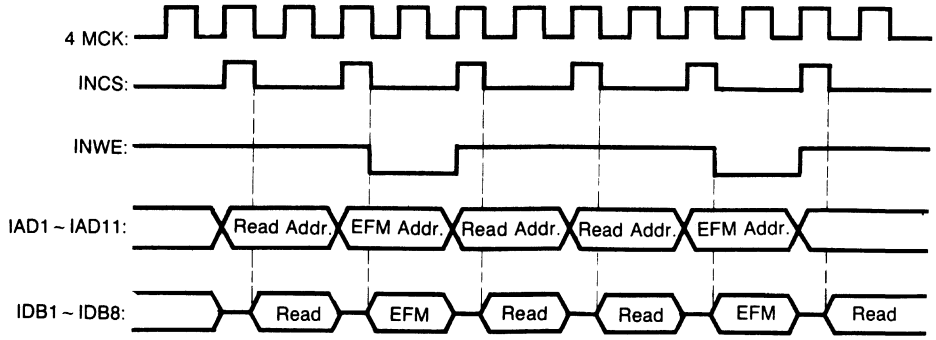
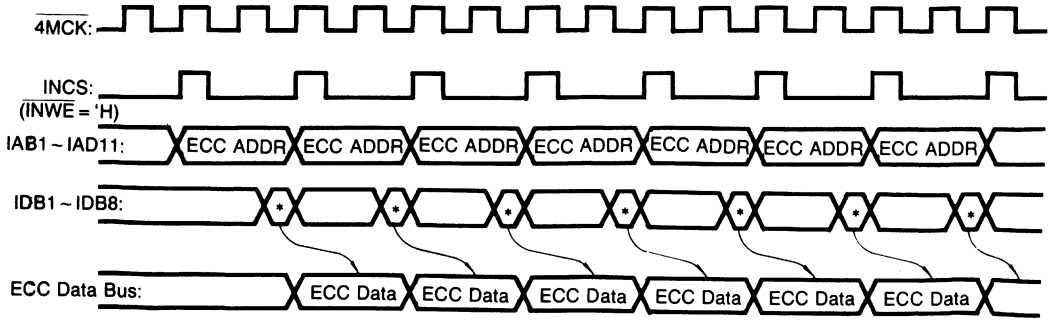


Fig. 18

3) R/W Demand of ECC Data

For C1 and C2, ECC treatment is 129 times of the Address demand signals generated, due to an R/W operation, and must be given to 64 PCM data and 65 Pointers during a frame.
The write of FCC processing is the same as 2) an EFM Write operation.
In reading, it is as follows:

A. In the use of 16K SRAM Reading Timing (SRAM: H)



*: Valid ECC Data

Fig. 19

4) D/A Converter Read Demand

Since each 6 sampling data on the left and right channel and 12 C2 Pointer data must be read for a frame, 36 read enable demand signals are caused. The timing chart for a D/A Converter Read is the same as the R/W demand block of ECC data. As a result, the number of the maximum R/W operation action demanded for a frame is 179.

5) Address Generated Block

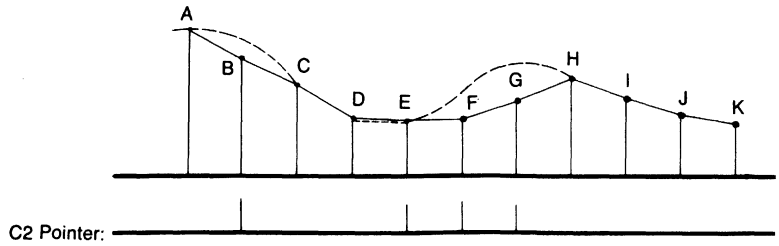
The interleaving data in encoding is deinterleaved in decoding. The data of 108 frames is needed to get 8 frames of PCM data in a CDP format. To get data suitable for a CDP format, 2 counters are needed. A write base counter is used to write. EFM demodulation data are hindered in storing data in SRAM due to disk shaking, the instability of a servo system, etc.

6) Jitter Margin

EFM demodulation data are hindered in storing data in SRAM due to disk shaking, the instability of a servo system, etc. Now that the data that must be kept is limited by the size of SRAM in view of time, data is destroyed if the value of the read/write base counter has a difference above ± 5 frames. Loading into the value of the write base counter with enforcement, the value of read the base counter has a jitter margin below ± 4 frames when there is a difference of over ± 5 frames in the read/write base counter value.
A read base counter value is loaded into a write base counter with enforcement when data on the left and right channels are all muting, or when NCLV is 'H' and CLV-Servo is stop, forward or reverse. When the difference between the read/write base counter is above ± 4 frame, a 'H' signal is outputted to the JIT terminal for a period.

INTERLEAVE, MUTE BLOCK

When a burst error occurs on a disk, sometimes the data can't be corrected even if a ECC process is conducted. An interpolator block revises data by using a C2 Pointer outputted through the ECC Block. PCM data inputted to a data bus are inputted to the left and right channels, respectively, in the order of 8-bit C2 Pointer, Lower 8-bit, and Upper 8-bit. A pre-hold method is taken when a DA Flag is 'H' continuously. In case of the occurrence of a single error, a mean value interploating method is carried out with the range of the PCM Data before and after an error happens. When a check against a checked cycle is 'L', R-CH Data is outputted. L-CH Data is outputted when the check is 'H'. For the timing chart of an interpolator block see figure 6.



$B = \frac{A+C}{2}$: Mean value interpolation

F = E = D : Pre-hold interpolation

G = F + H : Mean value interpolation

Fig. 20

2) Mute and Attenuation

By using a Mute terminal and the ATTM signal of the CNTL-S Reg., AUDIO data is muted or reduced. There are two kinds of mute: zero-cross muting and muting.

A. Zero-Cross Muting
Audio data is muted when a mute terminal is 'H' and when 6 bits in a high position of Audio Data are all 'H' or 'L'.

B. Muting
Audio data is muting when ZCMT of the CNTL-Z Reg. is 'L' and when a mute terminal is 'H'.

C. Attenuation
By means of the ATTM signal of the CNTL-S Reg. and the signal of the Mute terminal, an audio signal attenuation occurs as the following.

ATTM	MUTE	Degree of Attenuation
0	0	0 dB
0	1	$-\infty$ dB
1	0	- 12 dB
1	1	- 12 dB

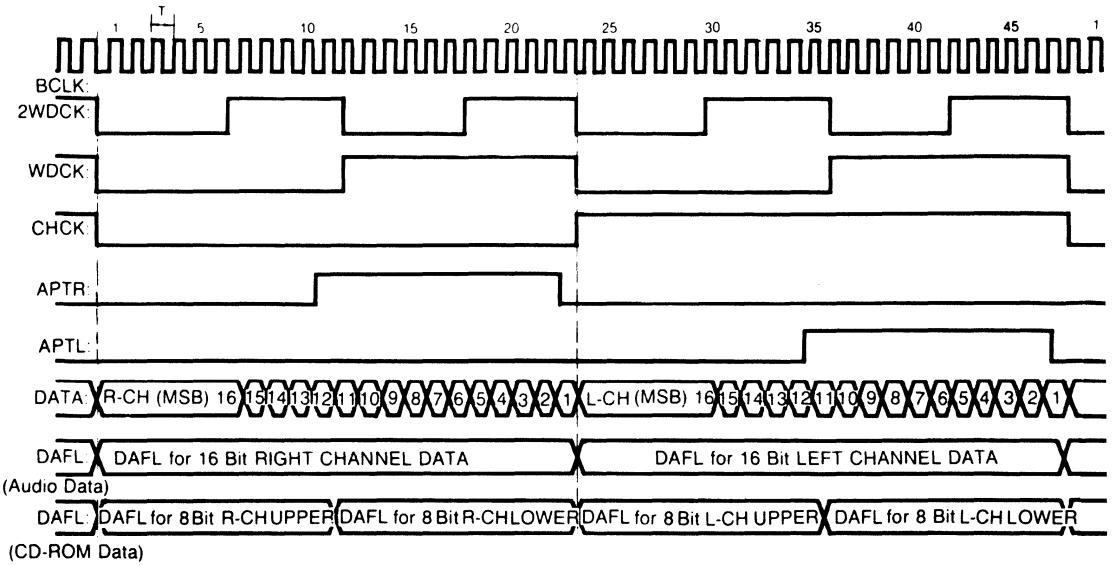


Fig. 21. When Sel. 5 is 'L', and DF is off, the Timing Chart of PCM Data

CLV SERVO

CNTL-C Reg. is selected to control CLV Servo by the Data inputted from μ-COM. In CNTL-C Reg, the data from μ-com appoints CLV servo action mode and controls the spindle motor.

1) Forward

The states of output terminal, related to the mode that rotates a spindle motor forward, are SMDP = 'H', SMSD = Hi-Z, SMEF = 'L' and SMON = 'H', respectively.

2) Reverse

The modes to rotate a spindle motor reversly are SMDP = 'L', SMSD = 'Hi-Z', SMEF = 'L', and SMOD = 'H'.

3) SPEED-Mode

The SPEED-Mode is the mode for the rough control of a spindle motor when a track is jumps or a EFM phase is unlocked. If a cycle of VCO is 'T', the pulse width of a frame sync is '22T'. Sometimes an EFM signal is above 22T, due to noises on a disc, etc. A correct frame sync cannot be detected when the signal is not removed. In this case, the pulse width of an EFM signal is detected at a cycle of XTFR/2 or XTFR/4, which are peak hold clocks. The pulse width an of EFM signal is detected at a cycle of XTFR/16 or XTFR/32, which are bottom hold clocks. The value detected is used for a frame synchronization signal. When the frame synchronization signal is smaller than 21T, the SMPD terminal outputs 'L'. When it is 22T, Hi-Z is outputted. 'H' is outputted when it is above 23T.
When the GAIN signal of CNTL-W Reg. is 'L', the SMDP terminal is outputted after being attenuated at – 12dB. When the signal is 'H', the terminal is outputted without any attenuation. <cf. figure 22>
In SMSD, SMEF, and SMON terminals Hi-Z, 'L', and 'H' are outputted.

4) HSPEED-Mode

The rough servo mode, which moves 20,000 tracks in high speed, acts between the inside of the CD and the outside of the CD. In the domain of a mirror of the track without, a pit EFM and the signal of 20KHz overlap. In this case, since in a speed-mode the peak range of a longer mirror signal than the original frame sync is detected, a servo operation becomes unstable. In HSPEED-mode, a peak hold uses a 8.4672/256 MHz signal, and a bottom hold removes a mirror component and stabilizes the high speed servo operation by using an XTFR/16 or XTFR/32 period signal.
In SMSD, SMEF, and SMON terminals, Hi-Z, 'L', and 'H' are outputted.

5) PHASE-Mode

A PHASE Mode is the mode that control an EFM Phase. When NCLV of CNTL-Z is 'L', it detects a phase difference between PBFR/4 and XTFR/4, and when NCLV is 'H', it detects the phase difference between Read base Counter/4, and write base Counter/4, and then outputs to the SMPD terminal. See figure 8.
If the VCO/2 signal cycle is put as 'T' and the PBFR, during a 'H' period, as a V_{pb}, it outputs 'H' to a SMSD terminal from the falling edge of PBFR for (W_{pb}-278T) x 32, and later outputs 'L' to the falling edge of PBFR. Refer to figure 24

6) XPHSP-Mode

A XPHSP mode is the mode used in normal operation. It samples a LKFS signal made in the frame sync block at a cycle of PBFR/16. After sampling 'H', DHASE mode is carried out. When 'L' is sampled continuously 8 times, it goes over to speed-mode. CNTL-W Reg. decides the choice of the peak hold of the speed-mode, the bottom hold cycle of SPEED-and HSPEED-Mode, and the choice of a gain.

7) VPHSP-Mode

A VPHSP-Mode is the mode used for rough servo control. It uses VCO instead of X'tal in the EFM pattern test. When the range of VCO center changes, VCO is easily loaded because the rotation of a spindle motor changes in the same direction.

8) STOP

Stop is the mode used to stop a spindle motor.
SMDP = 'L', SMSD = Hi-Z, SMEF = 'L', SMON = 'L'

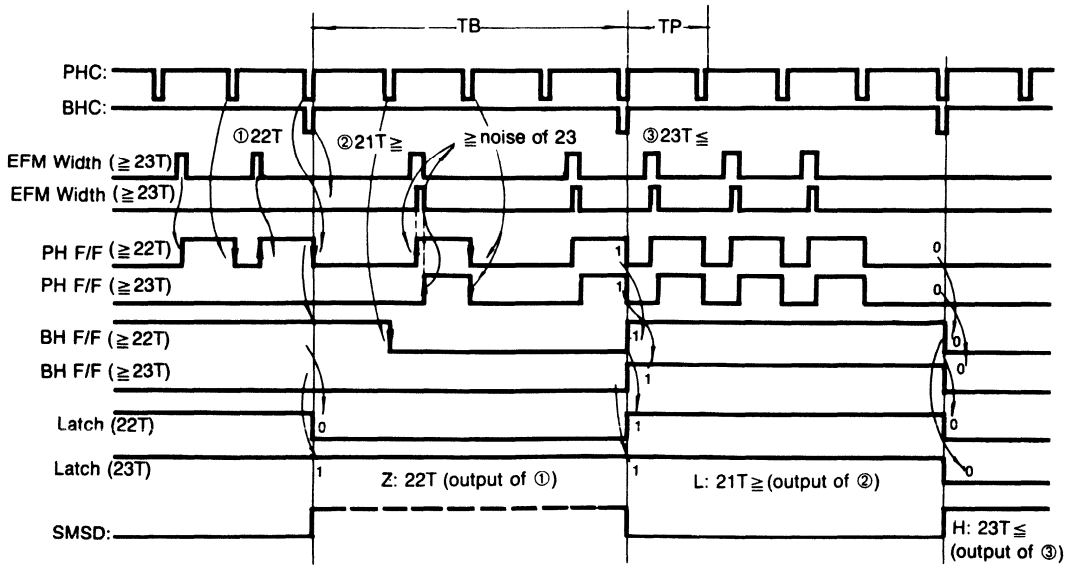


Fig. 22 When gain is 'H' in a speed-mode Timing Chart of SMSD output

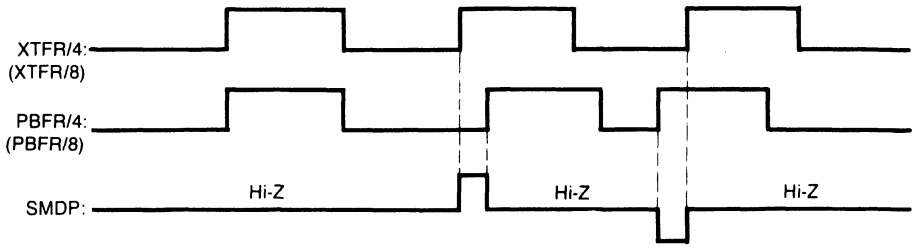
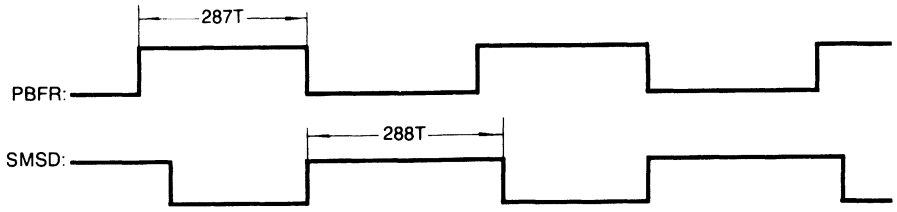
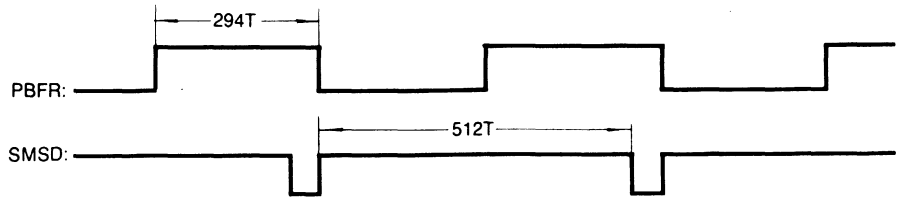


Fig. 23 Output Timing Chart of a SMDP terminal



(a) When PBFR is 287T, Timing Chart of SMSD output

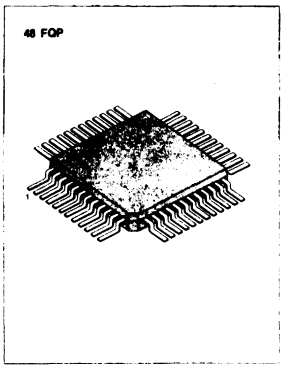


(b) When PBFR is 294T, Timing Chart of SMSD output

Fig. 24 In a PHASE Mode Timing Chart of SMSD output (T: VCO/2)

SERVO SIGNAL PROCESSOR

The KA9221 is a Bi-Mos integrated circuit designed for the servo control of the compact disc players application.



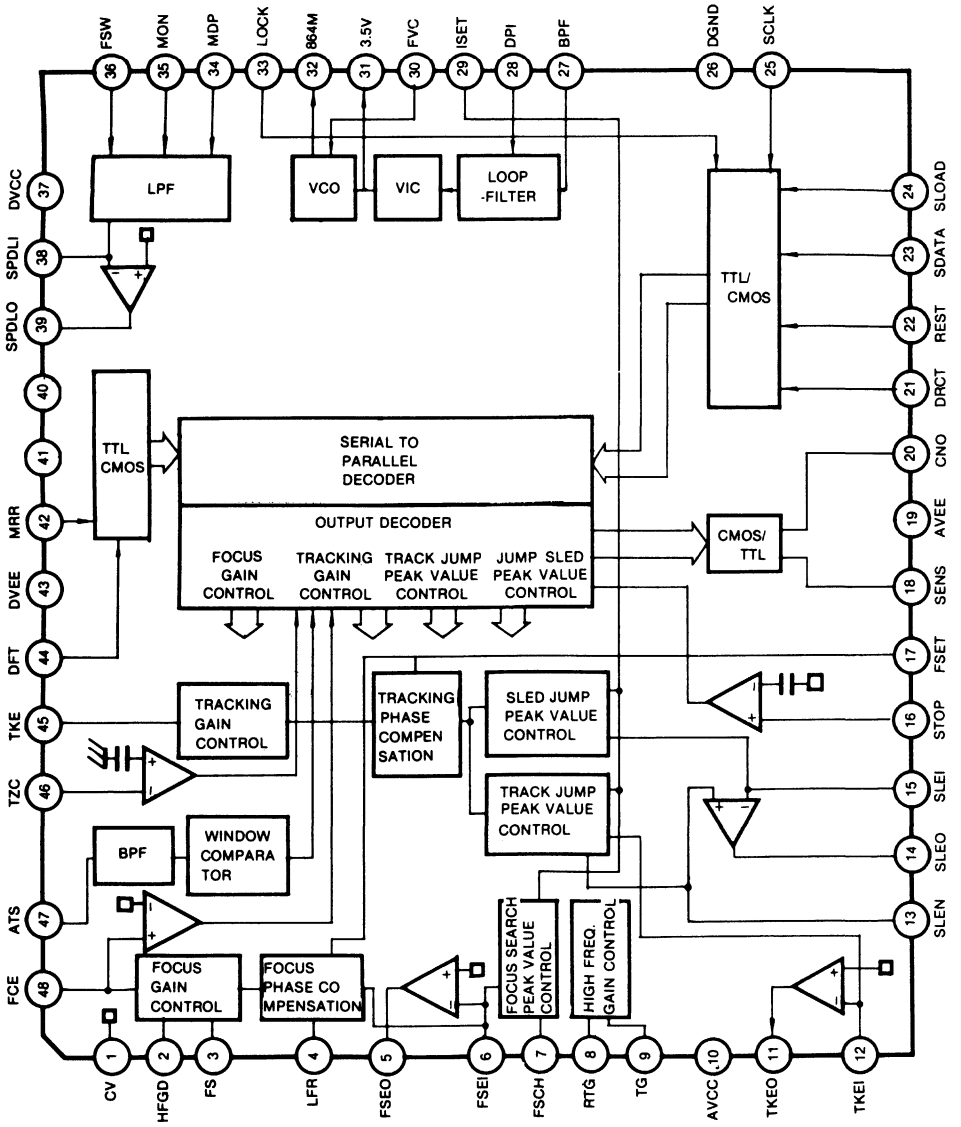
FEATURES

- **Servo control functions:**
  (Focus, tracking, sled servo control)
- **Loop filter and VCO for EFM clock reproduction PLL**
- **Provide function**
  Preventing sled runway Anti-shock
  Spindle servo
- **Provide adjustable peak of focus search,**
  track jump and sled kick with external resister
- **Low power consumption: 80 mW at 5V**
- **Operating supply voltage range: 3.4 ~ 5.5V**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA9221	48 QFP	−20°C ~ +75°C

BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Symbol	Descriptions
1	CV	Center Voltage
2	HFGD	Reduce high frequency gain with capacitor connected between pin 2 and pin 3.
3	FS	High frequency gain of focus servo can be changed by switching FS3 on or off.
4	LFR	Rising low frequency bandwidth of focus loop.
5	FSEO	Focus servo error output.
6	FSEI	Inverting input pin for focus amplifier.
7	FSCH	Time constant external pin to generate focus search wave form.
8	RTG	Time constant external pin to swich the tracking gain of high frequency.
9	TG	Provide time constant to change the high frequency tracking gain.
10	AV_{CC}	Analog positive power supply.
11	TKEO	Tracking error output.
12	TKEI	Inverting input pin for tracking amplifier.
13	SLEN	Non-inverting input pin for tracking amplifier.
14	SLEO	Sled output.
15	SLEI	Inverting input pin for sled amplifier
16	STOP	Pin for detecting a signal for the on/off limit switch of the innermost part of the disc.
17	FSET	Setting the peak frequency of the focus, tracking phase compensation and to of the CLVLPF.
18	SENS	Output pin for FZC, AS TZC, STOP and BUSY by command from CPU.
19	AV_{EE}	Analog negative power supply.

PIN DESCRIPTION (Continued)

Pin No.	Symbol	Descriptions
20	CNO	Track number count output
21	DRCT	Control pin for one track jump
22	REST	Reset input pin, reset at "L".
23	SDATA	Serial data input.
24	SLOAD	Latch input.
25	SCLK	Serial data transfer clock.
26	DGND	Digital ground.
27	BPF	Provide time constant for the loop filter.
28	DPI	Input pin for detected phase
29	ISET	Cunent is input, determining the peaks of focus search, track jump, and sled kick.
30	FVC	External resister to adjust free runing frequency of VCO.
31	VREGI	External regulator voltage input pin for VCO.
32	864M	Output pin of 8.64MHz VCO.
33	LOCK	Pin for the operation of the sled runway prevention circuit at "L".
34	MDP	Pin for connecting the DSP.
35	MON	Pin for connecting the DSP.
36	FSW	Providing an external LPF time constant of the CLV servo.
37	DV_{CC}	Digital positive power supply.
38	SPDLI	Inverting for spindle servo amplifier.
39	SPDLO	Spindle servo error output.
40	N.C	No connecting
41	N.C	No connecting
42	MRR	Mirror signal input pin.
43	DV_{EE}	Digital negative power supply.
44	DFT	Defect signal input pin.
45	TKE	Tracking error signal input pin.
46	TZC	Input pin for the zero cross tracking comparator.
47	ATS	Input pin for detect ATSC.
48	FCE	Input pin for focus error signal.

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	$V_{CC} - V_{EE}$	12	V
Power Dissipation	P_D	600	mW
Operating Temperature	T_{OPR}	−20 ~ +75	°C
Storage Temperature	T_{STG}	−55 ~ +150	°C

ELECTRICAL CHARACTERISTICS (I)

(Ta = 25°C, Pin 10 = Pin 37 = 2.5V, Pin 19, Pin 26, Pin 43 = −2.5V, Pin 31 = 1V, Pin1 = 0V, S42: 2, Unless otherwise specified)

	Characteristic	No.	Symbol	Test Conditions	Min	Typ	Max	Unit
	Circuit Current 1	1	I_{CC1}		2.0	5.3	10.0	mA
	Supply Current 2	2	I_{CC2}		5.0	11.0	15.0	
	Supply Current 3	3	I_{CC3}		−12.0	−7.8	−2.0	
	Supply Current 4	4	I_{CC4}		−14.0	−9.4	−4.0	
Focus Servo	DC Voltage Gain	5	A_{VF}	V_2 = 0.1V	19	21	23	dB
	Offset Voltage	6	V_{offF}		−110	0	110	mV
	Output High Voltage 1	7	V_{FH1}	V_2 = 0.5V	2.0			V
	Output Low Voltage 1	8	V_{FL1}	V_2 = −0.5V			−2.0	V
	Output High Voltage 2	9	V_{FH2}	V_2 = 0.5V	1.2			V
	Output Low Voltage 2	10	V_{FL2}	V_2 = −0.5V			−1.2	V
	Search Voltage 1	11	V_{FS1}		−0.62	−0.50	−0.38	V
	Search Voltage 2	12	V_{FS2}		0.38	0.50	0.62	V
	Feed Through	13	A_{FF}	SG48 = 10KHz, 40mVp-p Gain difference between 08 and 00 of SD			−35	dB
	AC Gain 1	14	A_{F1}	SG48 = 1.2KHz, 200mVp-p	20.5	23.4	26.0	dB
	AC Gain 2	15	A_{F2}	SG48 = 1.2KHz, 200mVp-p	15.5	18.0	21.0	dB
	AC Phase 1	16	P_{FA1}	SG48 = 1.2KHz, 200mVp-p Phase difference between input (Pin 48) and output (Pin 5)	40	60	80	deg
	AC Phase 2	17	P_{FA2}	SG48 = 1.2KHz, 200mVp-p Phase difference between input (Pin 48) and output (Pin 5)	40	65	90	deg
Tracking Servo	DC Voltage Gain	18	A_{VT}	V_8 = −0.2V	13	15	17	dB
	Offset Voltage	19	V_{offT}		−100	0	100	mV
	Output High Voltage 1	20	V_{TH1}	V_8 = −1.5V	2.0			V
	Output Low Voltage 1	21	V_{TL1}	V_8 = 1.5V			−2.0	V
	Output High Voltage 2	22	V_{TH2}	V_8 = −1.5V	1.2			V
	Output Low Voltage 2	23	V_{TL2}	V_8 = 1.5V			−1.2	V
	Jump Voltage 1	24	V_{TJ1}		−0.61	−0.5	−0.39	V
	Jump Voltage 2	25	V_{TJ2}		0.42	0.5	0.61	V
	Feed Through	26	A_{TF}	SG45 = 10KHz, 50mVp-p Gain difference between 25 and 20 of SD			−39	dB
	AC Gain 1	27	A_{T1}	SG45 = 1.2KHz, 200mVp-p	11.3	14.5	16.7	dB
	AC Gain 2	28	A_{T2}	SG45 = 1.2KHz, 200mVp-p	19.5	22.0	24.0	dB

ELECTRICAL CHARACTERISTICS (Continued)

	Characteristic	No.	Symbol	Test Conditions	Min	Typ	Max	Unit
	AC Phase 1	29	P_{TA1}	SG45 = 1.2KHz, 200mVp-p Phase difference between input (Pin 45) and output (Pin 11)	−135	−125	−100	deg
	AC Phase 2	30	P_{TA2}	SG45 = 2.7KHz, 200mVp-p Phase difference between input (Pin 45) and output (Pin 11)	−195	−150	−80	deg
	Defect Output Voltage	31	V_{DFCT}	SG45 = 1.2KHz, 200mVp-p	−240	0	240	mV
Sled Servo	DC Voltage Gain	32	V_{VSL}	SG13 = 100Hz, 100mVp-p	21.2	22.7	24.2	dB
	Output High Voltage 1	33	$V_{SLH}1$	V_7 = 0.4V	2.0			V
	Output Low Voltage 1	34	$V_{SLL}1$	V_7 = −0.4V			−2.0	V
	Output High Voltage 2	35	$V_{SLH}2$	V_7 = 0.4V	1.2			V
	Output Low Voltage 2	36	$V_{SLL}2$	V_7 = −0.4V			−1.2	V
	Kick Voltage 1	37	$V_{SK}1$		0.47	0.58	0.70	V
	Kick Voltage 2	38	$V_{SK}2$		−0.70	−0.58	−0.47	V
	Feed Through	39	A_{SLF}	SG13 = 10KHz, 100mVp-p Gain difference between 25 and 20 of SD			−34	dB
Spindle Servo	Spingle Gain	40	A_{VSP}	SG34 = 100Hz, 200mVp-p	14.5	16.5	18.5	dB
	Output High Voltage 1	41	V_{SPH1}	V_6 = 1.0V	1.8			V
	Output Low Voltage 1	42	V_{SPL1}	V_6 = −1.0V			−1.8	V
	Output High Voltage 2	43	V_{SPH2}	V_6 = 1.0V	1.15			V
	Output Low Voltage 2	44	V_{SPL2}	V_6 = 1.0V			−1.15	V
	AC Gain	45	A_{SP}	SG34 = 2KHz, 200mVp-p	−7.0	−4.3	−2.0	dB
PLL	VCO Frequency	46	f_{VCO}	V_5 = 0V	7.8	8.6	9.5	MHz
	VCO Deviation 1	47	Δf_1	VCO Frequency deviation from f_{VCO}, V_5 = 148mV	7.5	11.0	14.5	%
	VCO Deviation 2	48	Δf_2	VCO Frequency deviation from f_{VCO}, V_5 = 148mV	−14.5	−11.0	−7.5	%
	VCO Deviation 3	49	Δf_3	VCO Frequency deviation from f_{VCO}, V_5 = 148mV	2.55	4.05	5.55	%
	VCO Level	50	V_{fVCO}	V_5 = 0V	0.992	2.392	3.792	Vp-p
SENS Output Low Voltage		51	V_{SNL}				−1.98	V
CNO Output Low Voltage		52	V_{COL}	SG46 = 10KHz, 2Vp-p, S42:1			−1.98	V
FZC Threshold Voltage		53	$V_{th\ (FZC)}$	Voltage of V when SENS becomes high (= 1.1V) by V1 to V4	40	50	60	mV
ATSC Threshold Voltage 1		54	$V_{th\ (ATSC)\ 1}$		−44	−26	−8	mV
ATSC Threshold Voltage 2		55	$V_{th\ (ATSC)\ 2}$		8	26	44	mV
TZC Threshold Voltage		56	$V_{th\ (TZC)}$		−19	0	19	mV
SSTOP Threshold Voltage		57	$V_{th\ (STOP)}$		−64	−50	−32	mV

ELECTRICAL CHARACTERISTICS (II)

(Ta = 25°C, Pin 10, Pin 37 = 1.7V, Pin 19, Pin 26, Pin 43 = − 1.7V, Pin 31 = 1.7V, Pin 1 = 0V, S42 = 2, unless otherwise specified)

	Characteristic	No.	Symbol	Test Conditions	Min	Typ	Max	Unit
Focus Servo	Offset Voltage	58	V_{offF}		− 110	0	110	mV
	Output High Voltage	59	V_{FH}	V_2 = 0.5V	1.18			V
	Output Low Voltage	60	V_{FL}	V_2 = − 0.5V			− 1.18	V
	Search Voltage 1	61	V_{FS1}		− 0.62	− 0.50	− 0.38	V
	Search Voltage 2	62	V_{FS2}		0.38	0.50	0.62	V
Tracking Servo	Offset Voltage	63	V_{offT}		− 100	0	100	mV
	Output High Voltage	64	V_{TH}	V_8 = − 1.5V	1.18			V
	Output Low Voltage	65	V_{TL}	V_8 = 1.5V			− 1.18	V
	Jump Voltage 1	66	V_{TJ1}		− 0.61	− 0.50	− 0.39	V
	Jump Voltage 2	67	V_{TJ2}		0.39	0.50	0.61	V
Sled Servo	Output High Voltage	68	V_{SLH}	V_7 = 0.4V	1.18			V
	Output Low Voltage	69	V_{SLL}	V_7 = 0.4V			− 1.18	V
	Kick Voltage 1	70	V_{SK1}		0.47	0.58	0.70	V
	Kick Voltage 2	71	V_{SK2}		− 0.70	− 0.58	− 0.47	V
Spindle	Output High Voltage 1	72	V_{SPH}	V_6 = 1.0V	0.98			V
	Output Low Voltage 2	73	V_{SPL}	V_6 = − 1.0V			− 0.98	V

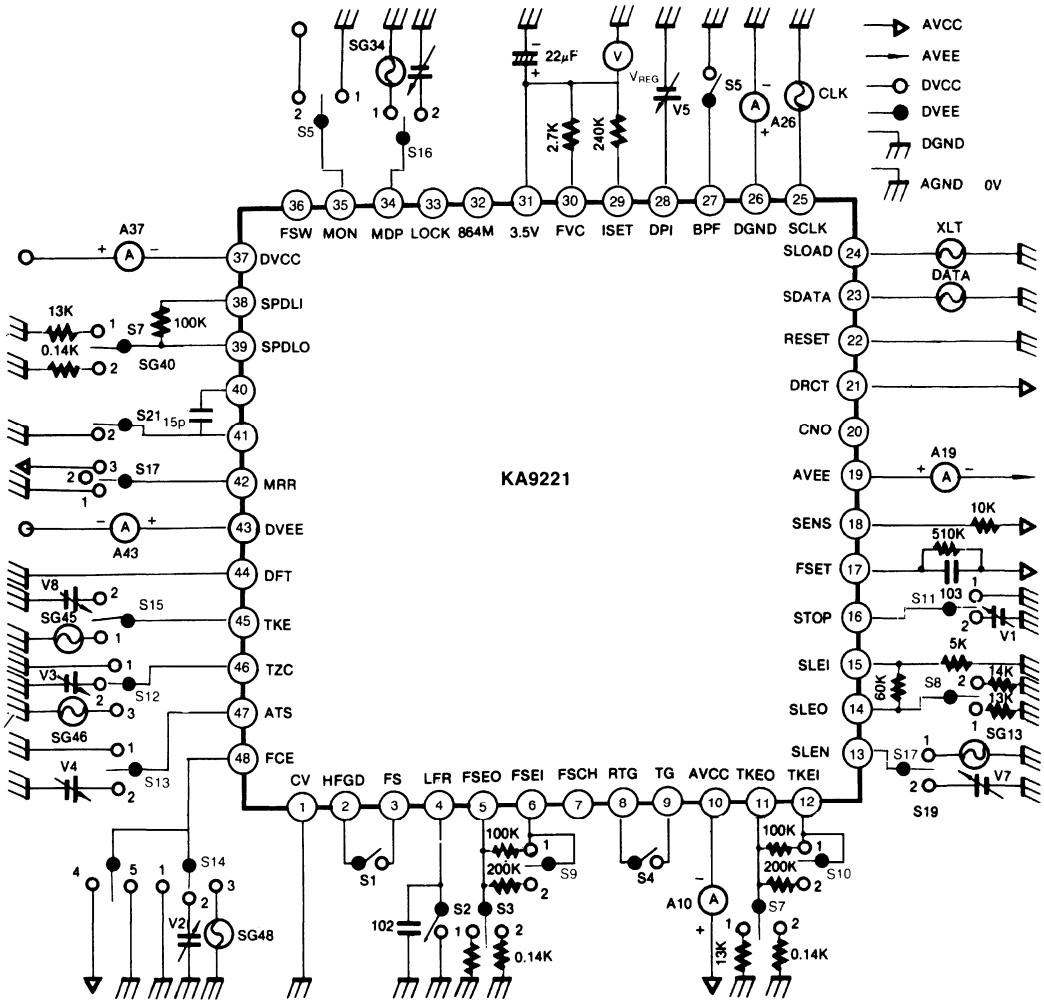
TEST METHODE (SWITCH CONDITIONS)

No.	Symbol	SWITCH Conditions																		I SD	Input Point	Test Point
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18			
1	I_{CC1}	OFF	OFF	1	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	OFF	00		10
2	I_{CC2}	OFF	OFF	1	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	OFF	00		37
3	I_{CC3}	OFF	OFF	1	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	OFF	00		19,23
4	I_{CC4}	OFF	OFF	1	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	OFF	00		26
5	A_{VF}	OFF	OFF	1	OFF	1	1	1	1	1	1	1	1	1	2	1	1	1	ON	08	48	5
6	V_{offF}	OFF	OFF	1	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	ON	08	48	5
7	V_{FH1}	OFF	OFF	1	OFF	1	1	1	1	2	1	1	1	1	1	1	1	1	ON	08	48	5
8	V_{FL1}	OFF	OFF	1	OFF	1	1	1	1	2	1	1	1	1	2	1	1	1	ON	08	48	5
9	V_{FH2}	OFF	OFF	2	OFF	1	1	1	1	2	1	1	1	1	2	1	1	1	ON	08	48	5
10	V_{FL2}	OFF	OFF	2	OFF	1	1	1	1	2	1	1	1	1	2	1	1	1	ON	08	48	5
11	V_{FS1}	OFF	OFF	1	OFF	1	1	1	1	1	1	1	1	1	2	1	1	1	ON	02		5
12	V_{FS2}	OFF	OFF	1	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	ON	03		5
13	A_{FF}	ON	ON	1	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	OFF		48	5
14	A_{F1}	ON	ON	1	OFF	1	1	1	1	1	1	1	1	1	3	1	1	1	ON	08	48	5
15	A_{F2}	ON	ON	1	OFF	1	1	1	1	1	1	1	1	1	3	1	1	1	ON	0C	48	5
16	P_{FA1}	ON	ON	1	OFF	1	1	1	1	1	1	1	1	1	3	1	1	1	ON	08	48	5
17	P_{FA2}	ON	ON	1	OFF	1	1	1	1	1	1	1	1	1	3	1	1	1	ON	0C	48	5
18	A_{VT}	ON	ON	1	OFF	1	1	1	1	1	1	1	1	1	3	2	1	1	ON	25	45	11
19	V_{offT}	OFF	OFF	1	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	ON	25	45	11
20	V_{TH1}	OFF	OFF	1	OFF	1	1	1	1	1	2	1	1	1	1	2	1	1	ON	25	45	11
21	V_{TL1}	OFF	OFF	1	OFF	1	1	1	1	1	2	1	1	1	1	2	1	1	ON	25	45	11
22	V_{TH2}	OFF	OFF	1	OFF	1	1	2	1	1	2	1	1	1	1	2	1	1	ON	25	45	11
23	V_{TL2}	OFF	OFF	1	OFF	1	1	2	1	1	2	1	1	1	1	2	1	1	ON	25	45	11
24	V_{TJ1}	OFF	OFF	1	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	ON	2C		11
25	V_{TJ2}	OFF	OFF	1	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	ON	28		11
26	A_{TF}	OFF	OFF	1	ON	1	1	1	1	1	1	1	1	1	1	3	1	1	ON	13	45	11
27	A_{T1}	OFF	OFF	1	ON	1	1	1	1	1	1	1	1	1	1	3	1	1	ON	25	45	11
28	A_{T2}	OFF	OFF	1	ON	1	1	1	1	1	1	1	1	1	1	3	1	1	ON	25	45	11
29	P_{TA1}	OFF	OFF	1	ON	1	1	1	1	1	1	1	1	1	1	3	1	1	ON	25	45	11
30	P_{TA2}	OFF	OFF	1	ON	1	1	1	1	1	1	1	1	1	1	3	1	1	ON	25	45	11
31	V_{DFCT}	OFF	OFF	1	ON	1	1	1	1	1	1	1	1	1	1	3	1	1	ON	25	45	11
32	A_{VSL}	OFF	OFF	1	OFF	1	1	1	1	1	1	1	1	1	1	3	1	1	ON	25	13	14
33	V_{SLH1}	OFF	OFF	1	OFF	1	1	1	1	1	1	1	1	1	1	1	1	2	ON	25	13	14
34	V_{SLL1}	OFF	OFF	1	OFF	1	1	1	1	1	1	1	1	1	1	1	1	2	ON	25	13	14
35	V_{SLH2}	OFF	OFF	1	OFF	1	1	1	1	1	1	1	1	1	1	1	1	2	ON	25	13	14
36	V_{SLL2}	OFF	OFF	1	OFF	1	1	1	2	1	1	1	1	1	1	1	1	2	ON	25	13	14
37	V_{SK1}	OFF	OFF	1	OFF	1	1	1	2	1	1	1	1	1	1	1	1	2	ON	22		14
38	V_{SK2}	OFF	OFF	1	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	ON	23		14

TEST METHODE (Continued)

No.	Symbol	SWITCH Conditions																		I SD	Input Point	Test Point
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18			
39	A_{SLF}	OFF	OFF	1	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	ON	23		14
40	A_{VSP}	OFF	OFF	1	OFF	2	1	1	1	1	1	1	1	1	1	1	1	1	ON		13	14
41	V_{SPH1}	OFF	OFF	1	OFF	2	1	1	1	1	1	1	1	1	1	1	1	1	ON	25	13	14
42	V_{SPL1}	OFF	OFF	1	OFF	2	1	1	1	1	1	1	1	1	1	1	1	1	ON	34		39
43	V_{SPH2}	OFF	OFF	1	OFF	2	2	1	1	1	1	1	1	1	1	1	1	1	ON		34	39
44	V_{SPL2}	OFF	OFF	1	OFF	2	2	1	1	1	1	1	1	1	1	1	1	1	ON		34	39
45	A_{SP}	OFF	OFF	1	OFF	2	1	1	1	1	1	1	1	1	1	1	1	1	ON		34	39
46	f_{VCO}	OFF	OFF	1	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	OFF		28	32
47	Δf_1	OFF	OFF	1	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	OFF		28	32
48	Δf_2	OFF	OFF	1	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	OFF		28	32
49	Δf_3	OFF	OFF	1	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	OFF		28	32
50	V_{fVCO}	OFF	OFF	1	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	OFF		28	32
51	V_{SNL}	OFF	OFF	1	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	ON			18
52	V_{COL}	OFF	OFF	1	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	ON		46	20
53	$V_{th\ (FZC)}$	OFF	OFF	1	OFF	1	1	1	1	1	1	1	3	1	2	1	1	1	ON	00	48	18
54	$V_{th\ (ATSC)\ 1}$	OFF	OFF	1	OFF	1	1	1	1	1	1	1	1	2	1	1	1	1	ON	10	47	18
55	$V_{th\ (FZC)\ 2}$	OFF	OFF	1	OFF	1	1	1	1	1	1	1	1	2	1	1	1	1	ON	10	47	18
56	$V_{th\ (TZC)}$	OFF	OFF	1	OFF	1	1	1	1	1	1	1	2	1	1	1	1	1	ON	20	46	18
57	$V_{th\ (SSTOP)}$	OFF	OFF	1	OFF	1	1	1	1	1	1	2	1	1	1	1	1	1	ON	30	16	18
58	V_{offF}	OFF	OFF	1	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	ON	08		5
59	V_{TH}	OFF	OFF	1	OFF	1	1	1	1	2	1	1	1	1	2	1	1	1	ON	08	48	5
60	V_{FL}	OFF	OFF	1	OFF	1	1	1	1	2	1	1	1	1	2	1	1	1	ON	08	48	5
61	V_{FS1}	OFF	OFF	1	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	ON	02	48	5
62	V_{FS2}	OFF	OFF	1	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	ON	03	48	5
63	V_{offT}	OFF	OFF	1	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	ON	25		11
64	V_{TH}	OFF	OFF	1	OFF	1	1	1	1	1	2	1	1	1	1	2	1	1	ON	25	45	11
65	V_{TL}	OFF	OFF	1	OFF	1	1	1	1	1	2	1	1	1	1	2	1	1	ON	25	45	11
66	V_{TJ1}	OFF	OFF	1	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	ON	2C		11
67	V_{TJ2}	OFF	OFF	1	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	ON	28		11
68	V_{SLH}	OFF	OFF	1	OFF	1	1	1	1	1	1	1	1	1	1	1	1	2	ON	25	13	14
69	V_{SLL}	OFF	OFF	1	OFF	1	1	1	1	1	1	1	1	1	1	1	1	2	ON	25	13	14
70	V_{SK1}	OFF	OFF	1	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	ON	22	13	14
71	V_{SK2}	OFF	OFF	1	OFF	1	1	1	1	1	1	1	1	1	1	1	1	1	ON	23	13	14
72	V_{SPA}	OFF	OFF	1	OFF	2	1	1	1	1	1	1	1	1	1	1	2	1	ON		34	39
73	V_{SPL}	OFF	OFF	1	OFF	2	1	1	1	1	1	1	1	1	1	1	1	2	OFF		34	39

TEST CIRCUIT



APPLICATION INFORMATION

CPU Serial Interface Timing Chart

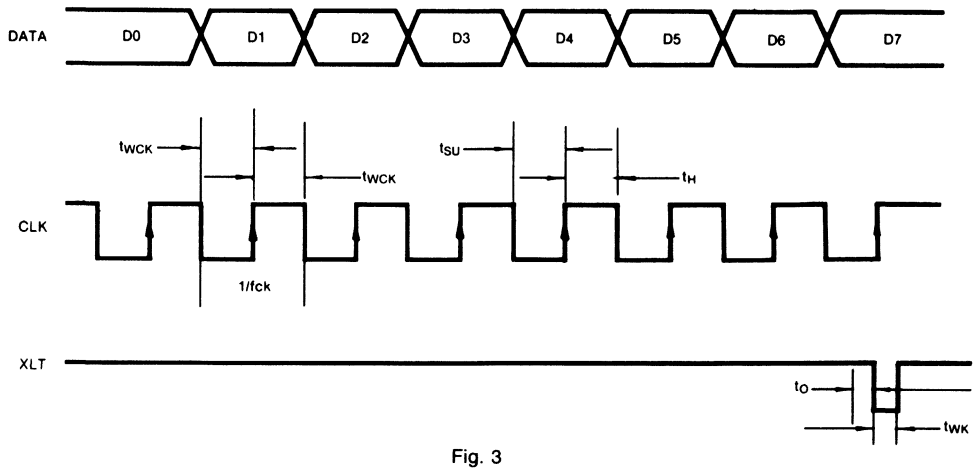


Fig. 3

$DV_{CC} - D_{GND} = 4.5$ to 5.5V

Item	Symbol	Min	Typ	Max	Unit
Clock Frequency	f_{CK}			1	MHz
Clock Pulse Width	f_{WCK}	500			ns
Hold Time	t_{SU}	500			ns
Setup Time	t_H	500			ns
Delay Time	t_D	500			ns
Latch Pulse Width	t_W	1000			ns

SYSTEM CONTROL

Item		Address				Data				Sens Output
		D7	D6	D5	D4	D3	D2	D1	D0	
Focus Control		0	0	0	0	FS4 Focus On	FS3 Gain Down	FS2 Search On	FS1 Search Up	FZC
Tracking Control		0	0	0	1	Anti Shock	Brake On	TG2 TG1 Gain Set *1		A.S
Tracking Mode		0	0	1	0	Tracking Mode *2		Sled Mode *3		TZC
Select		0	0	1	1	PS4 Focus Search + 2	PS3 Focus Search + 1	PS2 Sled Kick + 2	PS1 Sled Kick + 1	SSTOP
Auto Sequence *4		0	1	0	0	AS3	AS2	AS1	AS0	BUSY
	Blind(A,E)/Overflow(C)	0	1	0	1	0.18ms	0.09ms	0.045ms	0.022ms	Hi-Z
	Brake(B)					0.36ms	0.18ms	0.09ms	0.045ms	
	Kick(D)	0	1	1	0	11.6ms	5.8ms	2.9ms	1.45ms	
	Track Jump(N)	0	1	1	1	64	32	16	8	
	Track Move(M)					128	64	32	16	

Note: ***1. GAIN SET**
It is possible to set TG1 and TG2 independently.
When the anti-shock is 1 (00011xxx), invert both TG1 and TG2 when the internal anti-shock is H.

*5 RAM SET

***2 TRACKING MODE**

	D3	D2
OFF	0	0
ON	0	1
FWD JUMP	1	0
REV JUMP	1	1

***3 SLED MODE**

	D1	D0
OFF	0	0
ON	0	1
FWD MOVE	1	0
REV MOVE	1	1

***4 AUTO SEQUENCE**

	AS3	AS2	AS1	AS0
CANCEL	0	0	0	0
FOCUS ON	0	1	1	1
1 TRACK JUMP	1	0	0	X
10 TRACK JUMP	1	0	1	X
2N TRACK JUMP	1	1	0	X
M TRACK MOVE	1	1	1	X

X = 0 FORWARD
X = 1 REVERSE

- When CANCEL $40 is sent, the status immediately preceding the auto sequence mode (just before $4X is sent) is reset.
- The auto sequence mode starts with the first falling of the pin 40 input pulse (WDCK) after the $4X transfer and the falling of latch pulse.

***5 RAM SET**
- Values $0 to $E (not $F) can be set.
- The above set values are ones when WDCK (88.2KHz) is input to pin 40.
- The RAM is preset when the power is switched on and the internal initial set values are as follows:

Address	Data
0 1 0 1	0 1 0 1
0 1 1 0	0 1 1 1
0 1 1 1	1 1 1 0

- The actual count values are slightly different from the set values.

A	set value + 4 to 5	WDCK
B,D,E	set value + 3	WDCK
C	set value + 5	WDCK
N,M	set value + 3	Count out

SERIAL DATA TRUTH TABLE

Serial Data	Hexa.	Function
FOCUS CONTROL		FS = 4321
0 0 0 0 0 0 0 0	$00	0 0 0 0
0 0 0 0 0 0 0 1	$01	0 0 0 1
0 0 0 0 0 0 1 0	$02	0 0 1 0
0 0 0 0 0 0 1 1	$03	0 0 1 1
0 0 0 0 0 1 0 0	$04	0 1 0 0
0 0 0 0 0 1 0 1	$05	0 1 0 1
0 0 0 0 0 1 1 0	$06	0 1 1 0
0 0 0 0 0 1 1 1	$07	0 1 1 1
0 0 0 0 1 0 0 0	$08	1 0 0 0
0 0 0 0 1 0 0 1	$09	1 0 0 1
0 0 0 0 1 0 1 0	$0A	1 0 1 0
0 0 0 0 1 0 1 1	$0B	1 0 1 1
0 0 0 0 1 1 0 0	$0C	1 1 0 0
0 0 0 0 1 1 0 1	$0D	1 1 0 1
0 0 0 0 1 1 1 0	$0E	1 1 1 0
0 0 0 0 1 1 1 1	$0F	1 1 1 1
TRACKING CONTROL		AS = 0 / TG = 2 1 — AS = 1 / TG = 2 1
0 0 0 1 0 0 0 0	$10	0 0 — 0 0
0 0 0 1 0 0 0 1	$11	0 1 — 0 1
0 0 0 1 0 0 1 0	$12	1 0 — 1 0
0 0 0 1 0 0 1 1	$13	1 1 — 1 1
0 0 0 1 0 1 0 0	$14	0 0 — 0 0
0 0 0 1 0 1 0 1	$15	0 1 — 0 1
0 0 0 1 0 1 1 0	$16	1 0 — 1 0
0 0 0 1 0 1 1 1	$17	1 1 — 1 1
0 0 0 1 1 0 0 0	$18	0 0 — 1 1
0 0 0 1 1 0 0 1	$19	0 1 — 1 0
0 0 0 1 1 0 1 0	$1A	1 0 — 0 1
0 0 0 1 1 0 1 1	$1B	1 1 — 0 0
0 0 0 1 1 1 0 0	$1C	0 0 — 1 1
0 0 0 1 1 1 0 1	$1D	0 1 — 1 0
0 0 0 1 1 1 1 0	$1E	1 0 — 0 1
0 0 0 1 1 1 1 1	$1F	1 1 — 0 0

Serial Data	Hexa.	Function		
TRACKING MODE		DIRC = 1 TM = 654321	DIRC = 0 654321	DIRC = 1 654321
0 0 1 0 0 0 0 0	$20	000000	001000	000011
0 0 1 0 0 0 0 1	$21	000010	001010	000011
0 0 1 0 0 0 1 0	$22	010000	011000	100001
0 0 1 0 0 0 1 1	$23	100000	101000	100001
0 0 1 0 0 1 0 0	$24	000001	000100	000011
0 0 1 0 0 1 0 1	$25	000011	000110	000011
0 0 1 0 0 1 1 0	$26	010001	010100	100001
0 0 1 0 0 1 1 1	$27	100001	100100	100001
0 0 1 0 1 0 0 0	$28	000100	001000	000011
0 0 1 0 1 0 0 1	$29	000110	001010	000011
0 0 1 0 1 0 1 0	$2A	010100	011000	100001
0 0 1 0 1 0 1 1	$2B	100100	101000	100001
0 0 1 0 1 1 0 0	$2C	001000	000100	000011
0 0 1 0 1 1 0 1	$2D	001010	000110	000011
0 0 1 0 1 1 1 0	$2E	011000	010100	100001
0 0 1 0 1 1 1 1	$2F	101000	100100	100001

APPLICATION CIRCUIT

1. ±2.5V SPLIT POWER SUPPLY

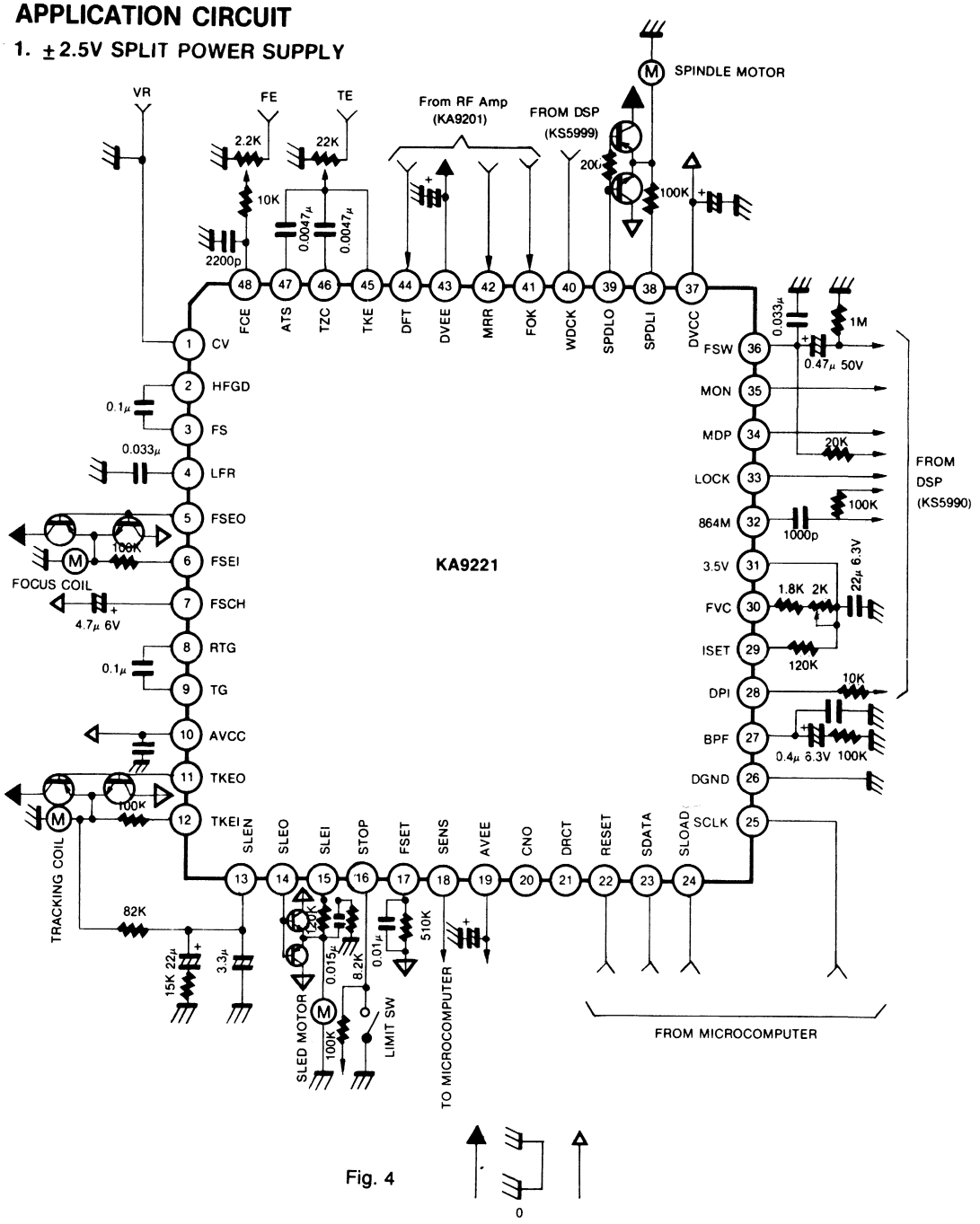


Fig. 4

2. +5V SINGLE POWER SUPPLY

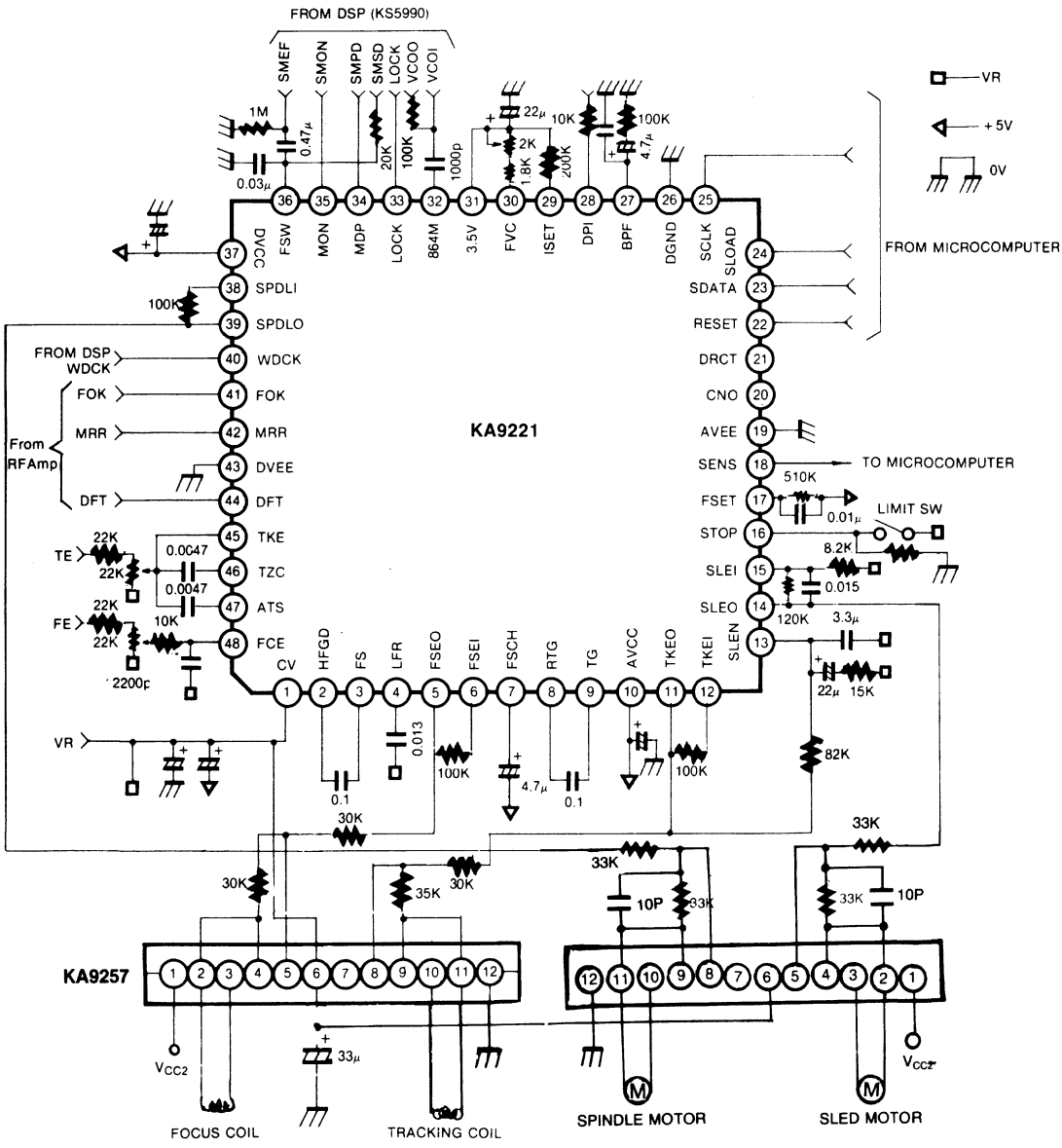
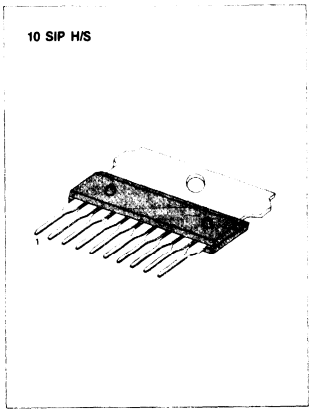


Fig. 5

DUAL POWER OPERATIONAL AMPLIFIER

The KA9256 is a dual power operational amplifier with an output maximum current of 1.0A ($V_S = \pm 15V$). It can be used as an arm driver for player, a driver for brush motors forward and reverse rotation control and an output driver for a hole motor.



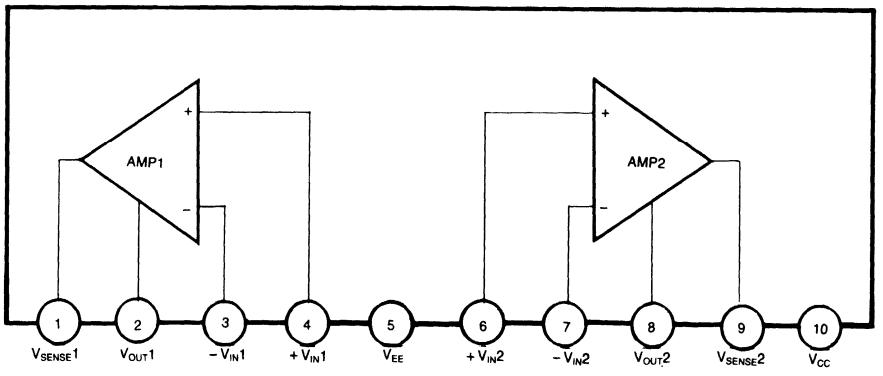
FEATURES

- Interal current limiting: $I_{SC} = 350mA$ ($R_{SC} = 2.2$)
- High output current: $I_O = 500mA$ max
- 10 SIP H/S package
- Internal phase compensation type

ORDERING INFORMATION

Device	Package	Operating Temperature
KA9256	10 SIP H/S	-25°C ~ +75°C

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	±8	V
Output Current	I_O	1.0	A
Power Dissipation	P_D	12.5	W
Operating Temperature Range	T_{OPR}	−25 ~ +75	°C
Storage Temperature Range	T_{STG}	−65 ~ +150	°C

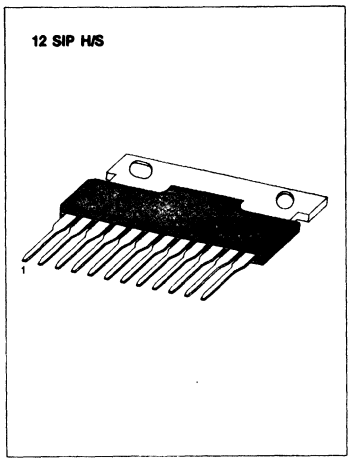
ELECTRICAL CHARACTERISTICS

(V_{CC} = +15V, V_{EE} = −15V, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}			2	6	mV
Input Offset Current	I_{IO}			10	200	nA
Input Bias Current	I_{BIAS}			100	700	nA
Supply Current	I_{CC}			10	20	mA
Output Voltage Swing	$V_{O(P-P)}$	$R_L = 33\Omega$	±12	±13		V
Large Signal Voltage Gain	A_V			100		dB
Input Voltage Range	V_I		±12	±14		V
Common Mode Rejection Ratio	CMRR		70	90		dB
Power Supply Rejection Ratio	PSRR			50	150	μV/V
Bandwidth	BW			1.0		MHz
Slew Rate	SR	$A_V = 1$, $R_L = 33\Omega$, $R = 10\Omega$, $C = 0.1\mu F$		0.15		V/μS
Limiting Current	I_{LIM}	$R_{SC} = 2.2\Omega$		0.35		A
Cross Talk	CT	$R_L = 33\Omega$, $V_O = 1V_{P-P}$		60		dB

DUAL POWER OPERATIONAL AMPLIFIER

The KA9257, a monolithic integrated circuit, is a dual power operational amplifier with a maximum output current of 0.5A. Since it consists of a balance transless, both forward and reverse operation of the motor can be achieved on a single power source. The device is suitable for a CD player.



FEATURES

- **2 channel BTL driver**
- **Low input bias (Iib = 30nA)**
- **Built in phase compensation capacitor**
- **Housed in a 12SIP H/S package for easy heat discharge**
- **Improved crosstalk: (CT = 80dB)**
- **High output current: (Io = 0.5A)**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA9257	12 SIP H/S	−25°C ~ +75°C

BLOCK DIAGRAM

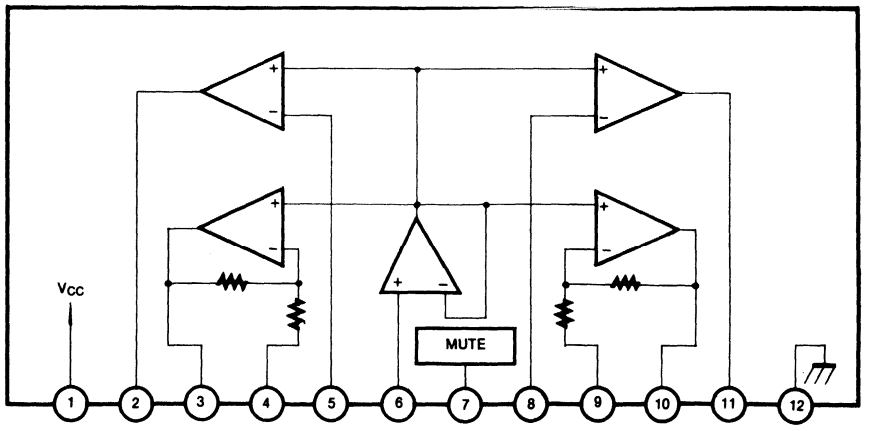


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	18	V
Power Dissipation	P_D	15	W
Operating Temperature	T_{OPR}	−25 ~ +75	°C
Storage Temperature	T_{STG}	−55 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 12V, f = 1KHz, R_L = 4ohm, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CCQ}	$V_I = 0$	—	3	10	mA
Input Bias Current	$I_{BIAS\ 1}$	$V_I = 0$	—	30	100	nA
Input Bias Pin Current	$I_{BIAS\ 2}$	$V_I = 0$	—	100	300	nA
Output Offset Voltage	V_{oo}	$V_I = 0$	−50	0	50	mV
Maximum Source Current	I_{SOURCE}	R_L = 4ohm, V_O = GND	0.7	1.4	—	A
Maximum Sink Current	I_{SINK}	R_L = ohm, $V_O = V_{CC}$	0.4	0.8	—	A
Maximum Output Voltage	$V_{O\ (MAX)}$	$V_I = 2V_{rms}$	1.8	2.5	—	V_{rms}
Closed Loop Voltage Gain	G_{VC}	$V_I = 0.1V_{rms}$	5.0	6.0	7.0	dB
Cut-off Frequency	f_T	V_I = 0.1rms, 3dB Down	15	20	—	KHz
Cross-Talk	CT	V_I = 0.1rms, BPF: 20-20KHz	40	80	—	dB
Ripple Rejection Ratio	RR	$V_{RR} = 0.1V_{rms}$ F_{RR} = 120Hz	30	40	—	dB
Slew-Rate	SR	$V_I = 0.3V_{PP}$ squarwave	—	0.3	—	V/μS

TEST CIRCUIT

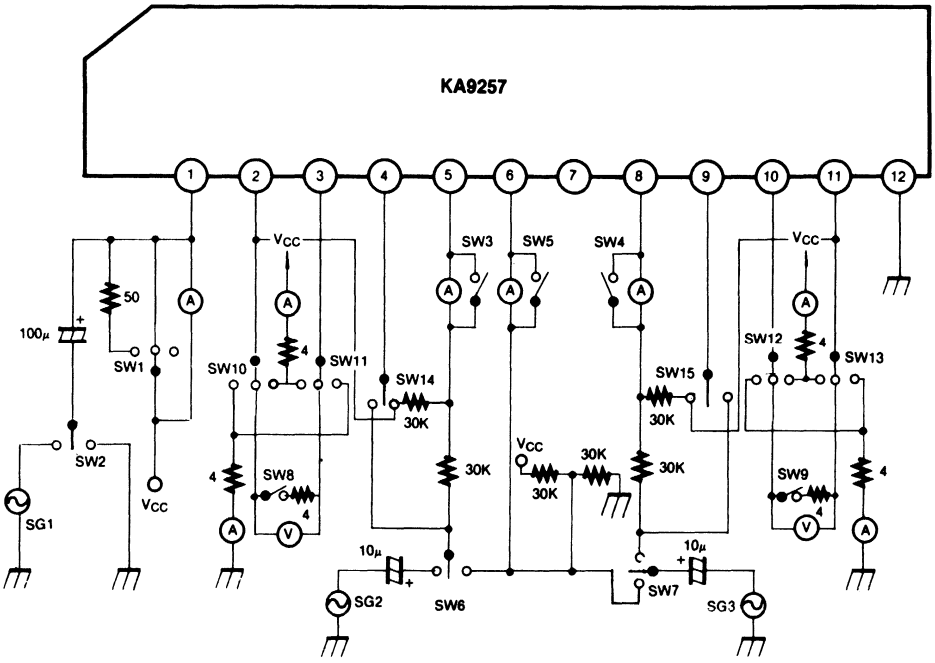


Fig. 2

APPLICATION CIRCUIT

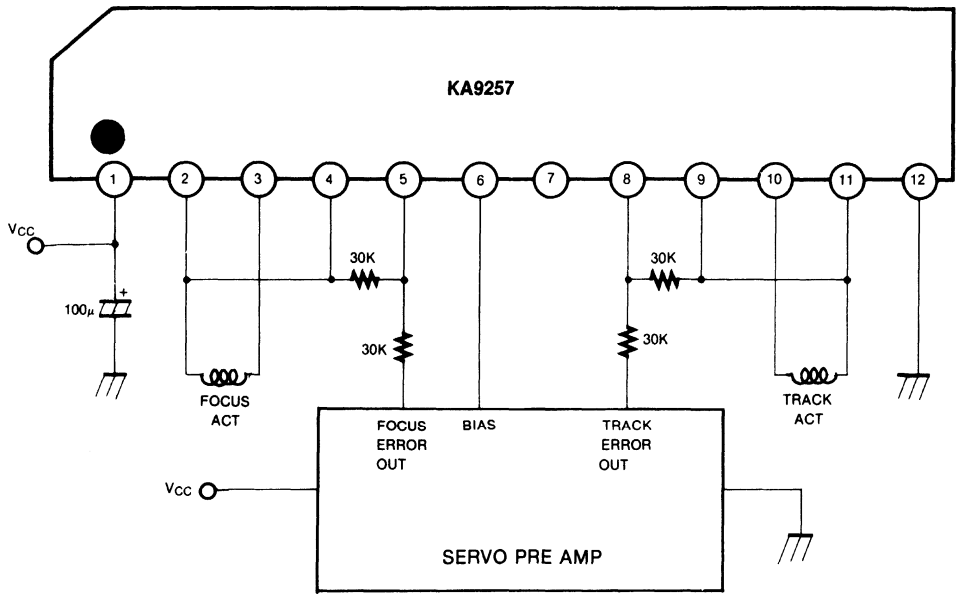


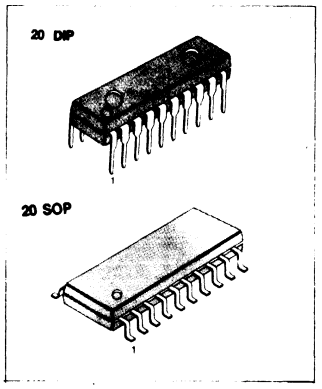
Fig. 3

Precautions

1. In designing the board, a minimum of 6cms of segregation should be allowed between the motor drive ICs (KA9257, KA9256) and other components such as the Micom and/or Recorder/Player ICs.
2. To get a stable supply of voltage and radiation shield effect, the CD Deck needs to be grounded.

DUAL CHANNEL AUDIO FILTER FOR CDP

The KA9270 is a monolithic integrated circuit designed for audio filter. It is used in compact disc player, digital audio tape recorder, etc.



FEATURES

- **Functions:** *Buffer for impedance matching
  *Low pass filter
  *De-emphasis control
  *Mute control
  *Reference voltage circuit (½ V_{CC} AMP)
- **Gain adjustable of audio output**
- **Minimum number of external parts required**
- **Recommend operation supply voltage range: 5.0 ~ 12.0V**
- **Package type: 20 DIP**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA9270	20DIP	-20°C ~ +75°C
KA9270D	20 SOP	

BLOCK DIAGRAM

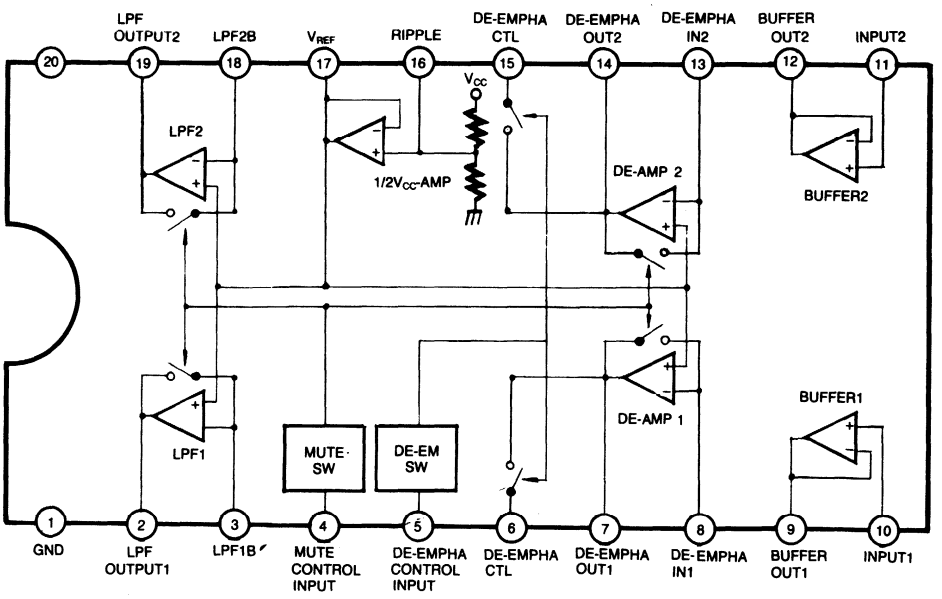


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Power Dissipation	P_D	550	μW
Operating Temperature	T_{OPR}	−20 ~ +75	°C
Storage Temperature	T_{STG}	−45 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 8V, f = 1KHz, R_L = 10KΩ, De-emphasis; off, Mute; off, S1 & S2; off, unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}	V_I = 0		1	4	6	mA
Maximum Output Voltage	V_{OM}	THD = 1%		1.8	2.1		Vrms
Total Harmonic Distortion	THD	V_O = 0dBm	f = 100Hz		0.01	0.05	%
			f = 1KHz		0.01	0.05	
			f = 10KHz		0.05	0.1	
			f = 16KHz		0.1	0.2	
			f = 20KHz		0.1	0.2	
Frequency Characteristics	f_V	V_O = 6dBm	f = 100Hz	−0.1	0	0.1	dB
			f = 1KHz	0	0	0	
			f = 10KHz	−0.5	0	0.5	
			f = 16KHz	−1.0	0	1.0	
			f = 120KHz	−1.5	0	1.5	
Cross Talk	CT	V_O = 0dBm	f = 100Hz	70	80		dB
			f = 1KHz	65	75		
			f = 10KHz	60	65		
Signal to Noise Ratio	S/N	V_O = 0dBm, R_G = 600Ω 20KHz LPF		73	80		dB
Channel Balance	CB	V_O = 0dBm		−1.0	0	1.0	dB
Open Loop Gain	G_{VO}	V_I = 900mVrms		−2.6	−0.6	1.0	dB
Gain Adjusting Range	G_{VR}	V_I = 900mV, S1, S2; ON		4.5	6		dB
Mute Attenuation Ratio	ATT_{MUTE}	V_I = 900mV, Mute SW; ON		40	50		dB
De-emphasis	DE_{EMPH}	De-emphasis: ON	f = 1K	−0.87	−0.37	0.13	dB
			f = 5K	−6.03	−4.53	−3.03	
			f = 16K	−10.53	−9.03	−7.53	

* Note: De-emphasis input conditions: V_O = 0dBm
De-emphasis off position

TEST CIRCUIT

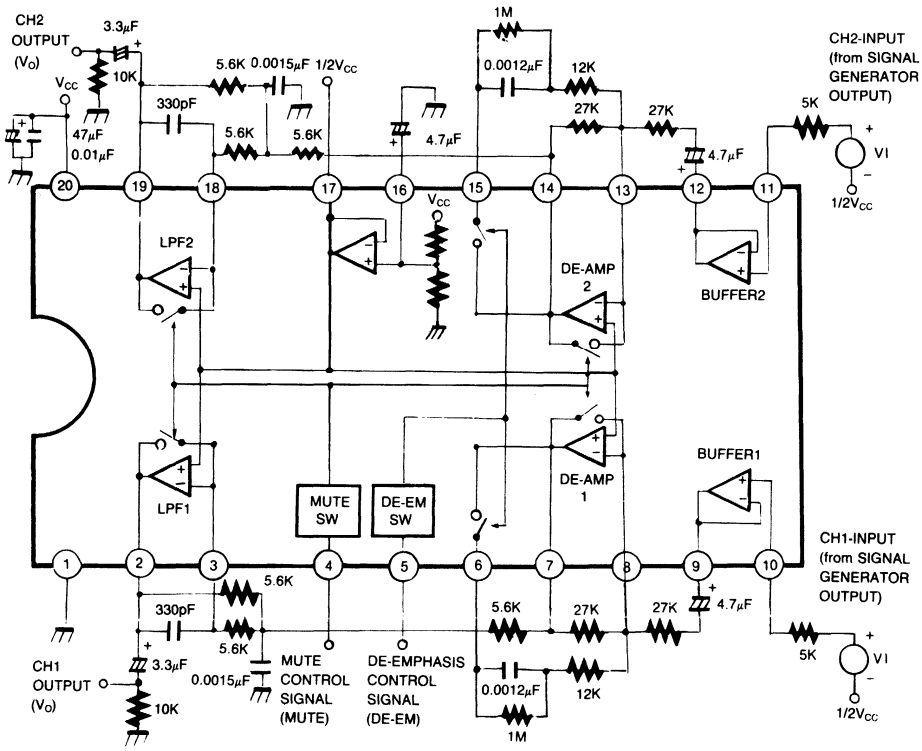


Fig. 2

APPLICATION INFORMATION

1. BUFFER

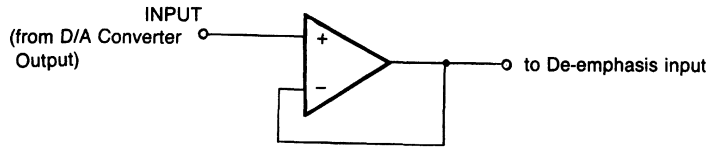


Fig. 3

It is used for impedance matching, between D/A converter output and de-emphasis input.

2. DE-EMPHASIS

a) De-emphasis operation condition

Control Input	De-emphasis Operation
High	ON
Low	OFF

b) De-emphasis characteristic at the de-emphasis ON

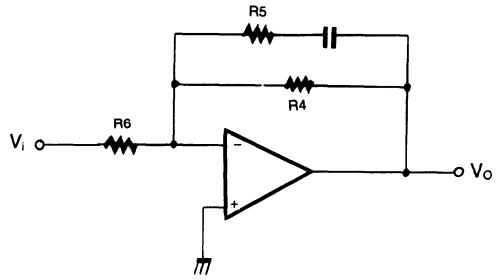


Fig. 4 Equivalent Circuit of De-emphasis ON Mode

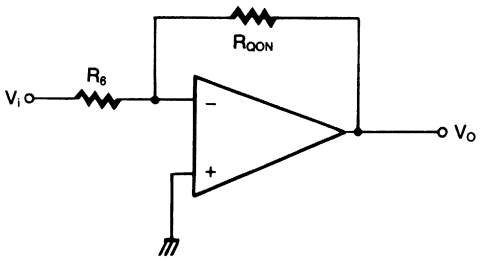
$Av \fallingdotseq R_4 / R_6$

$T_1 = C_1 (R_4 + R_5)$

$T_2 = C_1 \cdot R_5$

The de-emphasis characteristics is dependent on the external parts value.

3. MUTE



*Where:
R_{QON} = internal TR ON resistance

Fig. 5 Equivalent Circuit of Mute Switch ON Mode

Mute attenuation [M (att)] ratio is as follow;

$$M(att) = 20 \log \frac{V_O}{V_i}$$

$$= 20 \log \frac{R_{QON}}{R_6} (dB)$$

4. LOW PASS FILTER

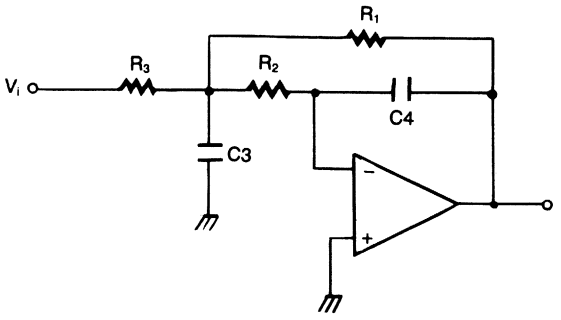


Fig. 6 Equivalent Circuit of LPF

Cutt off frequency (F_C) is as follow:

$$f_C = \frac{1}{2\pi \sqrt{R_2 R_1 C_3 C_4}} (Hz)$$

APPLICATION CIRCUIT

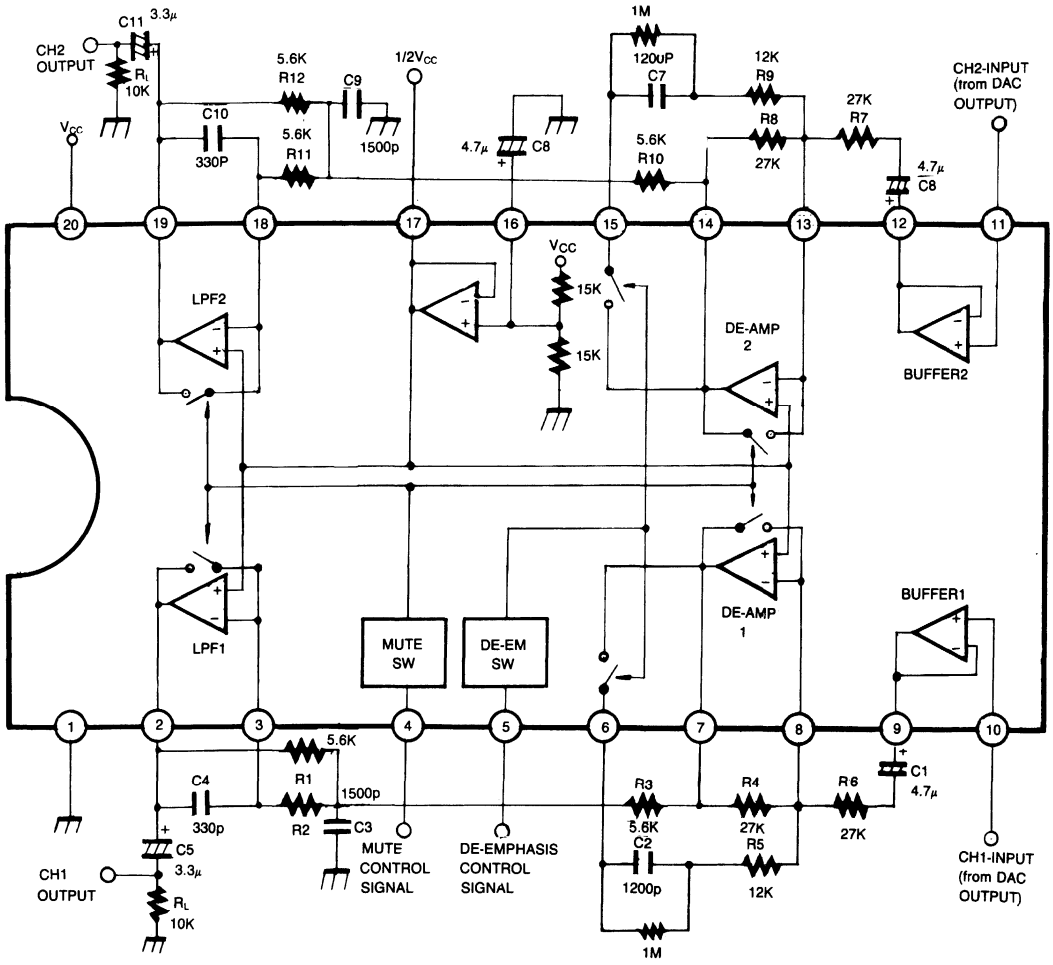
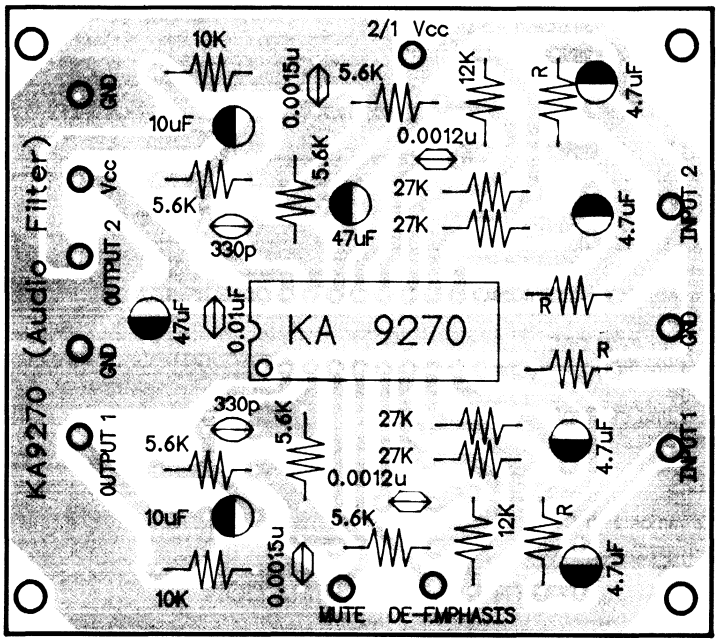


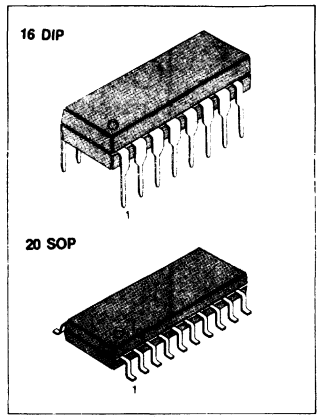
Fig. 7


KA9270 (Audio Filter)
KA 9270
2/1 Vcc
GND
Vcc
OUTPUT 2
OUTPUT 1
INPUT 2
INPUT 1
MUTE
DE-EMPHASIS
10K
10uF
0.0015u
5.6K
0.0012u
12K
4.7uF
27K
330p
47uF
0.01uF

(PCB PATTERN)

16-BIT D/A CONVERTER FOR CDPs

The KDA0316 is a CMOS, 16-bit digital-to-analog converter for compact disc players that uses a dynamic level shift conversion method, combining R-string, Pulse Width Modulation and level shift.



FEATURES

- **2's complement serial data input**
- **Contains two-channel D/A converter**
- **Can output L out and R out in phase**
- **To 176.4kHz maximum sampling frequency (corresponding to four oversampling)**
- **No deglich circuit needed**
- **Si-gate CMOS process (low power consumption)**
- **Single 5V supply voltage**
- **Built-in test circuit for PWM DAC**
- **Output swing level can be adjusted by the V_R input voltage**
- **MSB first and LSB first mode of input digital audio data is available**

APPLICATIONS

- Portable cassette radios with CDP
- Home audio component systems
- Electronic keyboards
- Music centers
- Mini CDPs
- Car CDPs

ORDERING INFORMATION

Device	THD(Max)(%)	Package	Operating Temperature
KDA0316LN	0.05	20 DIP	−30°C ~ +75°C
KDA0316N	0.08		
KDA0316LD	0.05	20 SOP	
KDA0316D	0.08		

PIN CONFIGURATION

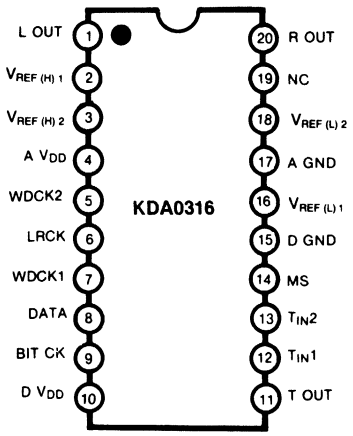


Fig. 1

PIN DESCRIPTION

Pin No	Symbol	Description
1	L OUT	Left channel output pin
2	$V_{REF\ (H)\ 1}$	Top reference voltage 1 pin
3	$V_{REF\ (H)\ 2}$	Top reference voltage 2 pin
4	A V_{DD}	Analog supply voltage pin
5	WDCK2	Word clock 2 input pin
6	LRCK	Left/right clock input pin
7	WDCK1	Word clock 1 input pin
8	DATA	Digital audio data input pin
9	BIT CK	Bit clock input pin
10	D V_{DD}	Digital supply voltage pin
11	T OUT	Test output pin
12	$T_{IN}1$	Test input pin
13	$T_{IN}2$	Test input pin
14	MS	Mode selecting pin
15	D GND	Digital ground pin
16	$V_{REF\ (L)\ 1}$	Bottom reference voltage 1 pin
17	A GND	Analog ground pin
18	$V_{REF\ (L)\ 2}$	Bottom reference voltage 2 pin
19	NC	No connection
20	R OUT	Right channel output pin

ABSOLUTE MAXIMUM RATINGS (Note 1 & 2)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{DD}	$-0.3 \sim +7.0$	V
Input Voltage	V_I	$-0.3 \sim V_{DD}+0.3$	V
Output Voltage	V_O	$-0.3 \sim V_{DD}+0.3$	V
Operating Temperature Range	V_{OPR}	$-30 \sim +75$	°C
Storage Temperature Range	V_{STG}	$-40 \sim +125$	°C
ESD Susceptibility (Note 3)	V_{ESD}	±900	V
Latch-up Current	I_{LATCH}	50	mA

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	4.5	5.0	5.5	V
Operating Temperature Range	T_{OPR}	−30		75	°C
Input High Voltage	V_{IH}	2.2		$V_{DD}+0.3$	V
Input Low Voltage	V_{IL}	−0.3		0.8	V
Reference High Voltage	$V_{REF\,(L)}$	$V_{DD}-0.5$		V_{DD}	V
Reference Low Voltage	$V_{REF\,(H)}$	0		0.5	V
Sampling Frequency	f_S			176.4	KHz

ELECTRICAL CHARACTERISTICS

(Converter Specifications: $V_{DD}=5V$, $V_{REF\,(H)}=5V$, $V_{REF\,(L)}=A\,GND$, IF = 0V, $f_S=176.4KHz$, Ta = 25°C., unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current	I_{CC}	$V_{DD}=5V$		3.5	5.5	mA
		$V_{DD}=5.5V$		4.0	7.0	
Total Harmonic Distortion	THD	MS = 0V or 5V Data = 1KHz, 0dB			0.05*1 0.08	%
		MS = 0V or 5V Data = 1KHz, −20dB			0.2	
Signal to Noise Ratio	S/N	Data = 1KHz, 0dB		92		dB
		$V_{DD}=4.5V$ Data = 1KHz, 0dB		87		
		MS = 5V Data = 1KHz, 0dB		92		
		MS = 5V, $V_{DD}=4.5V$ Data = 1KHz, 0dB		87		
Crosstalk	CT	Data = 1KHz, 0dB		−85		dB

*1: User's option value (KDA016LN, KDA0316LD)

Note 1: ABSOLUTE MAXIMUM RATINGS are those values beyond which the life of the device may be impaired. Normal operation is not guaranteed at these extremes.

Note 2: All voltage is measured with respect to the GND, unless otherwise noted. The separate A GND point should always be wired to the D GND.

Note 3: The 100pF is discharged through a 1.5KΩ resistor.

(2) V_{DD} and V_R power supply should be low impedance and high stable (for example, a three-terminal voltage

TEST CIRCUIT

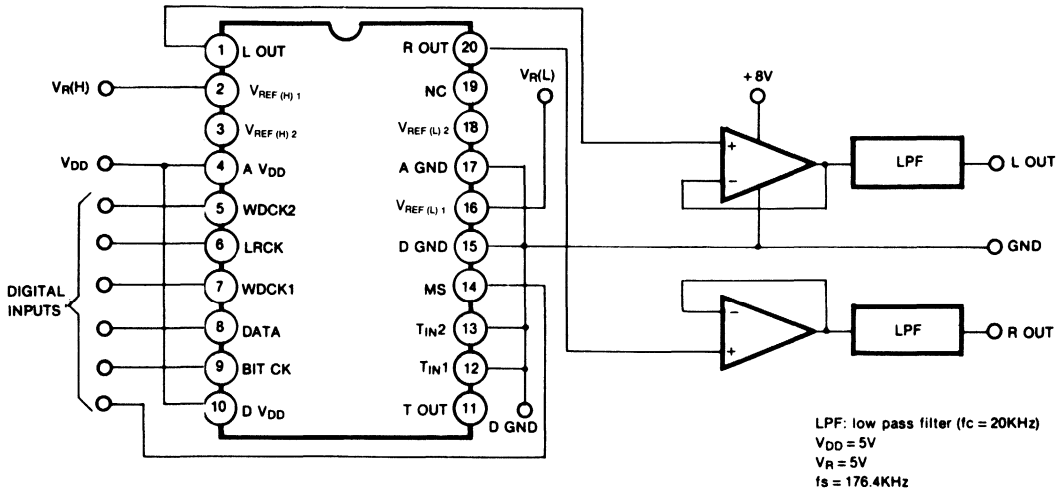
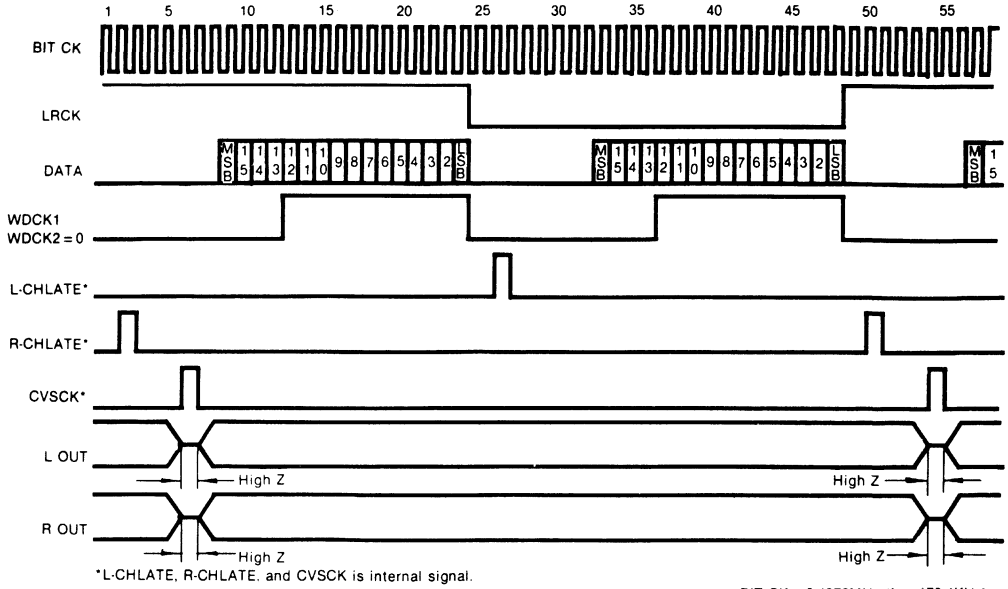


Fig. 2

APPLICATION INFORMATION

TIMING DIAGRAM 1 (When MS = "H")

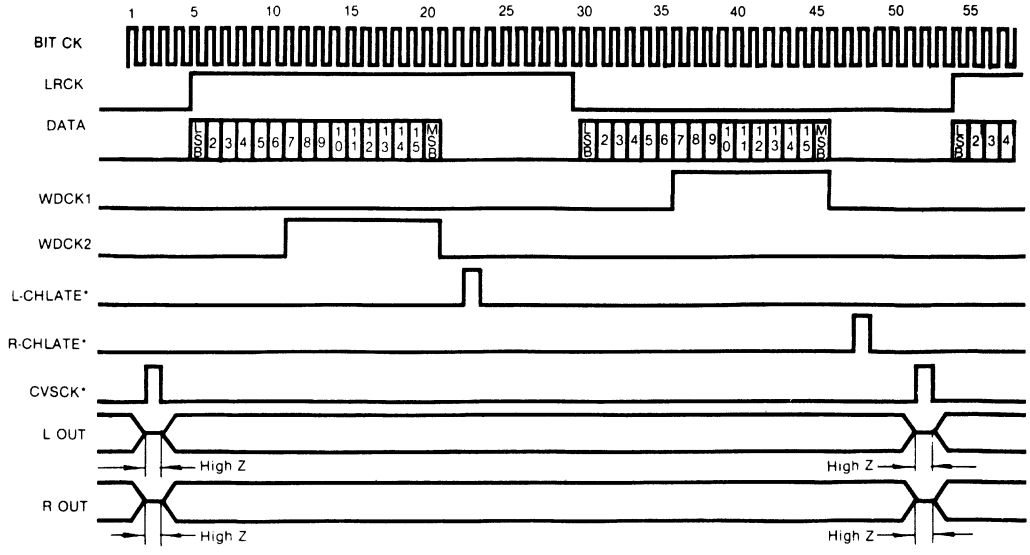


*L-CHLATE, R-CHLATE, and CVSCK is internal signal.

Fig. 3

BIT CK = 8.4672MHz (f_S = 176.4KHz)
4.2336MHz (f_S = 88.2KHz)
2.1168MHz (f_S = 44.1KHz)

TIMING DIAGRAM 2 (When MS = "L")



*L-CHLATE, R-CHLATE, and CVSCK is internal signal.

Fig. 4

BIT CK = 8.6436MHz (f_S = 176.4KHz)
4.3218MHz (f_S = 88.2KHz)
2.1609MHz (f_S = 44.1KHz)

APPLICATION CIRCUIT

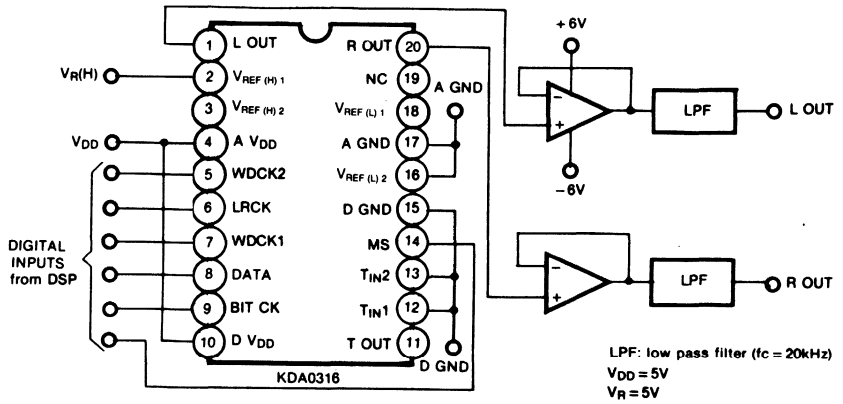


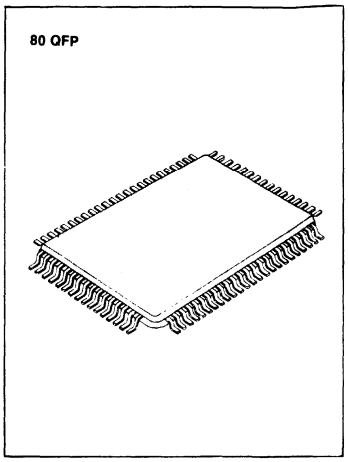
Fig. 5

Note: (1) D GND should be wired to the digital ground group and A GND to the analog ground group.
(2) V_{DD} and V_R power supply should be low impedance and high stable (for example, three-terminal voltage regulator).
(3) Because of the low output impedance and weak noise immunity of Pin 1 or Pin 20, noise reduction should be done by reducing the lead-wire length to the next OP amp stage.

4-BIT MICROCONTROLLER

KS56C820 is an SMCS56, core-based 4-bit CMOS Microcomputer with LCD drivers, various peripherals that allows a high level of control of target products, and numerous I/O's. The flexible I/O control commands that can handle 1, 4, and 8 bit data manipulations will allow diverse applications control.

KS56C820 has enough LCD drivers, and many CPU clock modes that minimizes current that it is suitable for applications on portable products like CDPs, DATs, cameras and LCD remote controllers.



FEATURES

- Memory Mapped I/O
- ROM: 8064 x 8 bits
- RAM: 512 x 4 bits
- One 8-bit timer/counter input source: 2 external, and 4 internal inputs
- Watch timer
- One 8-bit SIO
  - Can send either from LSB or MSB.
  - Can choose either transmit and receive, or receive only modes
- Multiple vector interrupts
  - Three external source interrupts: INT0, INT1, INT4
  - Three internal source interrupts: Basic Timer, Timer/counter, SIO
  - One external edge detectable quasi-interrupt: INT2
  - One quasi-interrupt for clock: INTW
- 32 I/O bits (max 40 I/O bits)
  - Inputs: 8 bits
  - I/O: 16 bits; built-in LED driver.
  - N-channel open drain I/O: 8 bitgs; can handle up to 10 volts.
  - Output: Maximum 8 bits (including segment driver output)
- Max. 16 digits of LCD driver
  - Static, 1/2, 1/3, 1/4 duty selectable.
  - 24, 28, 32 segment output selectable.
- 2KHz output for buzzer
- 16-bit Bit Sequential Carrier useful for remote controller.
- Two types of power-down modes
  - Idle: Only the CPU clock stops.
  - Stop: All internal clocks stop.
- Can choose from various instruction cycle times for power saving.
  - Using Main-system clock: 1, 2, 16μS/4MHz
  - Using Sub-system clock: 122μS/32.768KHz
- Built-in crystal/ceramic oscillator circuits for clock.
  - Crystal/ceramic oscillator circuit for main-system clock.
  - Crystal oscillator circuit for sub-system clock.
- 3/5V single power supply
- 80 Plastic Quad Flat Package

PIN CONFIGURATION

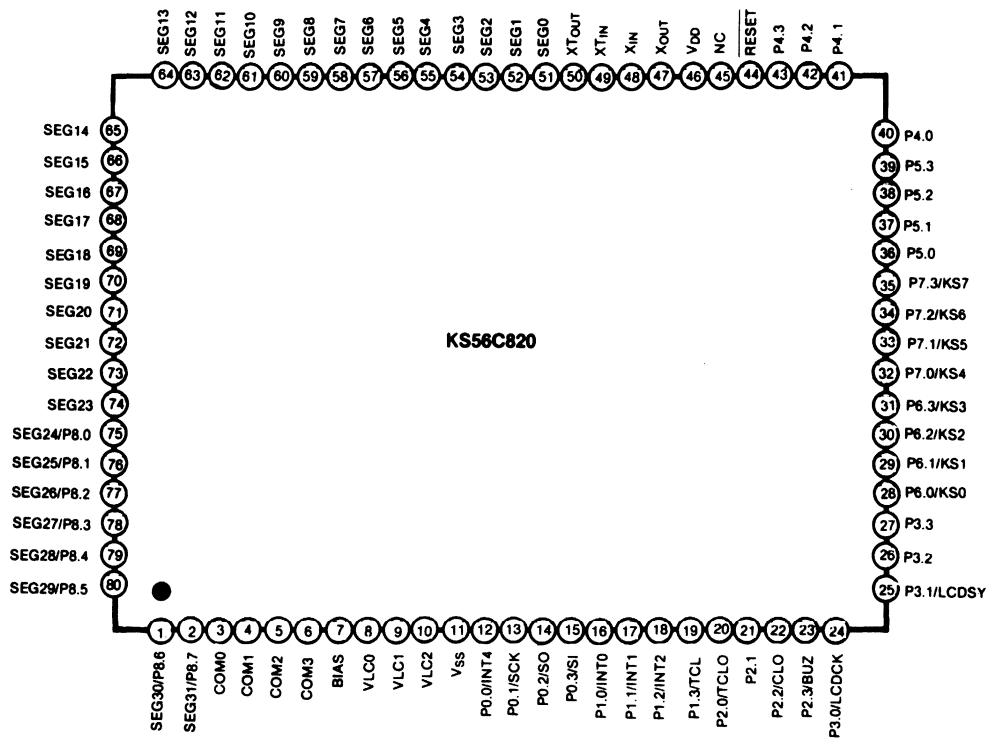


Fig. 1

PIN DESCRIPTION

Symbol	Description	
P1.0-P1.3	4-bit Input	Internal pull-up resistor can be specified in 4-bit unit by software
P2, P7	4-bit Input/Output	
P3, P6	I/O mode selectable in 1-bit unit by software	
P4, P5	4-bit input/output, N-ch open drain	
P8.0-P8.7	Outputs in 1-bit unit (shared with segment outputs)	
SEG0-SEG23	Segment output for LCD display	
SEG24-SEG31	Segment output for LCD display (shared with Port 8)	
COM0-COM3	Common signal output for LCD display	
VLC0-VLC2	LCD power supply pin	
BIAS	LCD power supply control pin for 3/5V operating	
LCDCK	LCD clock output for display expansion	
LCDSY	LCD sync. clock output for display expansion	
TCL	Timer/Counter external clock input	
TCLO	Timer/Counter clock output	
INT0, 1, 2, 4	External interrupt input	
CLO	Clock output	
BUZ	2KHz clock output for buzzer	
KS0-KS7	Semi-interrupt input detecting external falling edge	
SCK, SI, SO	SCK: serial clock, SI: serial input, SO: serial output	
X_{IN}, X_{OUT}	Crystal/Ceramic or RC clock I/O for Main-system clock	
XT_{IN}, XT_{OUT}	Crystal clock I/O for sub-system clock	

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Test Conditions		Value	Unit
Supply Voltage	V_{DD}			−0.3 ~ +7.0	V
Input Voltage	V_I			−0.3 ~ V_{DD} + 0.3	V
Output Voltage	V_O			−0.3 ~ V_{DD} + 0.3	V
High Output Current	I_{OH}	1 Port		−15	mA
		All Ports		−30	mA
Low Output Current	I_{OL}	1 Port	MAX.	30	mA
			TYP.	15	mA
		Port 2, Port 3	MAX.	100	mA
			TYP.	60	mA
		Port 6	MAX.	100	mA
			TYP.	60	mA
Operating Temperature	T_{OPR}			−20 ~ +75	°C
Storage Temperature	T_{STG}			−55 ~ +125	°C

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS (Ta = −40 ~ +85°C, V_{DD} = 4.0 ~ 6.0V)

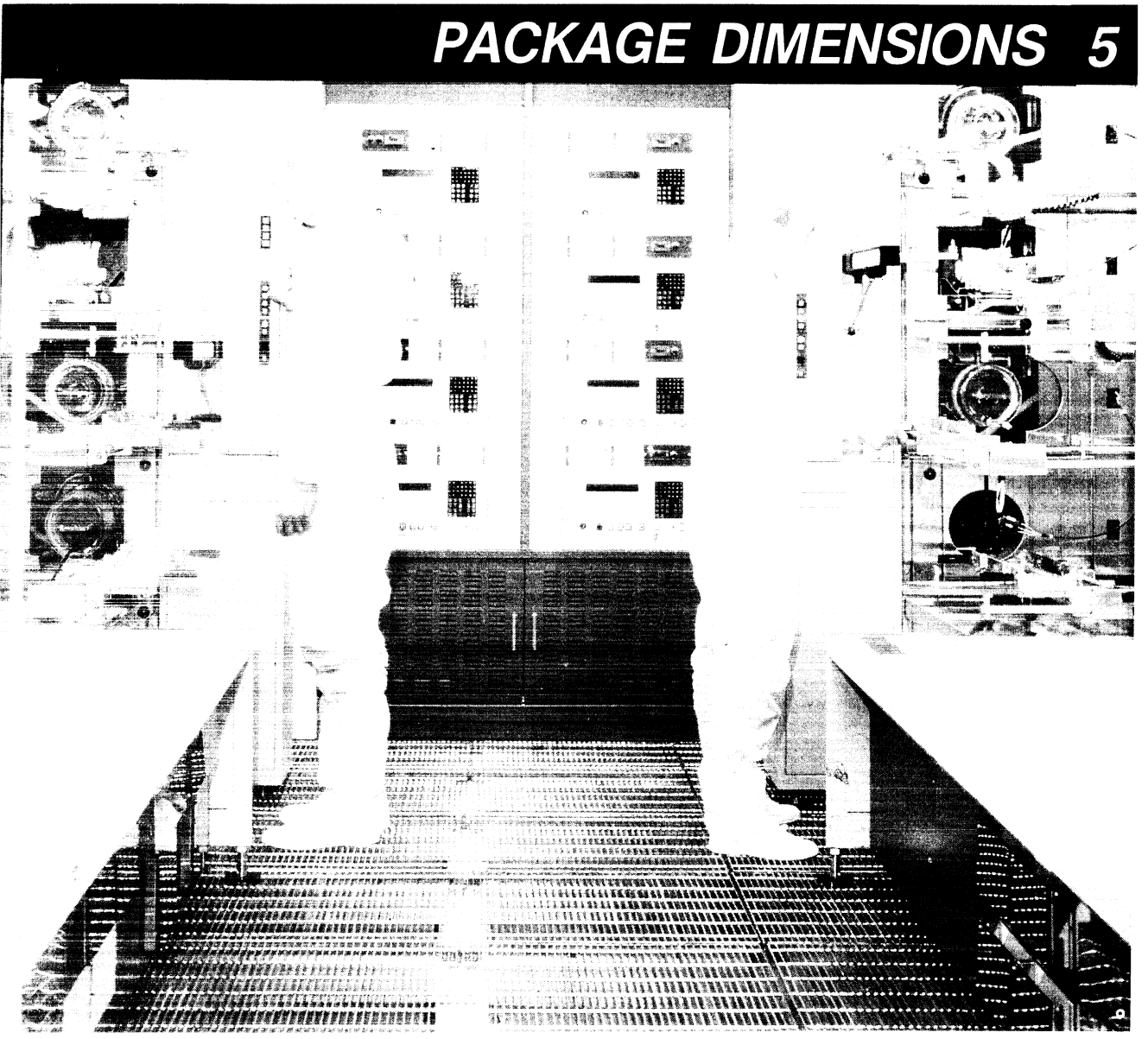
Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
High Input Voltage	V_{IH1}	Port 2, 3		0.7 V_{DD}		V_{DD}	V
	V_{IH2}	Port 1, 6, RESET		0.8 V_{DD}		V_{DD}	V
	V_{IH3}	Port 4, 5	built in pull up re-	0.7 V_{DD}		V_{DD}	V
			-sistor open drain	0.7 V_{DD}		10 V_{DD}	V
	V_{IH4}	X_{IN}, X_{OUT}, XT_{IN}		V_{DD} − 0.5		V_{DD}V	
Low Input Voltage	V_{IL1}	Port 2, 3		0		0.3 V_{DD}	V
	V_{IL2}	Port 1, 6, RESET		0		0.2 V_{DD}	V
	V_{IL3}	X_{IN}, X_{OUT}, XT_{IN}		0		0.4	V
High Output Voltage	V_{OH1}	Port 2, 3, 6, BIAS	I_{OH} = − 1mA	V_{DD} − 1.0			V
			I_{OH} = − 100μA	V_{DD} − 0.5			V
	V_{OH2}	P8.0-7	I_{OH} = − 100μA	V_{DD} − 2.0			V
			I_{OH} = − 30μA	V_{DD} − 1.0			V
Low Output Voltage	V_{OL1}	Port 2, 3, 6, BIAS	I_{OL} = 15mA		0.4	2.0	V
			I_{OL} = 1.6mA			0.4	V
			I_{OL} = 400μA			0.5	V
	V_{OL2}	P8.0-7	I_{OL} = 100μA			1.0	V
			I_{OL} = 50μA			1.0	V
Supply Current	I_{DD1}	4.19MHz	V_{DD} = 5V + 10%		2.5	8	mA
			V_{DD} = 3V + 10%		0.35	1.2	mA
	I_{DD2}		IDLE V_{DD} = 5V		500	1500	μA
			IDLE V_{DD} = 3V		150	450	μA
	I_{DD3}	32.768 KHz	V_{DD} = 3V + 10%		30	90	μA
	I_{DD4}		IDLE V_{DD} = 3V		5	15	μA

AC CHARACTERISTICS (Ta = −40 ~ +85°C, V_{DD} = 4.0 ~ 6.0V)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Cycle Time	t_{CY}	Main-system Clock	0.95		64	μS
		Sub-system Clock	114	122	125	μS
TCL Input Frequency	$f_{I(TCL)}$	V_{DD} = 4.5 ~ 6.0V	0		1	MHz
			0		275	KHz
TCL Input High & Low Level Width	$t_{WIH}/t_{WIL\ 1}$	V_{DD} = 4.5 ~ 6.0V	0.48			μS
			1.8			μS
Ext. Interrupt High & Low Level Width	$t_{WIH}/t_{WIL\ 2}$					μS
		INT1, INT2	10			μS
		KS0 − KS3	10			μS
RESET Low Level Width	$t_{WL(RST)}$		10			μS

NOTES

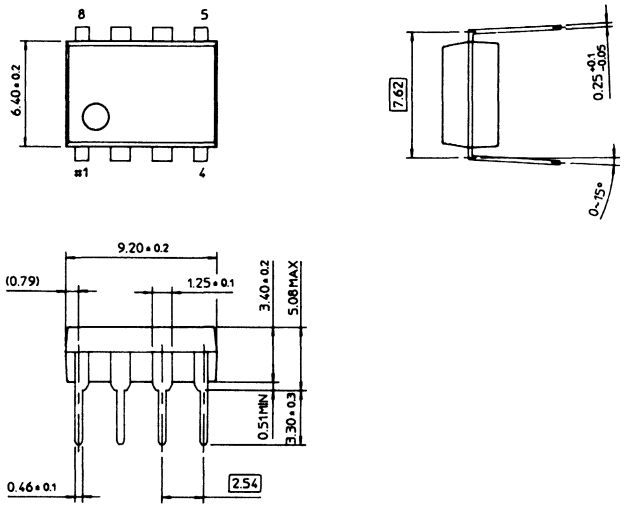
PACKAGE DIMENSIONS 5



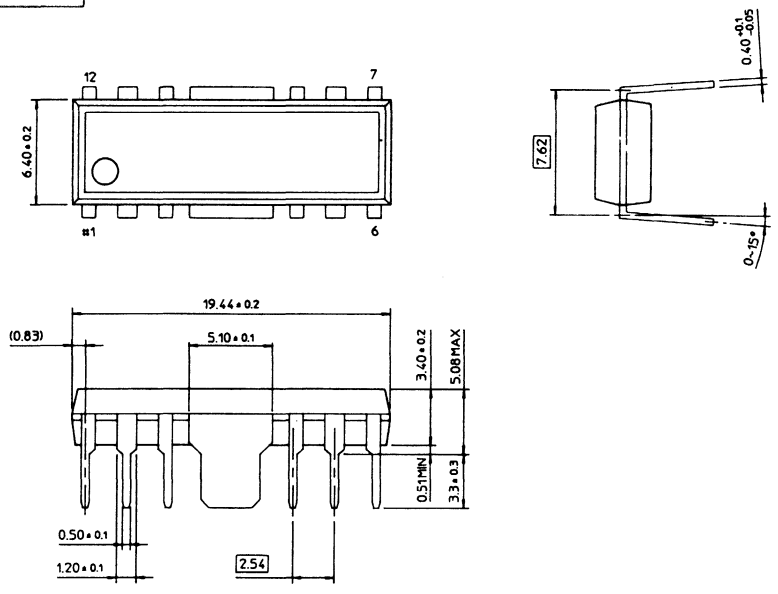
PACKAGE DIMENSIONS

Dimensions in Milimeters

8-DIP-300



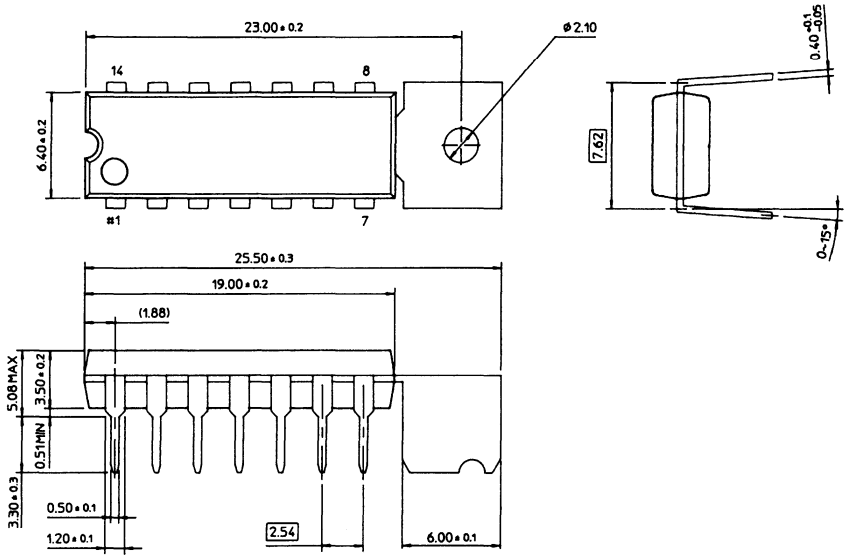
12-DIPH-300



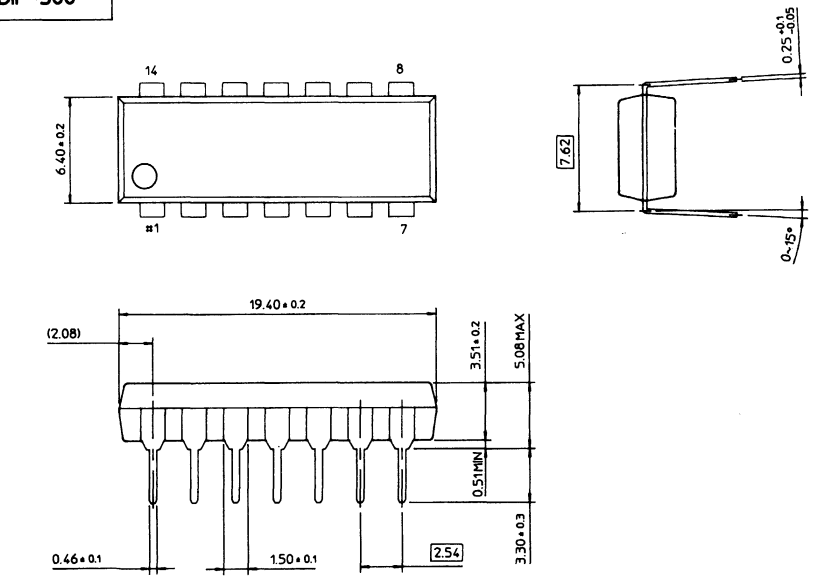
PACKAGE DIMENSIONS

Dimensions in Milimeters

14-DIPH-300



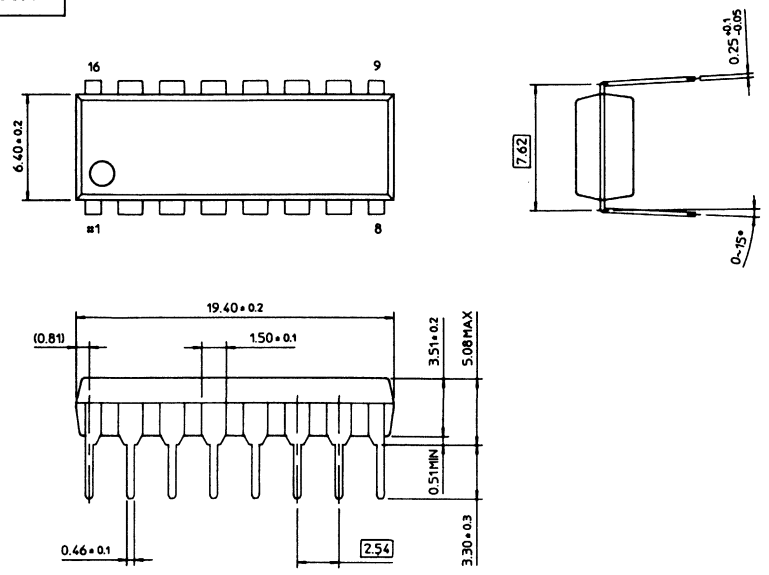
14-DIP-300



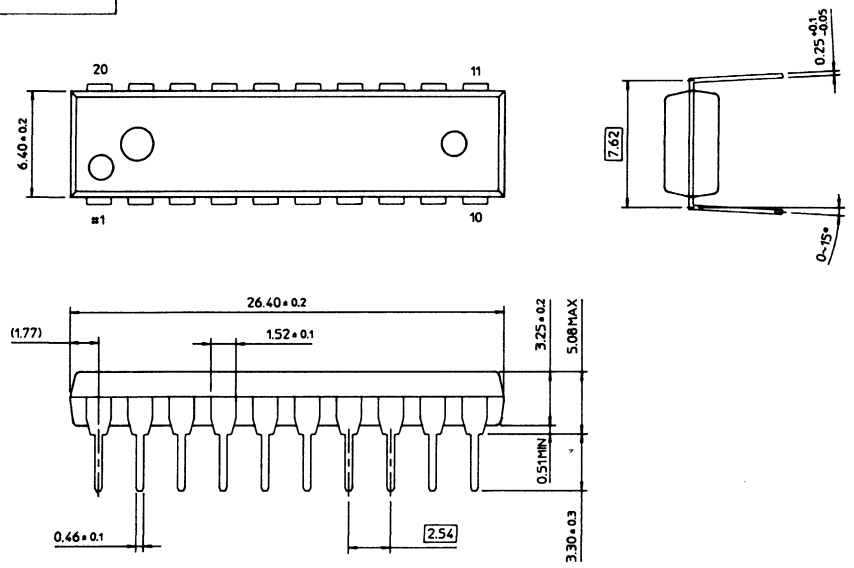
PACKAGE DIMENSIONS

Dimensions in Milimeters

16-DIP-300A



20-DIP-300A



PACKAGE DIMENSIONS

Dimensions in Milimeters

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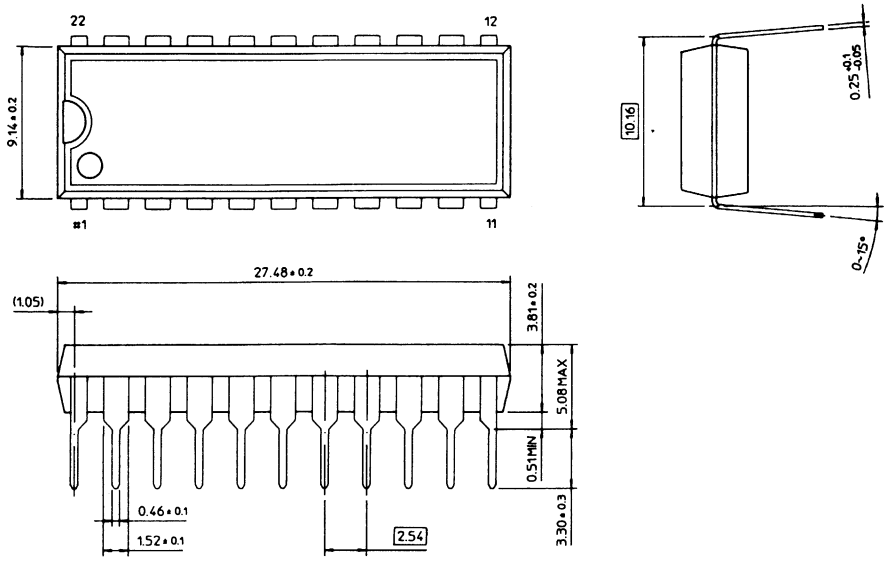

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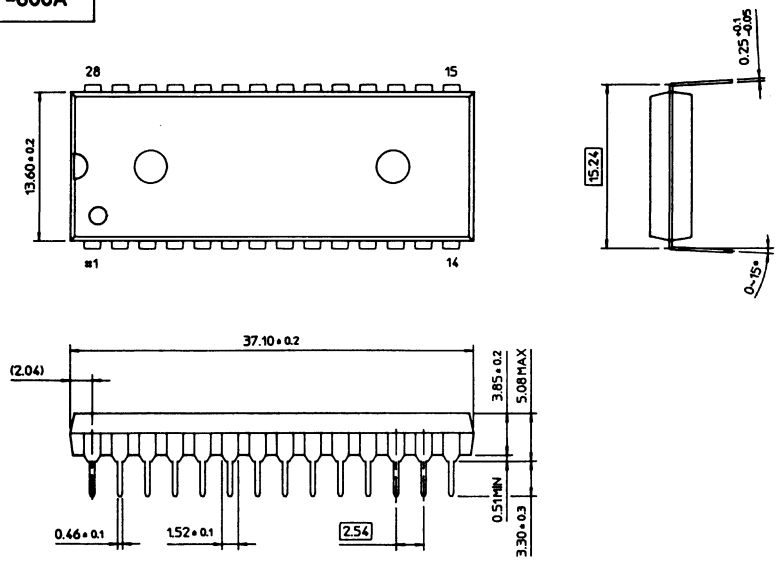
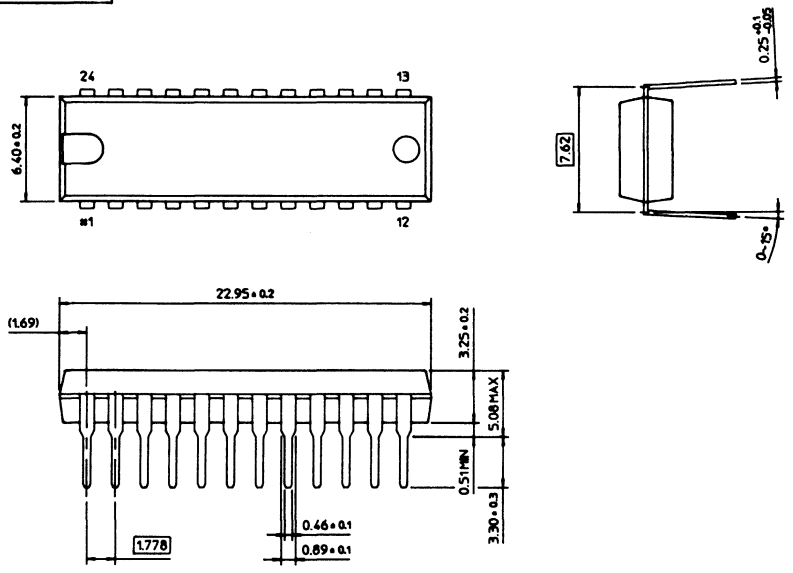


PACKAGE DIMENSIONS

Dimensions in Milimeters

24-SDIP-300



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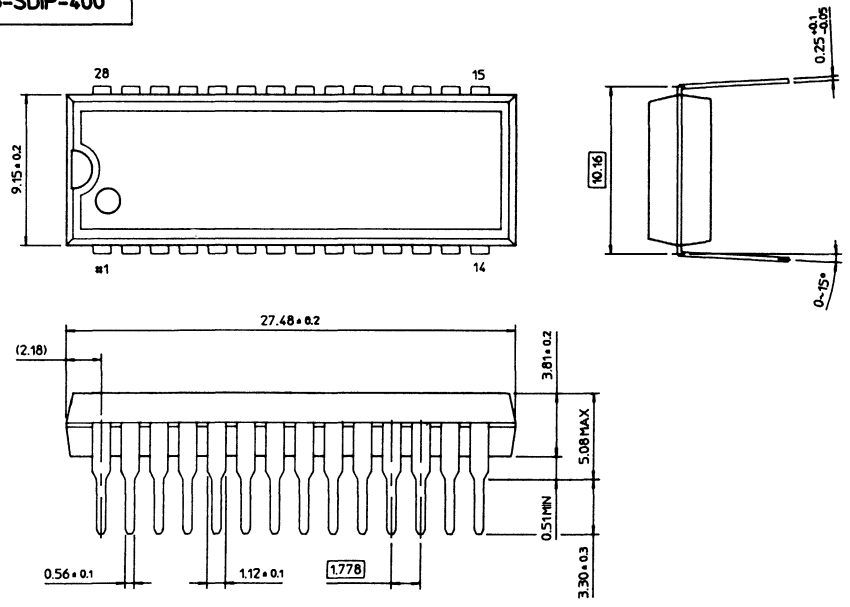
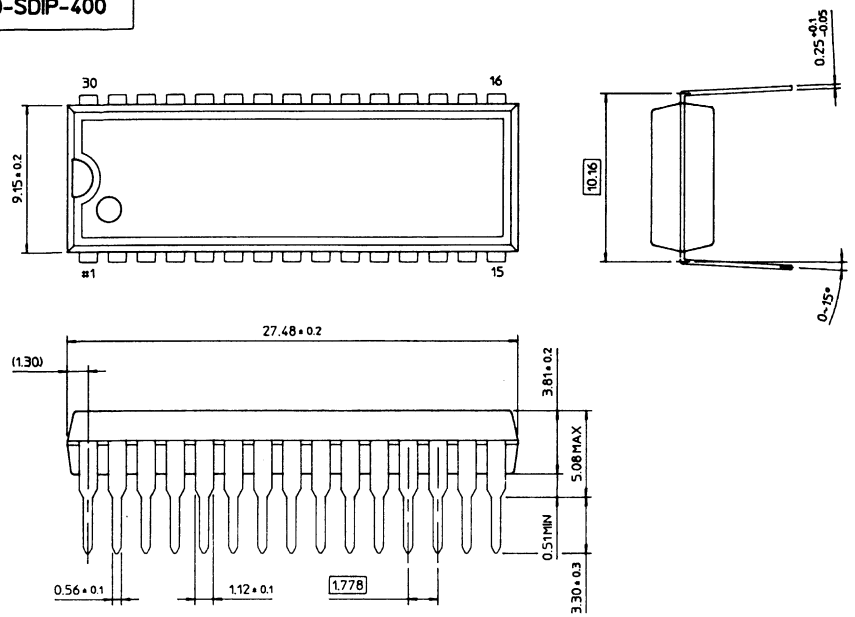


PACKAGE DIMENSIONS

Dimensions in Milimeters

30-SDIP-400



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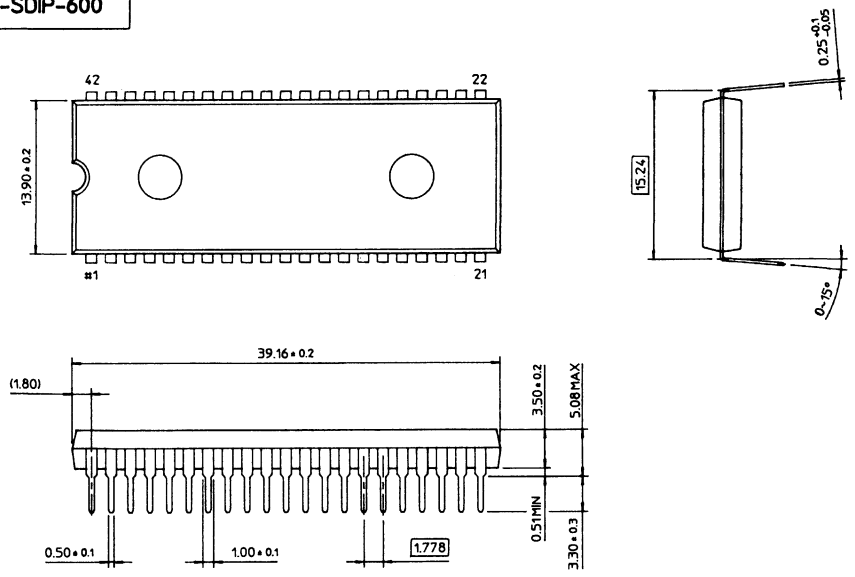
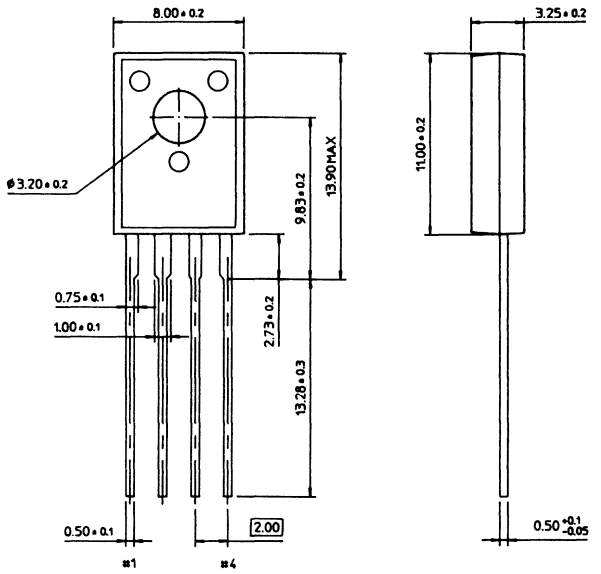


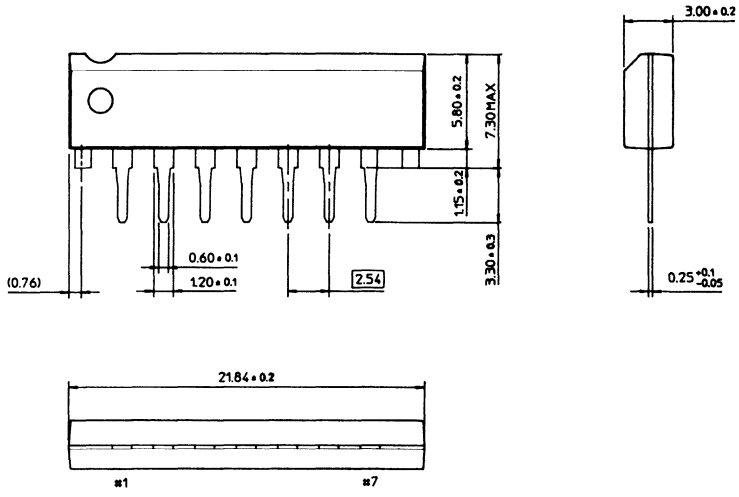
PACKAGE DIMENSIONS

Dimensions in Milimeters

4-SIP



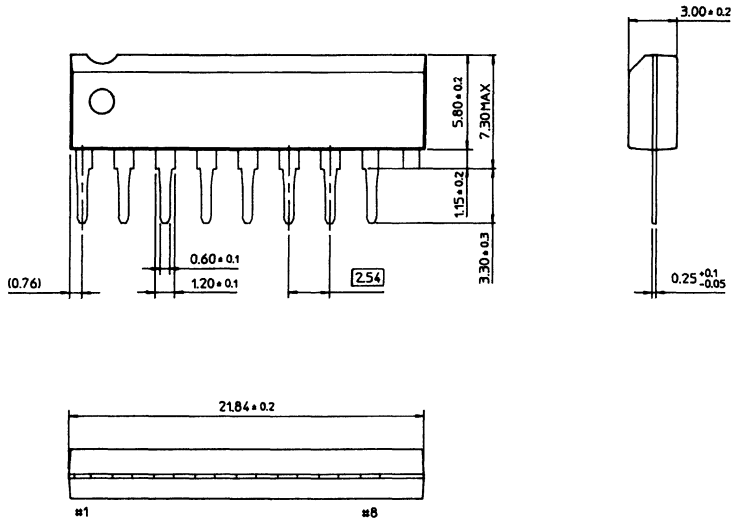
7-SIP



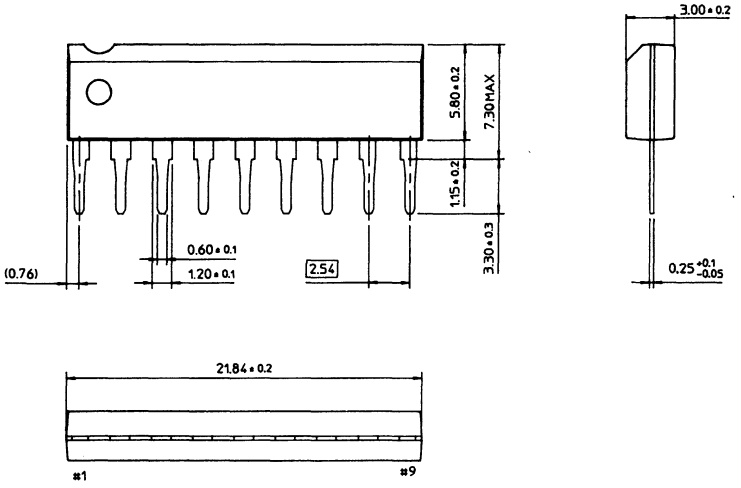
PACKAGE DIMENSIONS

Dimensions in Milimeters

8-SIP



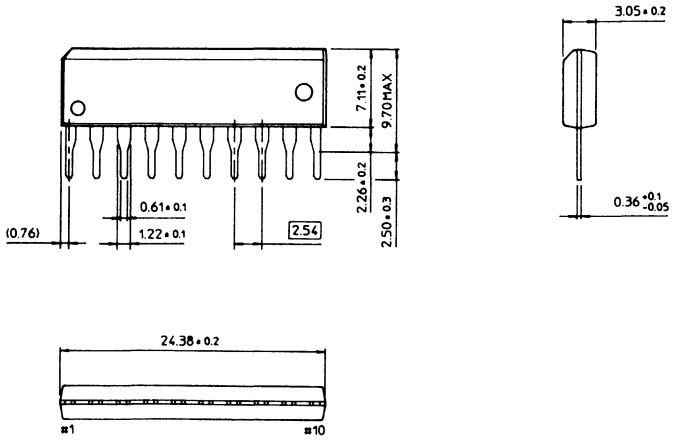
9-SIP



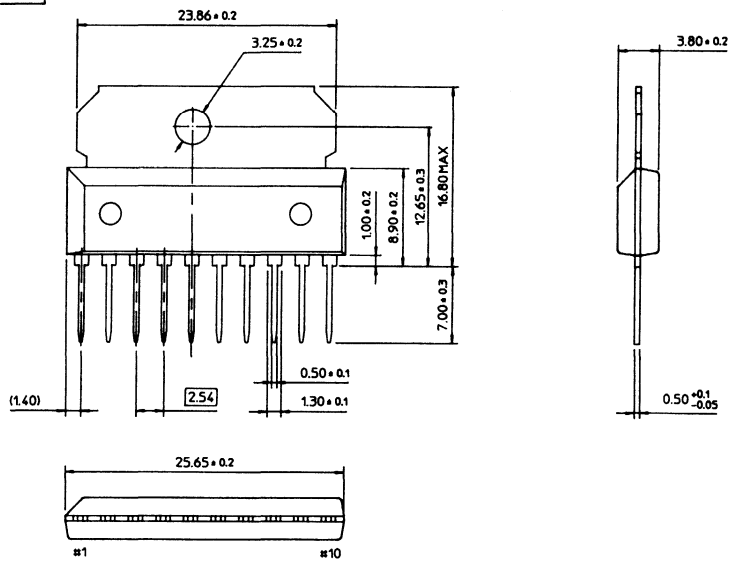
PACKAGE DIMENSIONS

Dimensions in Milimeters

10-SIP



10-SIPH-A



PACKAGE DIMENSIONS

Dimensions in Milimeters

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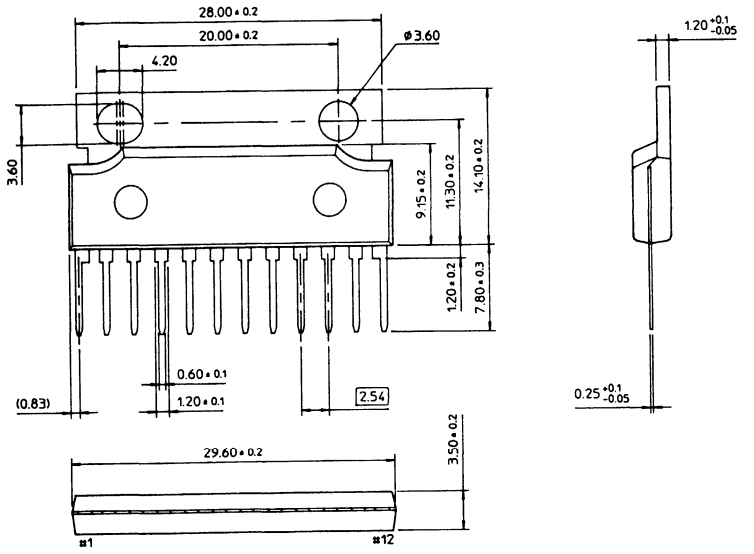

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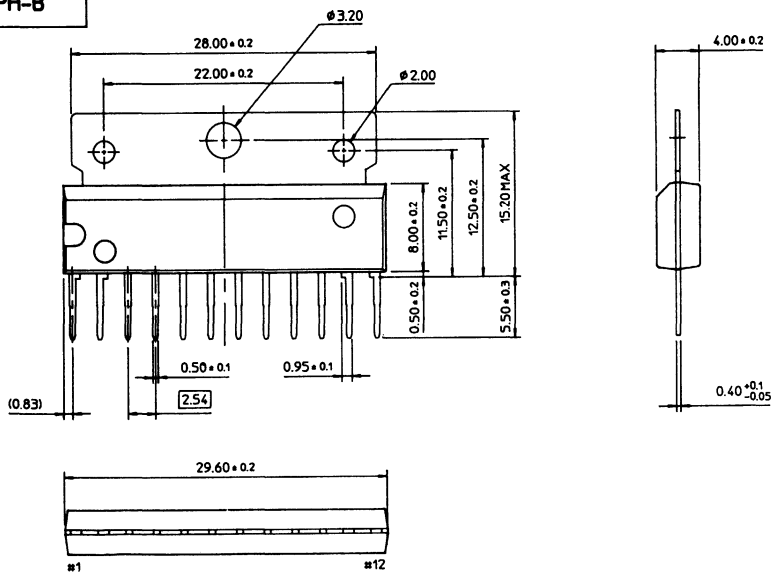

PACKAGE DIMENSIONS

Dimensions in Milimeters

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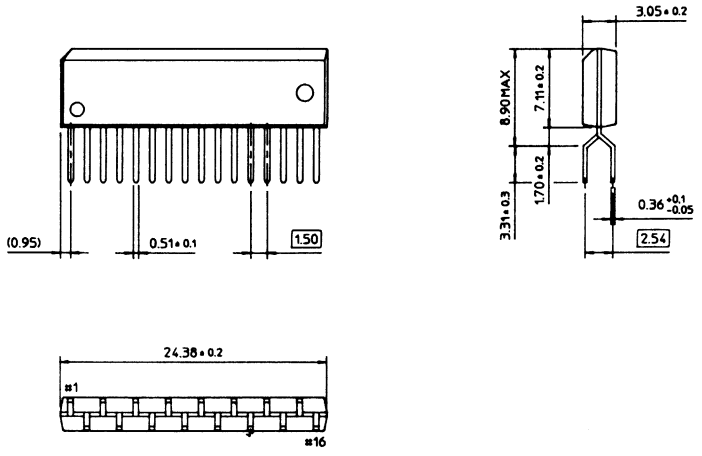

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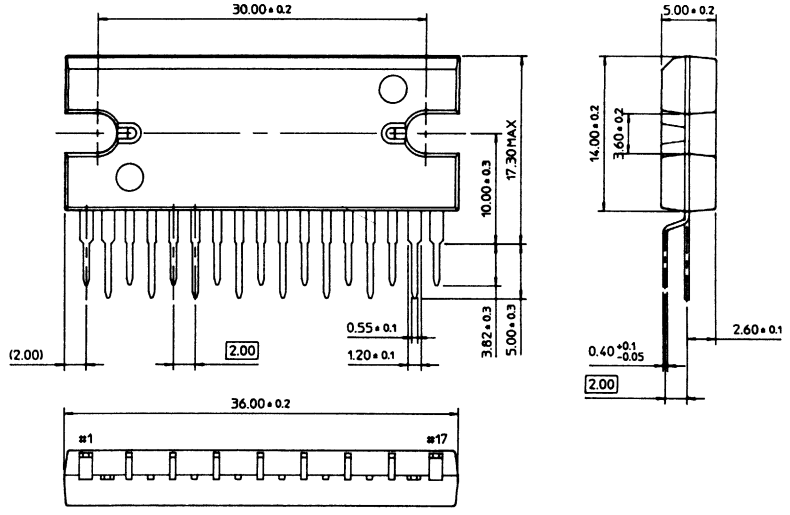

PACKAGE DIMENSIONS

Dimensions in Milimeters

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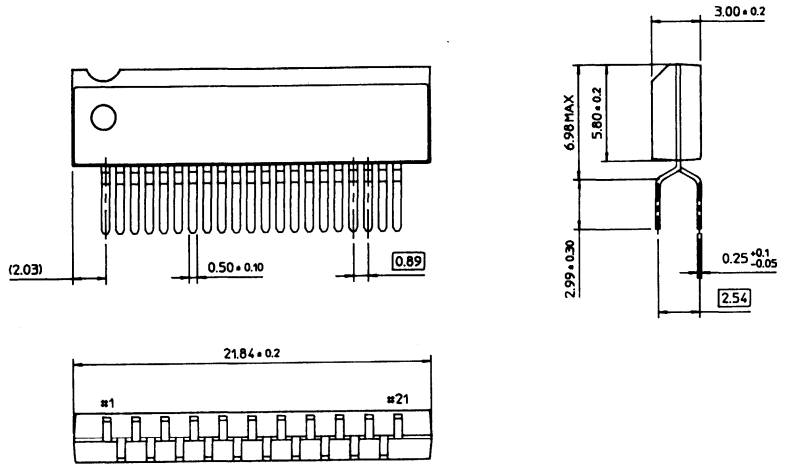

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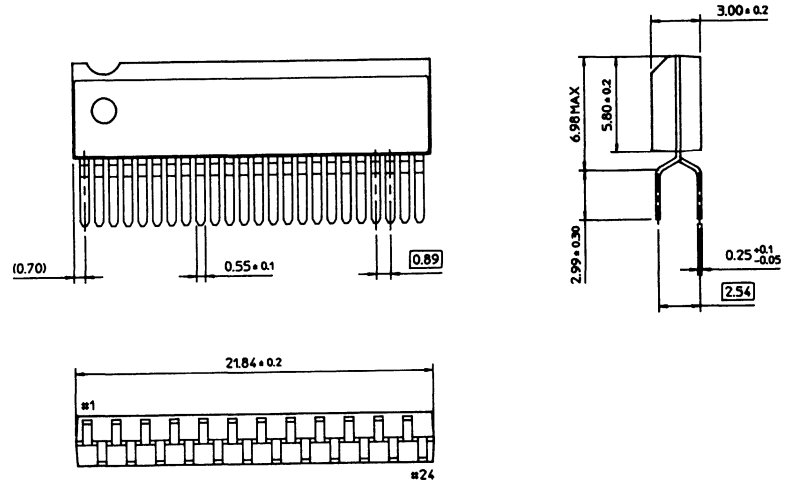
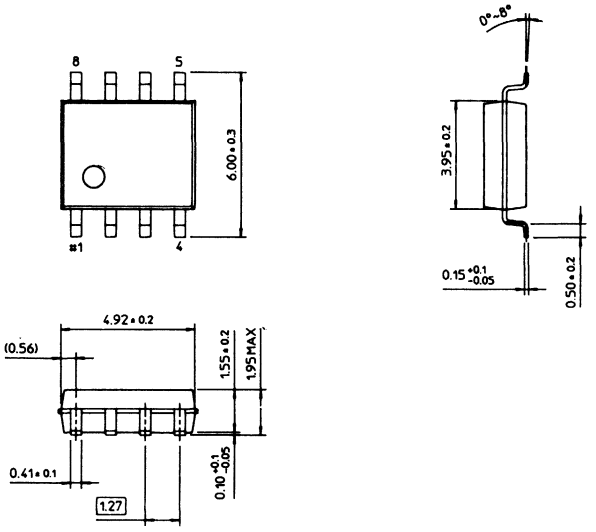


PACKAGE DIMENSIONS

Dimensions in Milimeters

8-SOP-225



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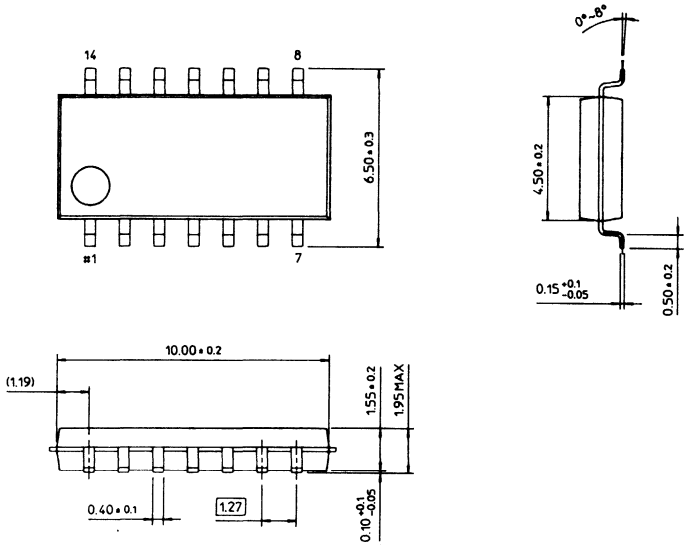
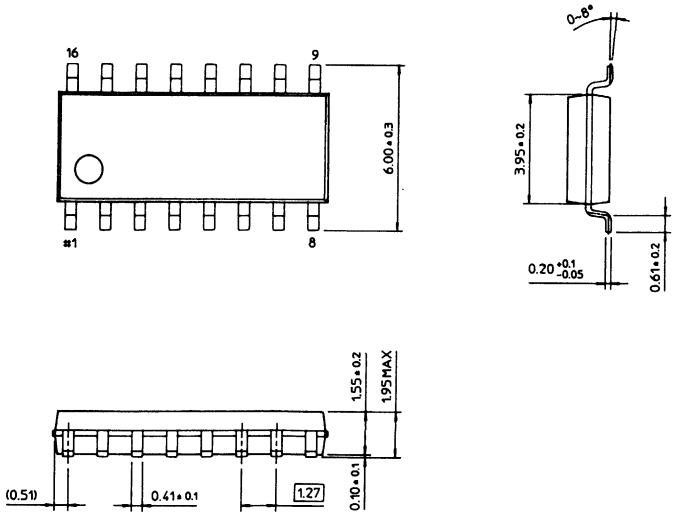


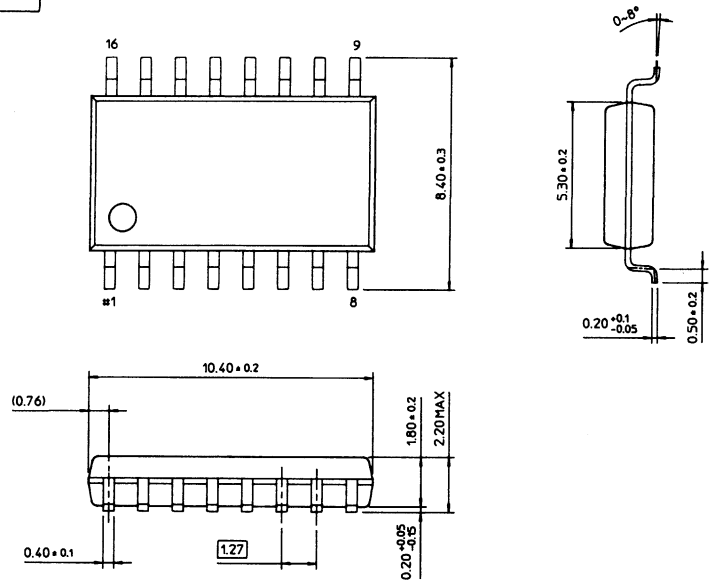
PACKAGE DIMENSIONS

Dimensions in Milimeters

16-SOP-225



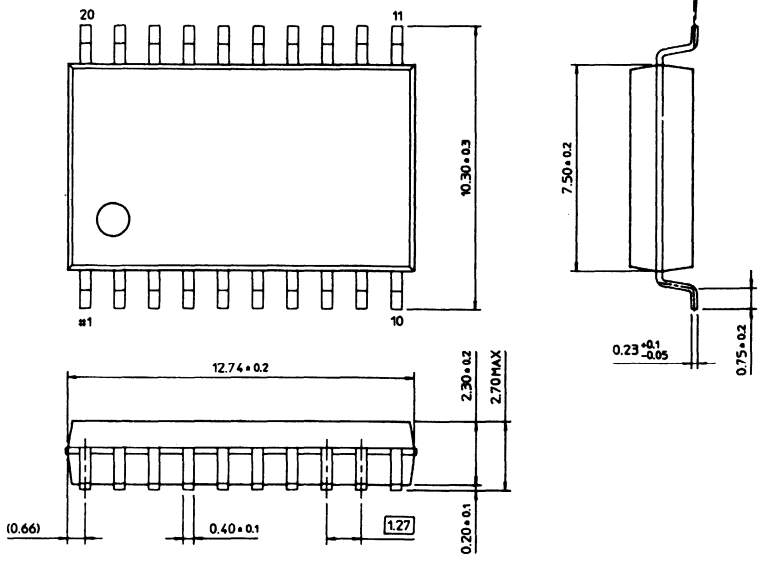
16-SOP-300



PACKAGE DIMENSIONS

Dimensions in Milimeters

20-SOP-375



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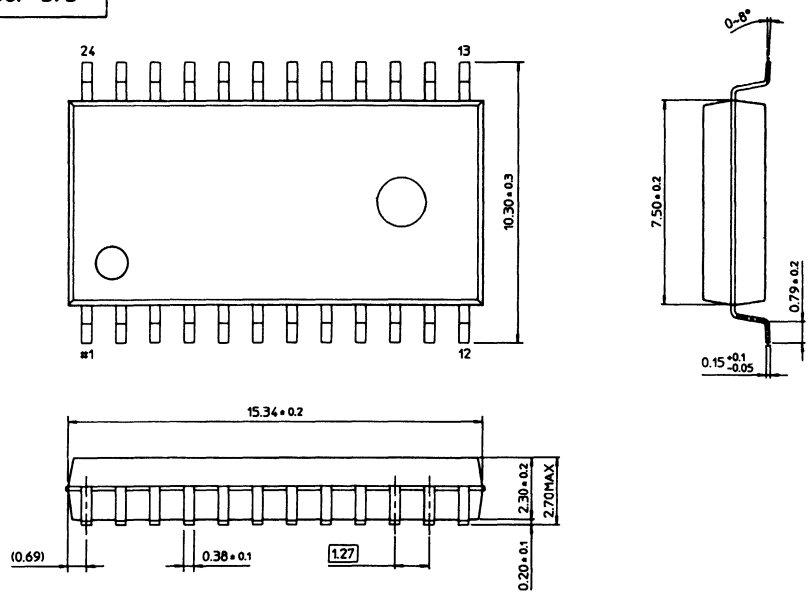
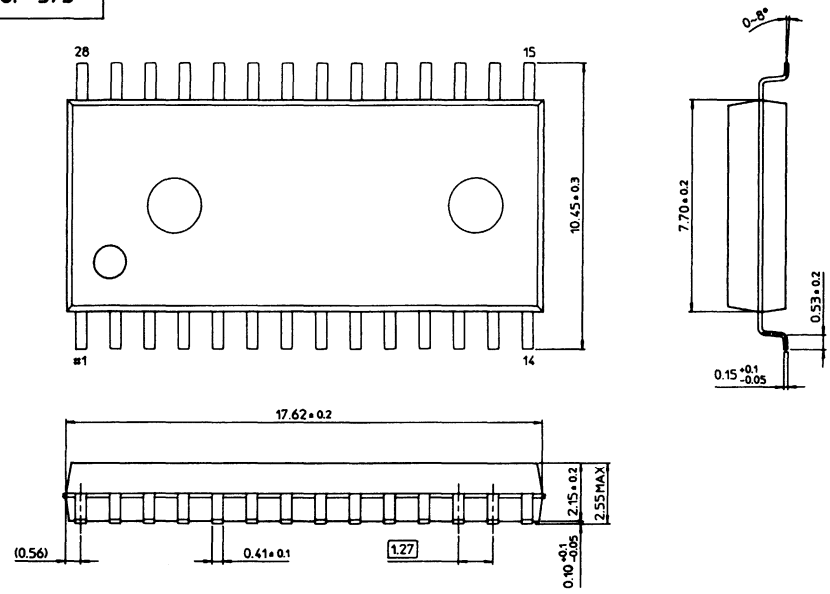


PACKAGE DIMENSIONS

Dimensions in Milimeters

28-SOP-375



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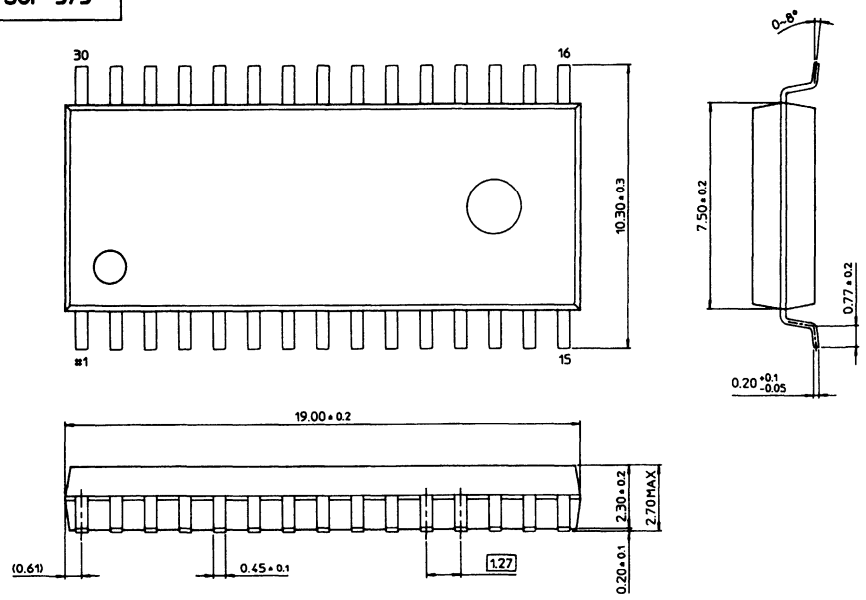
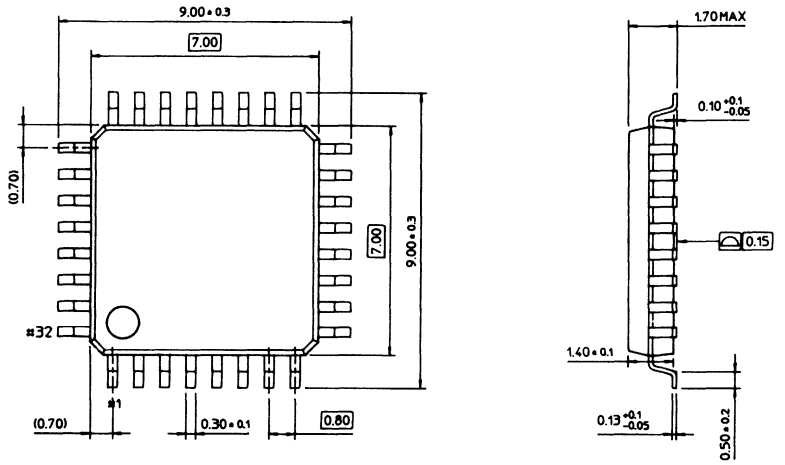


PACKAGE DIMENSIONS

Dimensions in Milimeters

32-QFP-0707



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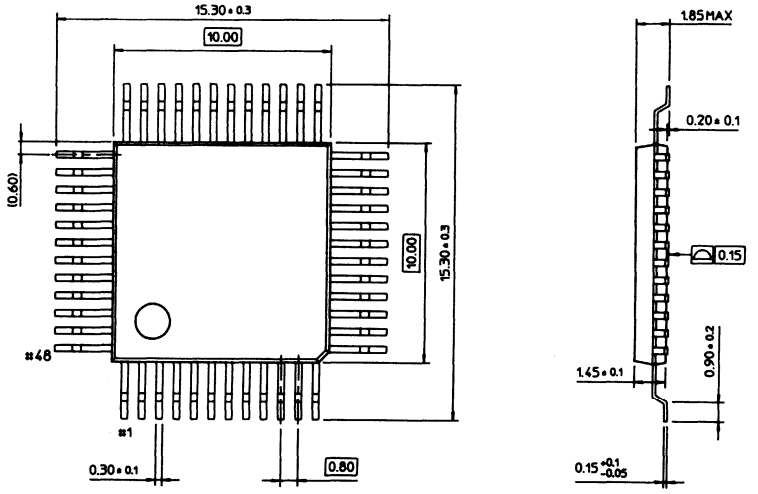
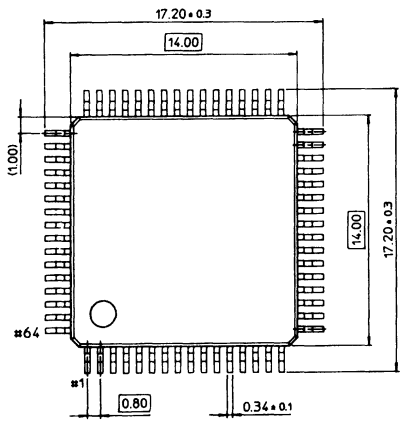
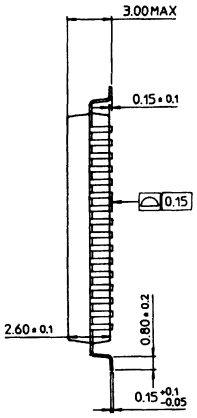


PACKAGE DIMENSIONS

Dimensions in Milimeters

64-QFP-1414





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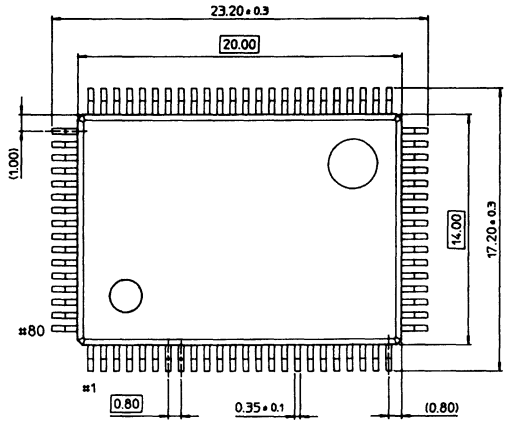
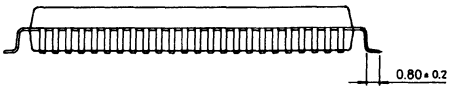
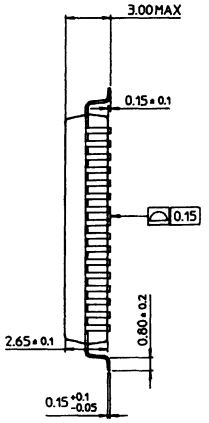


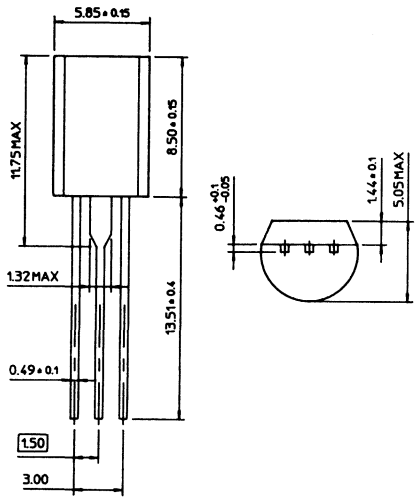




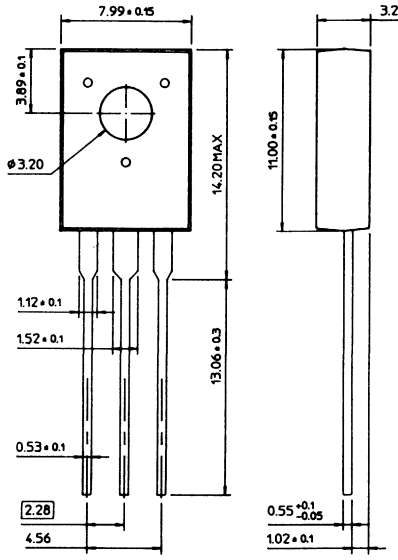
PACKAGE DIMENSIONS

Dimensions in Milimeters

TO-92L



TO-126



NOTES

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(708) 852-2011
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FAX: (617) 273-9363

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Dallas, TX 75248-3307
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FAX: (214) 770-7971

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Tustin, CA 92680
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FAX: (714) 832-7894

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Suite 217
Torrance, CA 90505
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FAX: (310) 539-2564

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Suite 204
Calabasas, CA 91302
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FAX: (403) 230-3183

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FAX: (416) 629-1795

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FAX: (407) 834-4524

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FAX: (317) 848-1264

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8819 Roman Court FAX: (502) 491-5250
Louisville, KY 40291

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